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Analysis and Calibration of Nonbinary-Weighted Capacitive DAC for High-Resolution SAR ADCs

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***Abstract*—This brief analyzes the effect of capacitor variation on the design of high-resolution nonbinary-weighted successive-approximation-register analog-to-digital converters in terms of radix, conversion steps, and accuracy. Moreover, the limitation caused by the one-side redundancy of the nonbinary-weighted network is addressed and a corresponding solution with a mathematical derivation is provided. In order to relax the mismatch requirement on the capacitor sizing while still ensuring enough linearity, a bottom-up weight calibration technique accounting for noise and offset errors is proposed, and its effectiveness is demonstrated. This calibration approach can be easily incorporated into a charge-redistribution converter without modifying its main architecture and conversion sequence.**

***Index Terms*—Capacitor variation, digital error correction, nonbinary weighted, redundancy, successive approximation, successive approximation register (SAR) analog-to-digital converters (ADCs), weight calibration.**

I. Introduction

SUCCESSIVE approximation register (SAR) analog-to-digital converters (ADCs) are well known for their exceptionally low power consumption [1], [2]. However, most studies have focused on moderate resolutions. Although the SAR architecture has been employed in an auxiliary role to enhance the high signal-to-noise ratio of pipelined ADCs [3], efficient design methodologies and circuit techniques for high-resolution stand-alone SAR ADCs have not been explored extensively. One of the limiting factors for SAR ADCs to achieve high resolution is the capacitor mismatch. One way to minimize the mismatch error is to size up the capacitor by paying the penalty of a larger area and lower speed. An alternative approach is using a smaller capacitive array together with some form of calibration. Analog calibrations using additional digital-to-analog converters (DACs) were proposed in the 1980s [4], [5]. Recently, more efforts [6]–[8] have been made to push calibration into the digital domain since the scaling of CMOS technology offers advantages of digital circuitry in terms of speed, power, and integration.

Equalization is a common digital calibration technique. Split-ADC equalization [6] implements two identical ADCs on the same chip, captures the difference between their outputs, and simultaneously calibrates their bit weights until the captured difference is minimized. To simplify this technique, a self-equalization approach [7] works on a single ADC by employing an offset double conversion scheme. The efficiency of equalization heavily depends on the input signal to achieve and accelerate convergence. Different from equalization, in this brief we introduce a digital calibration technique without applying any external input signal. It utilizes a concept similar to that in [8], in which the lower bit weights are assumed to be correct and the higher bit weights are measured and expressed by the lower bit weights. The concept applies to nonbinary-weighted converters. Compared with a binary-weighted converter, a nonbinary-weighted converter introduces redundancy during bit decision with more conversion steps, as shown in Fig. 1. Owing to the redundancy, the approximation of higher weights by lower weights is still feasible even when a certain amount of capacitor variation is taken into account. In [8], the converter combines a binary-weighted network with a ladder structure. To deal with the comparator offset during calibration, the converter needs to do double conversion with a specific requirement on the time sequence, which increases design complexity. Different from [8], in this brief the converter employs a subradix-2 single-array capacitive DAC, which has better tolerance to parasitics. Instead of double conversion, single normal successive approximation is performed. The effect of the comparator offset during calibration is then canceled by a subtraction in the digital postprocessing phase. Since the entire procedure does not affect the original conversion sequence of a charge-distribution SAR ADC, the calibration circuit can be easily incorporated into the converter without modifying its main architecture and digital logic.

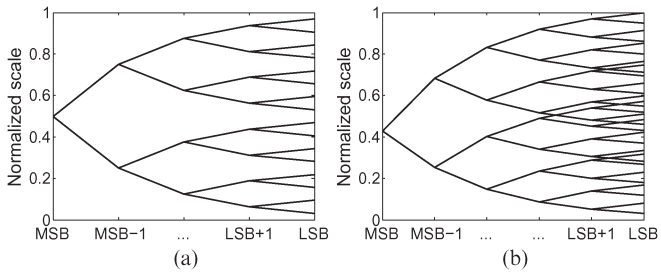

Fig. 1. Decision tree of a (a) binary-weighted converter and a (b) nonbinary-weighted converter.

Considering that the calibration applies to a subradix-2 single-array capacitive network, an in-depth understanding of the characteristics of such networks is beneficial. This brief analyzes the effect of capacitor variation on the design of a nonbinary-weighted capacitive DAC in terms of radix, conversion steps, and accuracy. In addition, this brief describes one important property associated with the nonbinary-weighted network, which is the one-side redundancy. It limits the ability of the ADC in correcting early decision errors due to insufficient settling or coupled noise by later decision steps. To solve this

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problem, a solution briefly discussed in [9] is introduced and a mathematical derivation of the solution is further provided.

This brief is organized as follows. Section II analyzes the characteristics of the nonbinary-weighted capacitive DAC. It starts with the analysis of the effect of capacitor variation and then moves to the one-side redundancy. Sections III and IV describe the calibration approach and present the simulation results, respectively. Section V concludes this brief.

II. Analysis of Nonbinary-Weighted DAC

A. Preliminaries

In order to achieve N-bit accuracy, the nonbinary-weighted converter with a radix $r(r < 2)$ requires S conversion steps $(S > N)$. The bit weight, which reflects the ratio between jth capacitor $C_j(S \geq j \geq 1)$ and total array capacitor $C_{\rm tot}$, is expressed as

$$W_j = \frac{C_j}{C_{\rm tot}}. \tag{1}$$

Based on the numerical weights and bit decisions D_i generated by the converter, the normalized input voltage can be represented by

$$V_{\rm IN} = \sum_{i=1}^{S} D_i W_i. \tag{2}$$

In order to ensure enough dynamic range of the nonbinary-weighted capacitive DAC with N-bit target accuracy, the following inequality should be satisfied [10]:

$$C_{\rm tot} > 2^N C_1. \tag{3}$$

The redundancy for bit j is expressed as

$$\text{Redundancy}(j) = \sum_{i=1}^{j-1} W_i - W_j. \tag{4}$$

It represents the overlap between the decision levels corresponding to digital code transitions involving $01\ldots1$ to $10\ldots0$. To guarantee the redundancy, it requires

$$\sum_{i=1}^{j-1} W_i > W_j. \tag{5}$$

Multiplying both sides with $C_{\rm tot}$, (5) can be further expressed in terms of the capacitor as

$$\sum_{i=1}^{j-1} C_i > C_j. \tag{6}$$

B. Accounting for Capacitor Variation

In this section, we analyze the effect of capacitor variation on the two inequalities, i.e., (3) and (6).

Each array capacitor is modeled as the sum of nominal capacitance and an error term [11]. The LSB capacitor as a unit capacitor is then modeled as

$$C_1 = C_u + \delta_1 \qquad E\left[\delta_1^2\right] = \sigma_u^2 \tag{7}$$

where C_u is the nominal capacitance, and δ_1 is a random variable with zero mean and a variance of σ_u^2. Then, the rest of the capacitors in the array can be modeled as

$$C_j = r^{j-1}C_u + \delta_j \qquad E\left[\delta_j^2\right] = r^{j-1}\sigma_u^2. \tag{8}$$

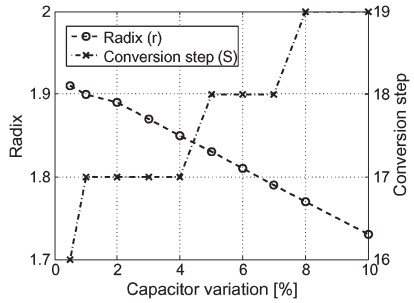

Fig. 2. Tradeoffs among σ_u/C_u, r, and S for 15-bit accuracy.

We first consider (3) by calculating the variance of $C_{\rm tot}$ as

$$\text{Var}[C_{\rm tot}] = \frac{1-r^S}{1-r}\sigma_u^2. \tag{9}$$

Further considering 3σ for a high yield, (3), accounting for capacitor variation, can be rewritten as

$$\frac{1-r^S}{1-r}C_u - 3\sqrt{\frac{1-r^S}{1-r}}\sigma_u > 2^N(C_u + 3\sigma_u). \tag{10}$$

Note that (10) is a conservative bound because the correlation between the variation in C_1 and $C_{\rm tot}$ is ignored. With further mathematical manipulation, (10) is finally expressed as

$$\frac{1-r^S}{1-r} - 2^N - 3\left(2^N + \sqrt{\frac{1-r^S}{1-r}}\right)\frac{\sigma_u}{C_u} > 0. \tag{11}$$

In a similar manner, (6), accounting for capacitor variation, can be written as

$$\frac{2r^{j-1} - r^j - 1}{r-1} - 3\left(\sqrt{r^{j-1}} + \sqrt{\frac{1-r^{j-1}}{1-r}}\right)\frac{\sigma_u}{C_u} > 0. \tag{12}$$

The radix determines the bit position at which redundancy starts. No redundancy is provided for the lower weighted bits. Given the standard deviation of the unit capacitor, (11) determines the minimum conversion steps under a certain radix for N-bit accuracy, and (12) determines the maximum radix for a specific bit position where the redundancy starts. A smaller radix introduces redundancy to more bits but also increases conversion steps. Fig. 2 depicts the tradeoffs among σ_u/C_u, r, and S for 15-bit accuracy. First, radix r is calculated according to (12) where the redundancy starts from bit 5. Second, the conversion step is calculated according to (11) with the chosen radix. This figure shows that a larger capacitor variation requires a smaller radix and thus needs more conversion steps.

C. Secondary Bit to Tackle One-Side Redundancy

Based on the decision tree of a nonbinary-weighted ADC, Fig. 3 shows the decision path after a wrong decision at the MSB approximation for two normalized input voltages. The three dashed lines indicate the level of the input voltage, the weight of the MSB, and the sum of the rest of the bit weights, respectively. The redundancy for the MSB, according to (4), is also indicated in this figure.

Now, assuming that a normalized input of 0.46 is applied to the ADC, as shown in Fig. 3(a), the expected decision for the MSB should be *High*, but a wrong decision of *Low* is

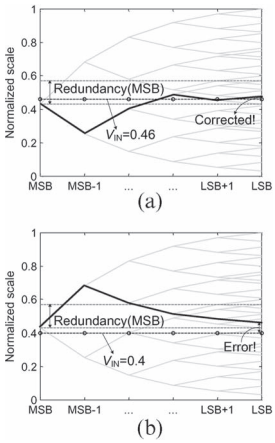

Fig. 3. Decision path (indicated by the black solid line) after a wrong decision at the MSB approximation for two normalized input voltages. (a) $V_{\rm IN} = 0.46$. (b) $V_{\rm IN} = 0.4$.

TABLE I
DISTANCE BETWEEN TWO BITS IN TERMS OF RADIX

radix	1.8	1.82	1.85	1.87	1.9
k (rounded)	4	4	4	4	4 or 5

made (underapproximation). In this case, as long as the input is covered by the redundancy range, the wrong decision can be still corrected by the later decision steps. Considering the opposite case of overapproximation, as shown in Fig. 3(b), the ADC gives a wrong decision of *High* for an input of 0.4 at the MSB decision step. Following the decision path, this wrong decision can never be corrected by the following steps.

The redundancy only helps correct underapproximation instead of overapproximation because it is at one side of the decision bit. Hence, it is important to shift the comparison threshold during the bit decision to the middle of the redundancy range [7], [9]. One way is to tie an extra capacitor bank to the original array and to increase the comparison threshold by switching on an additional capacitor together with the decision capacitor [7]. A more efficient approach is to simultaneously switch on two bits [9], in which one bit is the decision bit and the other is a lower weighted bit. The secondary bit has a weight about half of the redundancy. Once the decision is made, the secondary bit goes back to its initial status. In order to locate the position of the secondary bit, we write

$$W_j + \overbrace{\frac{1}{2}\cdot\left(\sum_{i=1}^{j-1} W_i - W_j\right)}^{\text{half of redundancy}} = W_j + W_{j-k} \tag{13}$$

where k indicates the distance between the secondary bit and the decision bit. With mathematical manipulation, (13) leads to the following approximation:

$$k \approx \frac{\log\frac{2(1-r)}{r-2}}{\log r}. \tag{14}$$

Table I shows the distance between two bits in terms of radix. It can be seen that a code distance of 4 works for all the listed radixes.

III. BOTTOM-UP WEIGHT CALIBRATION

Considering the variation of LSB capacitors contributing insignificant errors to the conversion accuracy, the bottom-up weight calibration approach uses the lower weights to measure and express the higher weights. The approach can be divided into two major steps: 1) the higher weights are sensed and digitized by the array via normal successive approximations; and 2) the correction of the higher weights are digitally applied afterward based on the conversion results. These two steps will be elaborated in Section III-A and B, respectively.

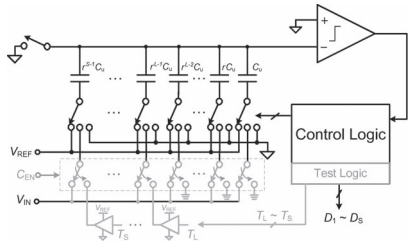

Fig. 4. SAR ADC incorporated weight conversion (the parts indicated by gray are the additional blocks).

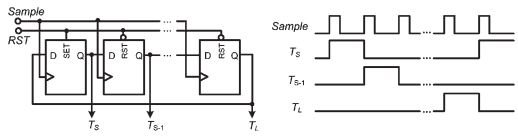

Fig. 5. Test logic to generate the calibration signals $(T_L \sim T_S)$ and the corresponding time sequence.

A. Weight Conversion

The first step of the calibration utilizes the successive approximation algorithm, and the conversion approach can be easily integrated into a charge-redistribution SAR ADC without modifying the basic architecture, as shown in Fig. 4. During the calibration mode, the control signal, which is denoted by $C_{\rm EN}$, switches the input branch from the input signal to the test signals. The test signals can be generated by a series of D-type flip-flops, as shown in Fig. 5.

The procedure of weight conversion is similar to that of a conventional SAR ADC. First, the information of the weight is sampled on the array, and then, the bit decisions from the MSB to the LSB are successively generated. Taking the MSB weight conversion as an example, during the sampling phase, as shown in Fig. 6(a), only MSB capacitor C_S is connected to the reference voltage, thereby sampling its weight information on the array. The next phase, as shown in Fig. 6(b), is the normal approximation of the MSB. Since the corresponding secondary bit is also switched on, it will result in a decision of *Low* for the MSB. After the first-bit approximation, the MSB capacitor is connected back to the ground, whereas capacitors of both MSB-1 and its secondary bit are connected to the reference voltage, as shown in Fig. 6(c). The approximation phase continues until the LSB decision is generated. A similar conversion procedure can be applied to other higher weights until W_L.

B. Bottom-Up Weight Calibration

Ideally, once all the conversions of the higher weights are complete, each of these bit weights is then expressed with the sum of its lower weights, which can be written as

$$W_j = \sum_{i=1}^{j-1} D_{i,j} W_i. \tag{15}$$

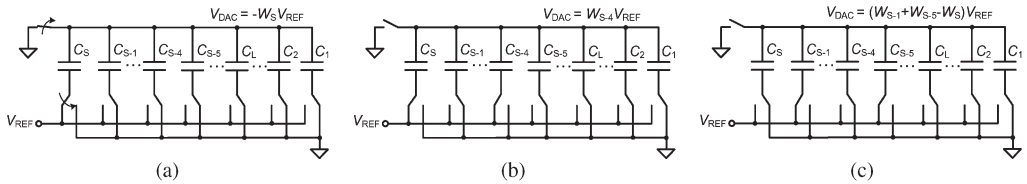

Fig. 6. DAC switching status during the conversion of the MSB weight (W_S). (a) Sampling. (b) First-bit approximation. (c) Second-bit approximation.

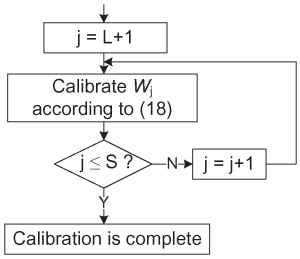

Fig. 7. Flowchart of the bottom-up weight calibration.

In reality, however, there exists offset during conversion. If the common-mode voltage of the DAC outputs is kept at the same level during the whole conversion, the effect of the signal-dependent dynamic offset from the succeeding comparator will be substantially reduced. Hence, the offset can be viewed as a constant static offset [12]. The conversion result of the bit weight, taking the offset into account, can be rewritten as

$$W_j \pm V_{\rm os} = \sum_{i=1}^{j-1} D_{i,j} W_i \tag{16}$$

where $V_{\rm os}$ is the normalized offset to the reference voltage. Since the offset is static, it can be canceled by subtracting the two consecutive converted results as

$$(W_j \pm V_{\rm os}) - (W_{j-1} \pm V_{\rm os}) = \sum_{i=1}^{j-1} D_{i,j} W_i - \sum_{i=1}^{j-2} D_{i,j-1} W_i. \tag{17}$$

Finally, W_j can be written as

$$W_j = W_{j-1} + \sum_{i=1}^{j-1} D_{i,j} W_i - \sum_{i=1}^{j-2} D_{i,j-1} W_i. \tag{18}$$

The flowchart of the bottom-up weight calibration is given in Fig. 7. The calibration starts from W_{L+1} by correcting its value according to (18). Then, based on the calibrated weight, the next higher weight W_{L+2} is corrected and updated. The procedure continues until all the remaining higher weights are calibrated.

The existence of offset will limit the number of weights to be converted. Fig. 8 shows weight conversion including either a positive offset or a negative offset. For the specific bit weight, its conversion range is between 0 and the sum of all its lower weights. Hence, in order to make it possible for the bit weight to be converted by its lower weights, the offset voltage should satisfy

$$V_{\rm os} \le \sum_{i=1}^{j-1} W_i - W_j, \quad \text{for positive offset} \tag{19}$$

$$V_{\rm os} \le W_j, \quad \text{for negative offset.} \tag{20}$$

Apart from the offset, the noise will also affect the conversion result. To overcome the noise effect, averaging can be used. The

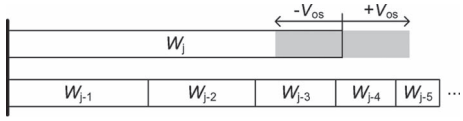

Fig. 8. Weight conversion with the existence of offset.

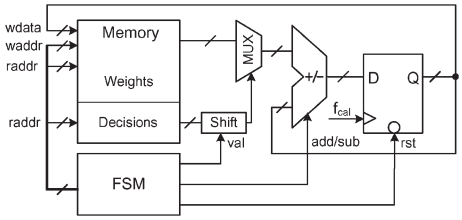

Fig. 9. Block diagram of the digital calibration logic.

ADC first converts the higher weights for multiple runs, and then, the decisions are averaged. Unlike the offset and noise, the gain error scales the bit weights by the same factor; hence, it will not affect the converted weight expression. Fig. 9 shows the block diagram of the digital calibration logic. The power and area of the calibration logic are estimated in Section IV.

IV. Simulation Results

A behavioral model of a 15-bit 1.85-radix 1-V SAR ADC with 17 conversion steps is created in Matlab, and the model accounts for the capacitor variation, the comparator offset, and noise. Since we are more interested in characterizing the effectiveness of the calibration method, the ADC is simulated in Matlab instead of Cadence to avoid other circuit nonidealities. In addition, Matlab allows us to run extensive Monte Carlo simulations, which otherwise will be extremely time consuming to run in Cadence.

In addition to the ideal case, three more offsets are chosen, i.e., $+0.01$, -0.01, and -0.001. The noise power is assumed to be equal to the quantization noise power of a 15-bit radix-2 ADC. The capacitor variation (σ_u/C_u) is chosen to be 3%. The ADC first calibrates the higher weights based on the average result of 16 runs. Then, it converts a sinusoidal input signal, and the signal-to-noise-and-distortion ratio (SNDR) of the converted result is evaluated. A total of 500 Monte Carlo simulations were performed to obtain the mean and standard deviation of the SNDR. Fig. 10 shows the simulated results versus the numbers of calibrated weights. The calibration improves the performance by increasing the mean and decreasing the standard deviation. A smaller offset allows the ADC to calibrate more weights, thus leading to a higher SNDR. It can be also seen that, with the same amount of offsets, the positive offset limits the ADC to calibrate fewer bit weights compared with the negative offset. The $+0.01$-, -0.01-, and -0.001-$V_{\rm os}$ limit the number of calibrated weights to 3, 6, and 9 bits, respectively. When it comes to the ideal case, the improvement stops at 11 bits.

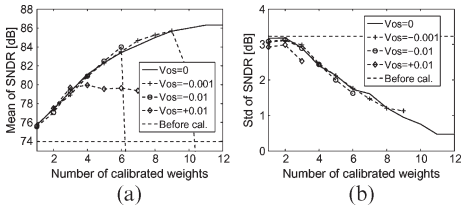

Fig. 10. Simulated SNDR versus the numbers of calibrated higher weights for $\sigma_u/C_u = 3\%$. (a) Mean. (b) Standard deviation.

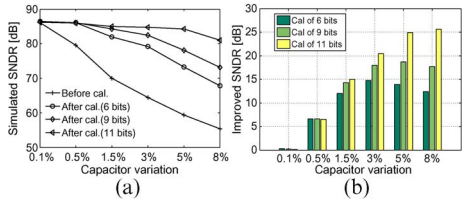

Fig. 11. Comparison between before and after the calibration. (a) Simulated SNDR (mean $-\ 3\sigma$). (b) Improved SNDR after the calibration. (The total number of calibrated weights is indicated.).

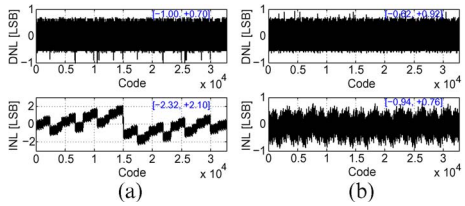

Fig. 12. DNL/INL plots of an ADC with $\sigma_u/C_u = 1.5\%$. (a) Before the calibration. (b) After the calibration of nine bits.

Fig. 11(a) shows the simulation results based on more values of capacitor variation. The reported SNDR is calculated as the mean value subtracted by 3σ. Fig. 11(b) illustrates the improvement after the calibration. For a sufficiently small capacitor variation, e.g., 0.1%, the weights do not deviate much, and there is no need to go for calibration. For a relatively small capacitor variation, e.g., 0.5%, calibrating more weights does not provide proportional improvement in the SNDR. As the variation increases, the higher weights deviate more, resulting in a worse SNDR before calibration. As the number of calibrated weights increases, different matching cases almost approach the same level of performance. Furthermore, it is also informative to visualize the improvement of the ADC linearity after calibration. As an example, Fig. 12 shows the differential nonlinearity (DNL)/integral nonlinearity (INL) plots of the ADC with a capacitor variation of 1.5% and an offset of -0.001 (nine calibrated bits) before and after the calibration. The peak DNL error is changed from $-1.00/+0.70$ LSB to $-0.62/+0.92$ LSB, and the peak INL error is changed from $-2.32/+2.10$ LSB to $-0.94/+0.76$ LSB. The calibration helps remove the missing codes and improve the ADC linearity.

After synthesis in Design Compiler, the estimated area of the calibration logic is about 0.01 mm^2, and the power is about 0.05 mW at 10 MHz in the standard 65-nm CMOS process. The estimated calibration time is about 500 clock cycles, in which 200 cycles is for weight conversion and 300 cycles is for digital calibration. Since this technique is input independent, the digital calibration does not need to simultaneously run with the ADC. Once the weight information is sensed, digitized, and stored, the digital postprocessing can be run offline at an arbitrary frequency. Table II compares this brief with other digital calibration techniques.

TABLE II
COMPARISON WITH OTHER DIGITAL CALIBRATION TECHNIQUES

	[6]	[7]	This work
Resolution [bit]	16	12	15
Radix	2	1.86	1.85
Conversion steps	16	14	17
Input-dependent	Yes	Yes	No
Frequency [MHz]	1	22.5	10
No. of cycles	200,000	22,000	500
Area (est.) [mm^2]	0.8	0.03	0.01
Power (est.) [mW]	2.6	0.23	0.05
SNDR [dB]	-	70	84 †
DNL/INL [LSB]	better than ±1	-	[-0.62 +0.92]/[-0.94 +0.76] †

† $\sigma_u/C_u = 1.5\%$ and 9 bits are calibrated, simulation results

V. CONCLUSION

The effect of capacitor variation on the design of nonbinary-weighted capacitive DACs has been analyzed. It shows that a larger capacitor variation requires a smaller radix and needs more conversion steps. In addition, to tackle the one-side redundancy, a secondary-bit approach has been utilized. Hence, the ADC can correct decision errors from both underapproximation and overapproximation. Finally, a bottom-up weight calibration approach has been proposed. Simulations based on a behavioral model of a 15-bit 1.85-radix ADC demonstrates that both the SNDR and the DNL/INL are improved after calibration.

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