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Modeling and Analysis of Harmonic Spurs in DLL-Based Frequency Synthesizers

Amin Ojani, *Student Member, IEEE*, Behzad Mesgarzadeh, *Member, IEEE*, and Atila Alvandpour, *Senior Member, IEEE*

Abstract—Periodic jitter raises the harmonic spurs at frequency synthesizer output spectrum, down-converting the out-of-band interferers into the desired band and corrupting the wanted signal. This paper proposes a comprehensive behavioral model for spur characterization of edge-combining delay-locked loop (DLL)-based synthesizers, which includes the effects of delay mismatch, static phase error (SPE), and duty cycle distortion (DCD). Based on the proposed model and utilizing Fourier series representation of DLL output phases, an analytical model which formulates the synthesizer spur-to-carrier ratio (SCR) is developed. Moreover, from statistical analysis of the analytical derivations, a closed-form expression for SCR is obtained, from which a spur-aware synthesizer design flow is proposed. Employing this flow and without Monte Carlo (MC) method, one can determine the required stage-delay standard deviation (SD) of a DLL-based synthesizer, at which a certain spurious performance demanded by a target wireless standard is satisfied. A design example is presented which utilizes the proposed design flow to fulfill the SCR requirement of -45 dBc for WiMedia-UWB standard. Transistor-level MC simulation of the synthesizer SCR for a standard 65-nm CMOS implementation exhibits good compliance with analytical models and predictions.

Index Terms—delay mismatch, DLL, duty cycle distortion, edge-combiner, frequency synthesizer, harmonic spur, periodic jitter, static phase error.

I. INTRODUCTION

DELAY-LOCKED loop (DLL)-based frequency multipliers have expanded their applications during the last decades into wireless communication systems [1]-[8]. Essential DLL characteristics such as the relatively wide loop-bandwidth, fast lock-in time, limited-accumulative jitter, and first-order stability, indicate the potentials of DLL-based frequency generation schemes [9]. However, designing such systems for RF applications, where carrier signals of certain spectral purity must be provided, has its own challenges. Since the accumulated random jitter within the delay line is reset back to zero at every reference clock edge, edge-combining DLL-based synthesizers exhibit a flat phase noise profile [1], [4]. On the other hand, as the DLL is locked to the reference period and the carrier is generated by combining the equally-spaced DLL edges, any misalignment of those edges result in periodic jitter and raises the reference harmonic spurs at synthesizer output spectrum, down-converting the out-of-band

interferers into the desired band. One of the major contributors to the level of spurious tones in such synthesizers is the duty cycle distortion (DCD) of the reference clock as well as the internal DLL phases. In addition, the static phase error (SPE) between the reference and feedback signals caused by up/down pulsewidth and current imbalances in phase detector (PD) and charge pump (CP) respectively, deteriorates the spurious performance. Moreover, delay mismatches among delay stages in the delay line, made by the local manufacturing imperfections, will also lead to harmonic spurs. Implied by the matching properties of MOS devices [10], to minimize the delay mismatch between delay stages, large-area devices should be utilized. Due to stochastic nature of the mismatch, statistical simulations such as Monte Carlo (MC) with large number of samples should be performed for accurate prediction of the synthesizer spurious performance. However, for such complex and limited-bandwidth feedback systems which require a large settling time for each MC sample, circuit-level MC becomes extremely cumbersome. Now consider that to satisfy a certain requirement on harmonic spurs and to avoid over-sizing the delay stages which leads to area and speed penalties, optimal device sizes need to be found by iteratively improving the circuit parameters and performing a new set of circuit-level MC to verify the obtained performance. Consequently, to accelerate the design procedure, it is crucial to develop an accurate behavioral model of the spur characteristics of DLL-based synthesizers, which includes all the main sources of periodic jitter. A thorough analytical model which formulates the spurious performance in terms of DCD, SPE and delay standard deviation (SD) is hence of great interest. A few works [4], [11]-[12] have studied the spur characteristics of edge-combining synthesizers, from which [4] and [11] limit their analysis solely to the effect of SPE. In [12], the effect of delay mismatch is also included, but the model is customized only for rising edge combiners (EC) and does not consider the effect of DCD on synthesizer's harmonic spurs. When both the clock edges of the DLL phases are used by the EC, the duty cycle variations of those phases will generate a periodicity. This implies that besides SPE and delay SD, the levels of harmonic spurs become also a function of DCD, which is not modeled in [12]. Therefore, it cannot be employed as a general model of edge-combining synthesizers for spur characterization.

In this work, we propose a comprehensive behavioral model of edge-combining DLL-based synthesizers, which includes

Fig. 1. (a) Block diagram of a DLL-based EC frequency synthesizer, (b) a V-I converter stage of EC, and (c) an active implementation of the delay stage.

the impact of DCD as well as the SPE and delay mismatch, on synthesizer spurious performance. Utilizing this model and the Fourier series representation of multiphase DLL outputs, an analytical model is developed, formulating the synthesizer spur-to-carrier ratio (SCR). We further expand our analysis by aid of statistical methods, to obtain a closed-form expression for mean SCR and its probability density function (PDF). Utilizing our closed-form formula, we propose a spur-aware synthesizer design methodology. Employing this design flow and without MC simulations, the required delay SD which satisfies a certain SCR requirement, can be accurately estimated. Based on the calculated delay SD, one can design the corresponding delay stage circuit.

The paper is organized as follows. Section II proposes a behavioral model of edge-combining DLL-based synthesizers. In Section III, an analytical model is derived from the Fourier series representation of multiphase DLL outputs. Statistical analysis which results in a close-form expression for synthesizer's spur levels is presented in Section IV. In Section V, a spur-aware synthesizer design methodology is proposed which is utilized in the design example of Section VI to find the required stage-delay SD which satisfies the spurious performance of a WiMedia ultra-wideband (UWB) standard. Finally, the paper is concluded in Section VII.

II. BEHAVIORAL MODEL OF DLL-BASED SYNTHESIZERS

Consider the edge-combining DLL-based synthesizer diagram shown in Fig. 1(a), where the system is locked to a reference clock frequency f_{ref} and generates a carrier at $f_c = N \times f_{ref}$ by combining N evenly-spaced DLL phases. To characterize the spurious performance, we propose a behavioral feedforward model of the in-lock synthesizer, which considers the effects of the delay mismatch, DCD, and SPE. Note that the model is developed based on a rising-falling current summation EC [1] which employs voltage-to-current (V-I) converter stages shown in Fig. 1(b). The architecture requires a voltage-controlled delay line (VCDL) with odd number of delay stages N . Nevertheless, the model is generic and can be applied to synthesizers of other types of DLL/EC configurations. To model the delay mismatch, we assume that the delay of each stage is a random variable of normal distribution. Note that in active implementations of the delay stage such as the one in Fig. 1(c), pull-up and pull-down parts responsible for delaying the falling and rising edges

Fig. 2. Waveform representation of N -stage DLL-based synthesizer including DCD, SPE and delay mismatch effects.

Fig. 3. Proposed Time-domain feedforward model of in-lock DLL-based EC synthesizer.

respectively, are of different physical properties. This implies that the rising edge time delay $\Delta t_{d,r}$ and falling edge time delay $\Delta t_{d,f}$, experience different mismatch profiles. Therefore, we model them as two independent Gaussian random variables

$$\Delta t_{d,r} \sim N(\mu_r, \sigma_r^2), \Delta t_{d,f} \sim N(\mu_f, \sigma_f^2) \quad (1)$$

where μ_r , σ_r^2 , μ_f , and σ_f^2 are the mean and variance of $\Delta t_{d,r}$ and $\Delta t_{d,f}$, respectively. A waveform representation of the proposed synthesizer model is illustrated in Fig. 2. To determine $\Delta t_{d,r}$ and $\Delta t_{d,f}$, we assume that the DLL is locked to the reference clock period T_{ref} , but with a time-domain SPE of T_{spe} . So, the total VCDL delay length would be

$$T_{VCDL} = T_{lock} = T_{ref} + T_{spe}. \quad (2)$$

We assume that the mean of the rising and falling edge delays are equal. So, for the in-lock DLL with an N -stage VCDL,

$$\mu_r = \mu_f = \mu = T_{lock} / N. \quad (3)$$

Hence, $\Delta t_{d,r}$ and $\Delta t_{d,f}$ for the m^{th} delay stage, are represented as

$$\Delta t_{d,rm} = \frac{T_{lock}}{N} - t_{avg} + G_{rm}, \Delta t_{d,fm} = \frac{T_{lock}}{N} - t_{avg} + G_{fm} \quad (4)$$

where $m \in [1, N]$, and G_{rm} and G_{fm} are independent zero-mean Gaussian variables, representing the delay mismatch of rising and falling edges, respectively, and extracted from $\Delta t_{d,r}$ and $\Delta t_{d,f}$ to simplify the analysis. So,

$$G_{r1}, \dots, G_{rN} \sim N(0, \sigma_r^2), G_{f1}, \dots, G_{fN} \sim N(0, \sigma_f^2). \quad (5)$$

Note that t_{avg} is an offset delay which is applied by the locked-loop to all the stages, such that despite the delay mismatch, the total VCDL delay length maintains equal to T_{lock} . In our feedforward model, this actually models the mismatch-averaging characteristic of the in-lock DLL. To calculate t_{avg} , we assume a rising-edge-locked system. So,

$$T_{lock} = \sum_{m=1}^N \Delta t_{d,rm}. \quad (6)$$

In addition, we can write from (4) that

$$\sum_{m=1}^N \Delta t_{d,rm} = T_{lock} - N t_{avg} + \sum_{m=1}^N G_{rm}. \quad (7)$$

Now, from (6) and (7), t_{avg} is found as a random variable that consists of the averaged sum of N random variables that is

$$t_{avg} = \frac{1}{N} \sum_{m=1}^N G_{rm} \sim N(0, \sigma_r^2 / N). \quad (8)$$

Note that parameter k (Fig. 2) models the input clock pulsewidth. So, the time-domain DCD value T_{dcd} is written as

$$T_{dcd} = (T_{ref} / 2) - k \quad (9)$$

Also note that as mentioned previously, apart from the DCD of the reference clock, the duty cycle is also distorted due to the inherent differences in physical properties of pull-up and pull-down devices. By linearity, it can be shown that the so-called internal duty cycle distortion (IDCD) within a delay stage follows a normal distribution defined as

$$IDCD = \Delta t_{d,r} - \Delta t_{d,f} \sim N(\mu_r - \mu_f, \sigma_r^2 + \sigma_f^2). \quad (10)$$

The above expression implies that an accurate ratio sizing between the pull-up and pull-down devices, as assumed in (3), can only eliminate the mean of IDCD, demonstrating that the inter-stage DCD is correlated to the delay mismatch.

Fig. 3 depicts the time-domain block diagram of our feedforward model where the combined output, containing the fundamental as well as reference harmonic components, is generated by summation of the time-shifted versions of the rising and falling reference clock edges. The model is implemented in MATLAB and the SCR at synthesizer's output spectrum for each MC sample (of randomized G_r and G_f values) is calculated by taking the fast Fourier transform (FFT) of the output signal. This model is employed as a reference for spurious performance analysis in upcoming sections.

III. ANALYTICAL MODELING USING FOURIER SERIES

Based on the introduced behavioral model in Section II, we develop an analytical model which formulates the synthesizer spurious performance in terms of DCD, SPE and delay SD. Containing the magnitude, phase and frequency information of periodic signals, Fourier series are efficient tools for analyzing the square wave multiphase DLL outputs. In Appendix A, we derive the Fourier series of the EC output signal from those of the DLL output phases according to Fig. 2. As a result, a_n Fourier coefficient of the synthesizer output is represented as

$$\begin{aligned} a_n &= \frac{2A_0}{T_{ref}} \sum_{m=1}^N \left(\int_{m\mu + \sum_{i=1}^m G_{ri} - m t_{avg}}^{k + m\mu + \sum_{i=1}^m G_{fi} - m t_{avg}} \cos(n\omega_{ref} t) dt \right) \\ &= \frac{2A_0}{n\pi} \sum_{m=1}^N \left[\sin \frac{n\pi}{T_{ref}} (k + X_{fm} - X_{rm}) \right. \\ &\quad \left. \cos \frac{n\pi}{T_{ref}} \left(\frac{2m(T_{ref} + T_{spe})}{N} + k + X_{fm} + X_{rm} \right) \right] \end{aligned} \quad (11)$$

where A_0 , ω_{ref} , and n are the amplitude, angular frequency and (integer) harmonic index of the reference clock, respectively, and X_{fm} and X_{rm} are random variables defined as

Fig. 4. MC histogram of mean SCR; behavioral vs. analytical model (15).

$$X_{fm} = -\frac{m}{N} \sum_{i=1}^N G_{ri} + \sum_{i=1}^m G_{fi}, \quad X_{rm} = -\frac{m}{N} \sum_{i=1}^N G_{ri} + \sum_{i=1}^m G_{ri}. \quad (12)$$

Similarly, for b_n coefficient of the EC output, we can write

$$\begin{aligned} b_n &= \frac{2A_0}{n\pi} \sum_{m=1}^N \left[\sin \frac{n\pi}{T_{ref}} (k + X_{fm} - X_{rm}) \right. \\ &\quad \left. \sin \frac{n\pi}{T_{ref}} \left(\frac{2m(T_{ref} + T_{spe})}{N} + k + X_{fm} + X_{rm} \right) \right] \end{aligned} \quad (13)$$

We can now find the magnitude of the vector (a_n, b_n) which represents the output spur magnitude for a given harmonic n located at $f_s = n \times f_{ref}$. Thus,

$$S_n = |a_n + jb_n| = \sqrt{a_n^2 + b_n^2}. \quad (14)$$

The synthesizer's SCR magnitude is therefore expressed as

$$SCR_n = \frac{S_n}{C} = \frac{|a_n + jb_n|}{|a_N + jb_N|} = \frac{\sqrt{a_n^2 + b_n^2}}{\sqrt{a_N^2 + b_N^2}} \quad (15)$$

where C is the fundamental tone (carrier) magnitude, located at f_c and calculated from (14) for $n = N$. To verify the derived analytical expression, Fig. 4 compares the MC histogram of the SCR distribution obtained from our reference behavioral model, with that of attained from the analytical model (15). Note that for the simulations presented in the current section as well as in Section IV, we utilize the following parameters, unless otherwise specified. The reference clock is $f_{ref} = 400$ MHz and the VCDL has $N = 25$ stages, generating a carrier at $f_c = 25 \times 400$ MHz. The SCR is simulated for the largest spur located at $f_s = f_c - f_{ref}$ ($n = N - 1$). Furthermore, T_{dcd} and T_{spe} are assumed to be 10% and 1% of the mean stage-delay $\mu = 100$ ps, which are 10 ps and 1 ps, respectively. Also, the numerical rising and falling edge delay SD values are $\sigma_r / \mu = \sigma_f / \mu = 1\% = 1$ ps. Now, to acquire a better insight into (15), we depict the dependence of the mean SCR, as a function of the delay SD, DCD, SPE, and N . It can be observed from Fig. 5(a) and (b) that the SCR is solely defined by the delay SD for small values of DCD and SPE, respectively, and as these parameters get larger, the SCR becomes a function of DCD and SPE as well. Therefore, it is crucial to maintain DCD and SPE sufficiently small, so that we can efficiently get benefit from reducing the delay SD. On the other hand, for a given delay SD, over-improving the SPE and DCD, might not have a significant contribution in lowering the level of spurs, as there exists a lower bound on SCR defined by the delay SD. For this specific example, it can be observed from Fig. 5(a) and (b), that even with a quite small delay SD of $\sigma / \mu = 0.2\%$, pushing T_{dcd} and T_{spe} below 10 ps and 1 ps, respectively, would not improve

Fig. 5. Simulated mean SCR of the synthesizer from the analytical expression (15), as a function of normalized: (a) DCD, (b) SPE, and (c) stage-delay SD.

Fig. 6. Graphical test of criteria (16) for a_n and b_n ($n = N - 1$): (a) in-lock normality, (b) open-loop normality, and (c) zero-mean and equal-variance.

SCR much. Also for the case of $\sigma/\mu = 1\%$, it can be noted from Fig. 5(b) that by pushing T_{spe} below 5 ps, we do not gain any further spur suppression. Fig. 5(c) illustrates how the SCR changes as the delay SD varies for different N . As can be observed, for fixed DCD and SPE, and a given normalized delay SD of $\sigma/\mu = 1\%$, increasing N from 5 to 25 to achieve a higher carrier frequency of 5 times, results in about 7 dB degradation in spurious performance, even though the delay SD is scaled with N to keep σ/μ constant.

IV. CLOSED-FORM EXPRESSION FOR SYNTHESIZER SCR

In this section, we further expand our analytical model from the previous section by utilizing moment methods and Taylor series approximations, and obtain closed-form expressions for the mean and PDF of SCR at synthesizer output spectrum. As a result, we can estimate the synthesizer spurious performance without performing MC. In part A, we analyze the random variable S_n (14), i.e. the harmonic spur magnitude, and show that it can be approximated as a Rayleigh random variable. To estimate the SCR distribution (15), we show in part B that the random variable C , i.e. the carrier magnitude, can be approximated as a constant value that is equal to its mean.

A. Magnitude of Spurious Tones

Provided that the spur Fourier coefficients a_n and b_n at the EC output represented by (11) and (13), are two independently and identically distributed (iid) Gaussian random variables of zero mean and equal variances σ_{cof}^2 , i.e.,

$$a_n \sim N(0, \sigma_{cof}^2), \quad b_n \sim N(0, \sigma_{cof}^2) \quad n \neq N, \quad (16)$$

then the spur magnitude $S_n = \sqrt{a_n^2 + b_n^2}$ will be a Rayleigh

random variable [13]. Assuming a_n and b_n are independent, if the criteria of (16) are satisfied, we can efficiently characterize the harmonic spurs of the synthesizer, using the properties of Rayleigh distribution. To investigate (16), we start from the normality test. Statistical approaches involve calculation of skewness and kurtosis of the coefficients. In this work, we use graphical approach which has less complexity and works well for our approximation. Using (11) and (13), the MC histograms of the output spur Fourier coefficients are plotted in Fig. 6(a), indicating that a_n fits well within its corresponding Gaussian dashed curve. The observed skew in b_n histogram is due to the rising-edge-delay mismatch averaging characteristic of the DLL, whose averaged value t_{avg} is applied to both the rising and falling edge delays, according to (4). This can be verified by plotting the histograms in Fig. 6(b), for an open-loop case ($t_{avg} = 0$), where no skew on b_n is observed. Nevertheless, as the skew in the closed-loop case is small, b_n coefficient is also considered as a normal variable.

To evaluate the Fourier coefficients of the output spur as a function of delay SD, we utilize the variance formula of

$$\text{var}[X] = E[X^2] - (E[X])^2 \quad (17)$$

in which $E[X]$ is the expectation operator. It can be inspected from Fig. 6(c), that for small delay SDs, the variance and second moment $E[X^2]$ are equal for each coefficient, indicating that the corresponding mean values $E[X]$ are sufficiently small to be considered as zero. In addition, it can be noted that the variance of a_n and b_n are almost identical for small SDs. This implies that the criteria of (16) can be considered as valid as long as the delay SD maintains sufficiently small. This is in fact the case in the context of frequency synthesis with stringent requirements on spur levels. Therefore, we

Fig. 7. Predicted and simulated (a) mean, and (b) variance of the Fourier coefficients a_n and b_n of the output spur, as a function of normalized delay SD.

approximate the magnitude of the output spurs S_n as a Rayleigh random variable with PDF and mean that are expressed respectively as

$$p_X(x) = \begin{cases} (x/\sigma_{cof}^2) \exp(-x^2/2\sigma_{cof}^2) & x \geq 0 \\ 0 & x < 0 \end{cases} \quad (18)$$

$$E[S_n] = \sigma_{cof} \sqrt{\pi/2} \quad (19)$$

where $\sigma_{cof}^2 = \text{var}[a_n] \approx \text{var}[b_n]$. To determine (18) and (19), we need to find the first and second moments of the output Fourier coefficients, and calculate their variance from (17). So, we expand the expression for a_n coefficient in (11) as

$$a_n = \frac{A_n}{2} \sum_{m=1}^N \left[\alpha_m \kappa_s (\cos(2\lambda X_{fm}) + \cos(2\lambda X_{rm})) + \alpha_m \kappa_c (\sin(2\lambda X_{fm}) - \sin(2\lambda X_{rm})) - \beta_m \kappa_s (\sin(2\lambda X_{fm}) + \sin(2\lambda X_{rm})) - \beta_m \kappa_c (\cos(2\lambda X_{rm}) - \cos(2\lambda X_{fm})) \right] \quad (20)$$

where

$$A_n = \frac{2A_0}{n\pi}, \quad \lambda = \frac{n\pi}{T_{ref}}, \quad \kappa_s = \sin \frac{kn\pi}{T_{ref}}, \quad \text{and} \quad \kappa_c = \cos \frac{kn\pi}{T_{ref}} \quad (21)$$

$$\alpha_m = \cos \left(\frac{n\pi}{T_{ref}} \left[\frac{2m}{N} (T_{ref} + T_{spe}) + k \right] \right) \quad (22)$$

$$\beta_m = \sin \left(\frac{n\pi}{T_{ref}} \left[\frac{2m}{N} (T_{ref} + T_{spe}) + k \right] \right). \quad (23)$$

In Appendix B, we first simplify (20) by utilizing the first and second-order Taylor series approximation of *sine* and *cosine* respectively, and then obtain the mean of a_n by finding its first moment. This can be similarly done for b_n . As a result,

$$E[a_n] = A_n \sum_{m=1}^N \left\{ \alpha_m \kappa_s - \alpha_m \kappa_s \lambda^2 m (\sigma_f^2 + \sigma_r^2) - \beta_m \kappa_c \lambda^2 m \left(\sigma_f^2 + \sigma_r^2 \left(\frac{2m}{N} - 1 \right) \right) \right\} \quad (24)$$

$$E[b_n] = A_n \sum_{m=1}^N \left\{ \beta_m \kappa_s - \beta_m \kappa_s \lambda^2 m (\sigma_f^2 + \sigma_r^2) + \alpha_m \kappa_c \lambda^2 m \left(\sigma_f^2 + \sigma_r^2 \left(\frac{2m}{N} - 1 \right) \right) \right\}. \quad (25)$$

As also discussed in Appendix B, to find a_n variance, we determine $(E[a_n])^2$ and $E[a_n^2]$, and substitute them in (17) to get

$$\begin{aligned} \text{var}[a_n] = (A_n \lambda)^2 & \left\{ \kappa_c^2 (\sigma_f^2 + \sigma_r^2) \left(\sum_{m=1}^N m \alpha_m^2 + 2 \sum_{m=1}^{N-1} \left(m \alpha_m \sum_{i=m+1}^N \alpha_i \right) \right) \right. \\ & + \kappa_s^2 (\sigma_f^2 + \sigma_r^2) \left(\sum_{m=1}^N m \beta_m^2 + 2 \sum_{m=1}^{N-1} \left(m \beta_m \sum_{i=m+1}^N \beta_i \right) \right) \\ & - 2 \kappa_s \kappa_c \sum_{m=1}^N \alpha_m \left(\sum_{i=1}^m i \beta_i \left[\sigma_f^2 + \left(\frac{2m}{N} - 1 \right) \sigma_r^2 \right] \right. \\ & \left. \left. + m \sum_{i=m+1}^N \beta_i \left[\sigma_f^2 + \left(\frac{2i}{N} - 1 \right) \sigma_r^2 \right] \right) \right\}. \quad (26) \end{aligned}$$

Similarly for b_n coefficient, the variance is derived as

$$\begin{aligned} \text{var}[b_n] = (A_n \lambda)^2 & \left\{ \kappa_c^2 (\sigma_f^2 + \sigma_r^2) \left(\sum_{m=1}^N m \beta_m^2 + 2 \sum_{m=1}^{N-1} \left(m \beta_m \sum_{i=m+1}^N \beta_i \right) \right) \right. \\ & + \kappa_s^2 (\sigma_f^2 + \sigma_r^2) \left(\sum_{m=1}^N m \alpha_m^2 + 2 \sum_{m=1}^{N-1} \left(m \alpha_m \sum_{i=m+1}^N \alpha_i \right) \right) \\ & + 2 \kappa_s \kappa_c \sum_{m=1}^N \beta_m \left(\sum_{i=1}^m i \alpha_i \left[\sigma_f^2 + \left(\frac{2m}{N} - 1 \right) \sigma_r^2 \right] \right. \\ & \left. \left. + m \sum_{i=m+1}^N \alpha_i \left[\sigma_f^2 + \left(\frac{2i}{N} - 1 \right) \sigma_r^2 \right] \right) \right\}. \quad (27) \end{aligned}$$

The value of σ_{cof}^2 in (18) and (19) can be approximated by the averaged sum of (26) and (27) as

$$\begin{aligned} \sigma_{cof}^2 \approx \frac{\text{var}[a_n] + \text{var}[b_n]}{2} & = \left(\frac{2A_0}{T_{ref}} \right)^2 (\sigma_f^2 + \sigma_r^2) \\ & \times \left(\frac{N(N+1)}{4} + \sum_{m=1}^{N-1} m \left(\alpha_m \sum_{i=m+1}^N \alpha_i + \beta_m \sum_{i=m+1}^N \beta_i \right) \right). \quad (28) \end{aligned}$$

To verify the derived mean and variance expressions, we plot them as dashed lines in Fig. 7(a) and (b), respectively, and compare them with those corresponding values attained from MC of our analytical model (15). As can be observed, for small delay SDs, the derived expressions match the simulations. For large delay SDs, the accuracy degrades due to the low-order Taylor series which was utilized to approximate a_n and b_n . Nonetheless, higher order Taylor approximation which results in complex derivations would not be necessary, because as mentioned before, the large values of SDs are in fact avoided due to the stringent requirements on synthesizer's output spur levels.

B. Magnitude of Spur-to-Carrier Ratio (SCR)

As indicated previously by (15), the synthesizer SCR is the

Fig. 8. (a) Simulated mean and variance of the carrier and spur magnitudes (C and S_n) as a function of normalized delay SD, (b) simulated mean and variance of the carrier's Fourier coefficients a_N and b_N as a function of normalized delay SD, and (c) simulated and predicted synthesizer SCR for the spur at $f_s = f_c - f_{ref}$.

Fig. 9. Closed-form formula (33) vs. MC of (15) for synthesizer's mean SCR as a function of normalized DCD: (a) $T_{spe} = 0$, (b) $T_{spe} = 1$ ps, and (c) $T_{spe} = 2$ ps.

ratio distribution of Rayleigh random variable S_n over the random variable C , i.e. the magnitude of the fundamental tone. Fourier coefficients of C , i.e., a_N and b_N , are calculated from (11) and (13) respectively, for $n = N$. In order to characterize the ratio random variable SCR, we depict the mean and variance of S_n and C as functions of delay SD in Fig. 8(a). It can be observed that the mean of the fundamental tone $E[C]$, is much larger than its own variance $\text{var}[C]$, as well as the mean $E[S]$ and variance $\text{var}[S]$ of the numerator S_n . Therefore, we approximate the SCR distribution by replacing C with its mean, and modify (15) as

$$SCR_n = S_n / E[C]. \quad (29)$$

To find $E[C]$, we plot the carrier coefficients a_N and b_N in Fig. 8(b) and observe that the mean values $E[a_N]$ and $E[b_N]$, are much larger than the variances $\text{var}[a_N]$ and $\text{var}[b_N]$. So, we approximate $E[C]$ as

$$E[C] = E\left[\sqrt{a_N^2 + b_N^2}\right] \approx \sqrt{(E[a_N])^2 + (E[b_N])^2}. \quad (30)$$

Shown in Fig. 8(b), the approximated $E[C]$ closely matches its MC-simulated counterpart. For small delay SD values, (30) can be further simplified to

$$E[C] \approx \frac{2}{N\pi} \left| \frac{\sin(kN\pi/T_{ref}) \sin(T_{spe}N\pi/T_{ref})}{\sin(T_{spe}\pi/T_{ref})} \right|, \quad T_{spe} \neq 0 \quad (31)$$

Finally, as SCR is the ratio of Rayleigh variable S_n to a constant, we use linearity to approximate SCR also as a Rayleigh variable with PDF and mean of

$$p_X(x) = \begin{cases} (x/\sigma_R^2) \exp(-x^2/2\sigma_R^2) & x \geq 0 \\ 0 & x < 0 \end{cases} \quad (32)$$

$$E[SCR_n] = \sigma_R \sqrt{\pi/2} \quad (33)$$

where

$$\sigma_R = \sigma_{cof} / E[C]. \quad (34)$$

Logarithmic representation of the PDF in (32) is obtained by change of variables, resulting in Log-Rayleigh PDF [14] of

$$p_Y(y) = \left(10^{10} / \sigma_R^2 \right) \exp\left(-10^{10} / 2\sigma_R^2 \right). \quad (35)$$

To verify the analysis, the distribution of the synthesizer's SCR is illustrated in Fig. 8(c). The dashed curve shows the normalized closed-form SCR PDF of (35), and the bar chart is the SCR histogram obtained from MC of our analytical model.

C. Closed-Form Expression Accuracy

In this part we evaluate the accuracy of the proposed Rayleigh-approximated closed-form formula, for large variations in SPE, DCD, and delay SD. To do so, we consider four different normalized delay SD values of $\sigma/\mu = 0.2\%$, 0.8% , 1.4% , and 2% , as well as three SPE values of $T_{spe} = 0$, 1 , and 2 ps. Then we sweep DCD from $T_{dcd} = 0.1$ to 30 ps. Fig. 9 plots the calculated mean SCR values from the closed-form expression (33) and compares them with the MC-simulated SCR of the analytical model (15). Shown in Fig. 9(a), with a zero SPE, the simulation and prediction follow each other even at a large DCD of 30 ps. A small offset of less than a dB is observable for the large delay SD of $\sigma/\mu = 2\%$, which is in line with our discussion in the previous part, and disappears as the delay SD gets smaller. On the other hand, as the DCD and SPE values get much larger compared to the delay SD value, the accuracy gets degraded. Analysis of several simulations

Fig. 10. Flowchart of the proposed spur-aware design flow.

indicates that at large DCD and SPE values for which

$$\frac{T_{spe}}{\mu} \cdot \frac{T_{dcd}}{\mu} > \frac{\sigma}{\mu}, \quad (36)$$

the criteria of (16) which is required for Rayleigh approximation, would not satisfy anymore. However, for reasonable values of SPE, DCD, and delay SD in the context of frequency synthesis, the proposed closed-form expression can predict the SCR of the largest spurs, with an acceptable accuracy. Fig. 9(c) demonstrates that a less than 1 dB error in SCR estimation can be obtained even for a small delay SD of $\sigma/\mu = 0.2\%$, and with reasonable DCD and SPE values of $T_{dcd} = 10$ ps and $T_{spe} = 2$ ps, achievable in state-of-the-art CMOS implementations [2], [6], [15].

V. A SPUR-AWARE SYNTHESIZER DESIGN FLOW

Based on our analysis in Section IV which led to a close-form formula for the output SCR, we now propose a spur-aware DLL-based frequency synthesizer design flow. This methodology determines the required value of the stage-delay SD, at which a certain spurious performance (SCR) at synthesizer's output is achieved. Since the proposed design flow does not employ MC simulations, the overall iterative design process to find the required delay SD is accelerated. Prior to discussing the flow, we first derive an expression for the best SCR for a given delay SD, which is achieved when SPE and DCD are negligibly small. To do so, we first simplify the variance of the output spur Fourier coefficients ($n \neq N$) which is given in (26) and (27). For $T_{spe} \approx T_{dcd} \approx 0$, we have

$$\text{var}[a_n]_{\min} = \frac{N(\sigma_f^2 + \sigma_r^2) [2 - \cos(2n\pi/N)]}{2T_{ref}^2 \sin^2(n\pi/N)}, \quad n \neq N \quad (37)$$

$$\text{var}[b_n]_{\min} = \frac{N(\sigma_f^2 + \sigma_r^2) [2 + \cos(2n\pi/N)]}{2T_{ref}^2 \sin^2(n\pi/N)}, \quad n \neq N \quad (38)$$

$$\sigma_{cof, \min}^2 \approx \frac{\text{var}[a_n]_{\min} + \text{var}[b_n]_{\min}}{2} = \frac{N(\sigma_f^2 + \sigma_r^2)}{T_{ref}^2 \sin^2(n\pi/N)}, \quad n \neq N \quad (39)$$

Also for very small SPE and DCD values, the mean magnitude of the carrier ($n = N$) in (30) is simplified as

$$E[C] = \frac{2T_{ref}^2 - (N+1)N^2\pi^2(\sigma_f^2 + \sigma_r^2)}{\pi T_{ref}^2} \approx \frac{2}{\pi}. \quad (40)$$

Fig. 11. WiMedia-UWB frequency allocation and the coexisting standards.

Now, by substitution of (39) and (40) into (33) and (34), the lower bound on the achievable mean SCR is determined as

$$E[SCR_n] \geq \frac{\pi\sqrt{\pi}}{2\sqrt{2N} \sin(n\pi/N)} \times \frac{\sqrt{\sigma_f^2 + \sigma_r^2}}{\mu}. \quad (41)$$

The above expression indicates the best achievable spur suppression for a given delay mismatch and very small SPE and DCD values. Now, by knowing the spurious performance specification SCR_{spec} of the target standard, i.e. the maximum allowed spur-to-carrier level, we can reformulate (41) to find an upper bound on the normalized delay SD, as

$$\frac{\sqrt{\sigma_f^2 + \sigma_r^2}}{\mu} \leq SCR_{spec} \times \frac{2\sqrt{2N} |\sin(n\pi/N)|}{\pi\sqrt{\pi}}. \quad (42)$$

The proposed spur-aware methodology is illustrated in form of a flow chart in Fig. 10. First, from the specifications of the target wireless standard, which provides information such as the frequency bands, channel spacing, and switching time, we determine the design parameters including the reference clock frequency f_{ref} , and the number of delay stages N . Then from (42) we find the upper bound on the delay SD, SD_{max} , by which a given SCR_{spec} satisfies when SPE and DCD are sufficiently small. Afterwards, to consider the effect of non-zero SPE and DCD, we use the initially-calculated SD_{max} as well as the estimated achievable SPE and DCD values, to calculate σ_{cof} from (28), $E[C]$ from (31), and finally σ_R from (34). Now we can determine the provided mean SCR from (33). If it is larger than SCR_{spec} , then we improve our initial delay SD and calculate the new mean SCR, and repeat this procedure until $SCR \leq SCR_{spec}$. Based on the calculated value of the required delay SD, one can do the sizing of the delay stage transistors using a similar approach as in [12].

VI. WiMedia-UWB SYNTHESIZER; A CASE STUDY

In this section we employ the proposed design flow in Section V to find the required stage-delay SD for a DLL-based frequency synthesizer, which satisfies the spurious performance requirement of WiMedia-UWB bandgroup (BG) 1 standard [16].

A. Design Procedure

The spectrum allocation of the standard as well as the coexisting wireless technologies is illustrated in Fig. 11. The spur suppression requirement of WiMedia-UWB is calculated from the interferer scenario [17]. As can be seen in Fig. 11, because of the strong out-of-band interferers from IEEE 802.11 a/b/g, those spurious tones which fall within 2.4 to 5 GHz range, should maintain below -45 dBc [17], [18]. Note

testbench is performed using Spectre Cadence in a standard 65-nm CMOS process. To increase the simulator accuracy, we set the tolerance options as *relative tolerance* = 10^{-5} , *absolute voltage tolerance* = 10^{-8} , and *absolute current tolerance* = 10^{-13} . Also, in order to speed up the simulations, we enabled the accelerated parallel simulator (APS) and multithreading with 16 threads on 16 available processors. The bar chart in Fig. 14 show the transistor-level MC histogram of the WiMedia-UWB synthesizer's output SCR, for the reference harmonics at $f_s = f_c + f_{ref} = 9504$ MHz. The dashed line represents the normalized predicted PDF of the WiMedia-UWB synthesizer's SCR, using the proposed closed-form formula of Log-Rayleigh approximation (35). Note that among those simulation parameters listed in Fig. 14, the assumed SPE value of $T_{spe} = 2$ ps can be slightly different for the case of transistor-level MC simulation, as an open loop VCDL is utilized ($t_{avg}=0$). With the above configurations and settings, the measured simulation time regarding a single design iteration using 10^4 MC samples on the open-loop VCDL is about 16.7×10^4 s (16.7 s/sample). Note that the simulation time becomes even higher when utilizing a closed-loop DLL for simulation. By employing the proposed methodology on the other hand, the design iterations are performed on the closed-form expressions (Fig. 10), where no simulation is involved. It can be observed from Fig. 14 that the predicted SCR PDF regarding the largest out-of-band harmonic spur at DLL-based WiMedia-UWB synthesizer output spectrum follows the corresponding MC histogram. Also the required SCR_{spec} of -39 dBc is satisfied and the predicted and simulated mean SCR values are closely matched with less than 1 dB error. Considering the utilized values of DCD, SPE, and delay SD, this result is in line with the accuracy condition in (36).

VII. CONCLUSION

Fixed-pattern jitter in DLL-based edge-combing frequency synthesizers is generated due to phase misalignment of the DLL output edges. The resulting harmonic spurs down-convert the out-of-band interferes into the wanted channels, corrupting the desired signal. This paper proposes a comprehensive behavioral model for DLL-based frequency synthesizers which includes the effect of delay mismatch, SPE, and DCD on synthesizer spurious performance. From the proposed model and employing the Fourier series analysis of the DLL output edges, an analytical model is obtained which formulates the spur-to-carrier ratio SCR, at synthesizer's output. The analytical expression is further developed by employing statistical methods, to derive a close-form expression for the harmonic SCR. Based on our closed-form derivations, a spur-aware design flow is introduced which determines the required stage-delay SD for a given SCR performance without using MC simulations, which speeds up the overall iterative design procedure. As an experimental case, the proposed design methodology is utilized to calculate the stage-delay SD of a DLL-based synthesizer, at which the SCR of WiMedia-UWB standard is satisfied. Based on the calculated delay SD, the

delay stage is then designed in a standard 65-nm CMOS process. Transistor-level MC simulation regarding the synthesizer's spurious performance demonstrates good compliance with behavioral model and analytical predictions.

APPENDIX A

The Fourier series of the m^{th} DLL output phase (neglecting the DC component) is expressed as

$$\Phi_m(t) = \sum_{n=1}^{\infty} a_{n,\Phi_m} \cos(n\omega_{ref}t) + \sum_{n=1}^{\infty} b_{n,\Phi_m} \sin(n\omega_{ref}t). \quad (48)$$

From the waveform representation of Fig. 2, the Fourier coefficients a_{n,Φ_m} and b_{n,Φ_m} in (48) are expressed as

$$a_{n,\Phi_m} = \frac{2A_0}{T_{ref}} \int_{m\mu + \sum_{i=1}^m G_i - m t_{avg}}^{k+m\mu + \sum_{i=1}^m G_i - m t_{avg}} \cos(n\omega_{ref}t) dt \quad (49)$$

$$b_{n,\Phi_m} = \frac{2A_0}{T_{ref}} \int_{m\mu + \sum_{i=1}^m G_i - m t_{avg}}^{k+m\mu + \sum_{i=1}^m G_i - m t_{avg}} \sin(n\omega_{ref}t) dt. \quad (50)$$

Since the EC output is constructed by summation of the multiphase DLL signals, its Fourier series can be written as

$$\begin{aligned} \Phi_{out}(t) &= \sum_{m=1}^N \Phi_m(t) \\ &= \sum_{m=1}^N \sum_{n=1}^{\infty} a_{n,\Phi_m} \cos(n\omega_{ref}t) + \sum_{m=1}^N \sum_{n=1}^{\infty} b_{n,\Phi_m} \sin(n\omega_{ref}t) \\ &= \sum_{n=1}^{\infty} \left(\cos(n\omega_{ref}t) \sum_{m=1}^N a_{n,\Phi_m} \right) + \sum_{n=1}^{\infty} \left(\sin(n\omega_{ref}t) \sum_{m=1}^N b_{n,\Phi_m} \right). \end{aligned} \quad (51)$$

Implied by linearity in (51), Fourier coefficients of the EC output are the sum of Fourier coefficients of the DLL phases,

$$a_n = \sum_{m=1}^N a_{n,\Phi_m}, \quad b_n = \sum_{m=1}^N b_{n,\Phi_m}. \quad (52)$$

APPENDIX B

Applying Taylor series approximation to (20), we get

$$\begin{aligned} a_n &= A_n \sum_{m=1}^N \left[\alpha_m \kappa_s - \alpha_m \kappa_s \lambda^2 (X_{fm}^2 + X_{rm}^2) + \alpha_m \kappa_c \lambda (X_{fm} - X_{rm}) \right. \\ &\quad \left. - \beta_m \kappa_s \lambda (X_{fm} + X_{rm}) - \beta_m \kappa_c \lambda^2 (X_{fm}^2 - X_{rm}^2) \right]. \end{aligned} \quad (53)$$

The mean of a_n is derived from its first moment as

$$\begin{aligned} E[a_n] &= A_n \sum_{m=1}^N \left(\alpha_m \kappa_s - \alpha_m \kappa_s \lambda^2 E[X_{fm}^2 + X_{rm}^2] \right. \\ &\quad \left. + \alpha_m \kappa_c \lambda E[X_{fm} - X_{rm}] - \beta_m \kappa_s \lambda E[X_{fm} + X_{rm}] \right. \\ &\quad \left. - \beta_m \kappa_c \lambda^2 E[X_{fm}^2 - X_{rm}^2] \right). \end{aligned} \quad (54)$$

To calculate $E[a_n]$, we first utilize (12) to write

$$E[X_{rm}] = E[X_{rm}] = 0 \quad (55)$$

$$E[X_{rm}^2] = m(1 - \frac{m}{N})\sigma_r^2, \quad E[X_{fm}^2] = m(\sigma_f^2 + \frac{m}{N}\sigma_r^2). \quad (56)$$

Then from linearity, we calculate the required expectations as

$$E[X_{fm} - X_{rm}] = E[X_{fm} + X_{rm}] = 0 \quad (57)$$

$$E[X_{fm}^2 + X_{rm}^2] = m(\sigma_f^2 + \sigma_r^2) \quad (58)$$

$$E[X_{fm}^2 - X_{rm}^2] = m\left(\sigma_f^2 + \sigma_r^2\left(\frac{2m}{N} - 1\right)\right). \quad (59)$$

To obtain a_n variance, $(E[a_n])^2$ and $E[a_n^2]$ are required. The former is determined from (54). The latter is derived by calculating a_n^2 from (53), and then applying the expectation. Substituting the resulting approximated expressions into (17),

$$\text{var}[a_n] \approx A_n^2 \lambda^2 \left\{ \kappa_c^2 A + \kappa_s^2 B - 2\kappa_s \kappa_c C \right\} \quad (60)$$

where

$$A = E \left[\left(\sum_{m=1}^N \alpha_m (X_{fm} - X_{rm}) \right)^2 \right] = (\sigma_f^2 + \sigma_r^2) \times \left(\sum_{m=1}^N m \alpha_m^2 + 2 \sum_{m=1}^{N-1} \left(m \alpha_m \sum_{i=m+1}^N \alpha_i \right) \right) \quad (61)$$

$$B = E \left[\left(\sum_{m=1}^N \beta_m (X_{fm} + X_{rm}) \right)^2 \right] = (\sigma_f^2 + \sigma_r^2) \times \left(\sum_{m=1}^N m \beta_m^2 + 2 \sum_{m=1}^{N-1} \left(m \beta_m \sum_{i=m+1}^N \beta_i \right) \right) \quad (62)$$

$$C = E \left[\sum_{m=1}^N \alpha_m (X_{fm} - X_{rm}) \sum_{m=1}^N \beta_m (X_{fm} + X_{rm}) \right] = \sum_{m=1}^N \alpha_m \left(\sum_{i=1}^m i \beta_i \left[\sigma_f^2 + \left(\frac{2m}{N} - 1 \right) \sigma_r^2 \right] + m \sum_{i=m+1}^N \beta_i \left[\sigma_f^2 + \left(\frac{2i}{N} - 1 \right) \sigma_r^2 \right] \right) \quad (63)$$

REFERENCES

- [1] G. Chien and P. R. Gray, "A 900-MHz Local Oscillator using a DLL-Based Frequency Multiplier Technique for PCS Applications," *IEEE J. Solid State Circuits*, vol. 35, no. 12, pp. 1996–1999, Dec. 2000.
- [2] J. Zhuang, Q. Du, and T. Kwasniewski, "A -107 dBc 10 kHz carrier offset 2-GHz DLL-based frequency synthesizer," *Proc. IEEE Custom Integr. Circuits Conf.*, pp. 301–304, Sep. 2003.
- [3] T. C. Lee and K. J. Hsiao, "A DLL-based frequency multiplier for MBOA-UWB system," *Proc. Symp. VLSI Circuits Dig. Tech. Papers*, pp. 42–45, Jun. 2005.
- [4] T. C. Lee and K. J. Hsiao, "The Design and Analysis of a DLL-Based Frequency Synthesizer for UWB Application," *IEEE J. Solid State Circuits*, vol. 41, no. 6, pp. 1245–1252, Jun. 2006.
- [5] S. Gierkink, "An 800 MHz -122 dBc/Hz-at-200 kHz clock multiplier based on a combination of PLL and recirculating DLL," *Proc. IEEE Int. Solid-State Circuits Conf.*, pp. 454–455, Feb. 2008.
- [6] P. C. Maulik and D. A. Mercer, "A DLL-based programmable clock multiplier in 0.18μm CMOS with -70 dBc reference spur," *IEEE J. Solid-State Circuits*, vol. 42, no. 8, pp. 1642–1648, Aug. 2007.
- [7] N. Khan, M. Hossain, K.L.E. Law, "A Low Power Frequency Synthesizer for 60-GHz Wireless Personal Area Networks," *IEEE Trans. Circuits Syst. II: Exp. Briefs*, vol. 58, no. 10, pp. 622–626, Oct. 2011.
- [8] H. J. Ng *et al.*, "A DLL-Supported, Low Phase Noise Fractional-N PLL with a Wideband VCO and a Highly Linear Frequency Ramp Generator for FMCW Radars," *IEEE Trans. Circuits Syst. I: Reg. Papers*, vol. 60, no. 12, pp. 3289–3302, Dec. 2013.
- [9] A. Elshazly *et al.*, "A 1.5GHz 890uW Digital MDLL with 400fsrms Integrated Jitter, -55.6dBc Reference Spur and 20fs/mV Supply-Noise Sensitivity Using 1b TDC," *Proc. IEEE Int. Solid-State Circuits Conf., Dig. Tech. Papers*, pp. 242–244, Feb. 2012.
- [10] M. J. M. Pelgrom, A. C. J. Duinmaijer, and A. P. G. Welbers, "Matching properties of MOS transistors," *IEEE J. Solid-State Circuits*, vol. 24, no. 10, pp. 1433–1440, Oct. 1989.
- [11] J. Zhuang, Q. Du and T. Kwasniewski, "Noise, spur characteristics and in-lock error reduction of DLL-based frequency synthesizers," *Proc. Int. Conf. Commun., Circuits Syst.*, pp. 1443–1446, Jun. 2004.
- [12] O. Casha *et al.*, "Analysis of the Spur Characteristics of Edge-Combining DLL-Based Frequency Multipliers," *IEEE Trans. Circuits Syst. II: Exp. Briefs*, vol. 56, no. 2, pp. 132–136, Feb. 2009.
- [13] J.G. Proakis, and M. Salehi, *Digital Communications, 5th Edition*, McGraw Hill, 2008.
- [14] B. Rivet, L. Girin and C. Jutten, "Log-Rayleigh Distribution: A Simple and Efficient Statistical Representation of Log-Spectral Coefficients," *IEEE Trans. Audio, Speech, Lang. Process.*, vol. 15, no. 3, pp. 796–802, Mar. 2007.
- [15] T. Ali, *et al.*, "A 4.6GHz MDLL with -46dBc reference spur and aperture position tuning," *Proc. IEEE Int. Solid-State Circuits Conf. Dig. Tech. Papers*, pp. 466–467, 2011.
- [16] *High rate Ultra Wideband PHY and MAC Standard*, ECMA-368. 3rd Edition, Dec. 2008 [Online].
- [17] K. Iniewski, *Wireless Technologies: Circuits, Systems, and Devices*. New York: CRC Press, 2007.
- [18] M. M. Izad and C. Hng "A Pulse Shaping Technique for Spur Suppression in Injection-Locked Synthesizers," *IEEE J. Solid State Circuits*, vol. 47, no. 3, pp. 652–664, Mar. 2012.
- [19] A. Ojani, B. Mesgarzadeh, and A. Alvandpour, "A DLL-Based Injection-Locked Frequency Synthesizer for WiMedia UWB," *Proc. IEEE Int. Symposium Circuits Syst.*, pp. 2027–2030, May 2012.

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