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Monte Carlo-Free Prediction of Spurious Performance for ECDLL-Based Synthesizers

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Abstract—Misalignment of delay-locked loop (DLL) output edges creates an undesired periodicity, resulting in reference harmonic tones at the output spectrum of edge-combining DLL (ECDLL)-based frequency synthesizers. These spurious tones corrupt the spectral purity to an unacceptable level for wireless applications. The spur magnitude is a random variable defined by the reference frequency, number of DLL phases, harmonic order, stage-delay standard deviation (SD), duty cycle distortion (DCD) of the reference clock, and static phase error (SPE) of the locked-loop due to charge pump/phase detector imperfections. Hence, to estimate the spurious performance of such synthesizers, exhaustive Monte Carlo (MC) simulations are inevitable. Based on closed-form expressions, this paper proposes a generic predictive model for harmonic spur characterization of ECDLL-based frequency synthesizers, whose prediction accuracy is independent of synthesizer design parameters and system non-idealities. Therefore, it can replace MC method to significantly accelerate the iterative design procedure of the synthesizer, while providing comparable predictions in terms of robustness and accuracy to that of MC. Validity, accuracy, and robustness of the proposed prediction method against wide-range values of non-idealities are verified through MC simulations of both the behavioral model and transistor-level model of the synthesizer in a standard 65-nm CMOS technology.

Index Terms—delay mismatch, DLL, duty cycle distortion, frequency synthesizer, harmonic spur, Monte Carlo, periodic jitter, predictive model, static phase error

I. INTRODUCTION

SPECTRAL purity is a key requirement for frequency generation schemes in wireless applications. In integer locked-loop-based frequency synthesis, where the system is locked to a low-frequency reference clock, non-idealities of the system can produce an erroneous periodicity, known as periodic jitter, resulting in appearance of reference harmonic tones at the spectrum of the synthesized carrier. These harmonic spurs can potentially downconvert out-of-band interferers into the desired band, corrupting the wanted signal. Delay-locked loop (DLL)-based frequency synthesis achieves low close-in phase noise by taking advantage of the low-accumulative-jitter property of DLLs, which is obtained by periodically resetting the jitter back to zero, and consists of two main approaches. In recirculating DLL-based approach [1]–[7] where the multiplied clock is generated by a similar mechanism as in ring voltage-controlled-oscillator (VCO)-based phase-locked loops (PLL), the harmonic spur-to-carrier ratio (SCR) is directly defined by the output frequency and static phase error (SPE) of the locked-loop [5], [7]. Edge-combining DLL (ECDLL)-based synthesizers [8]–[16], on the

other hand, are more prone to generation of spurious tones. As the carrier is produced by combining the equally-spaced DLL output edges, any sort of non-ideality, including SPE, duty cycle distortion (DCD), and stage-delay mismatch (as a stochastic variable), will cause misalignment in those edges, degrading the spurious performance. Consequently, the SCR in ECDLLs becomes a random variable which is defined by the design parameters, i.e., the reference frequency and number of DLL phases, as well as the system non-idealities, i.e., SPE, DCD, and stage-delay standard deviation (SD) [16]. As a result, spur characterization of ECDLL-based synthesizers requires exhaustive transient Monte Carlo (MC) simulations which significantly slow down their design procedure.

Among those prior arts [10], [12], [13], [16] which study the spurious characteristics of ECDLL synthesizers, a comprehensive behavioral model is proposed in [16] which includes all the aforementioned sources of harmonic spurs in such synthesizers, and provides an analysis which leads to derivation of a closed-form approximation for synthesizer SCR. However, there are two limitations regarding the approximation in [16]. First, the prediction accuracy is guaranteed only for some bounded values of SPE, DCD, and delay SD, and will degrade otherwise. Second, due to dependency of the prediction error upon the synthesizer design parameters and system non-idealities, it is challenging to define and formulate generic accuracy bounds of the model, without performing case-specific MC simulations for a given design scenario. These limitations indicate the necessity and importance of developing a more generic and accurate predictive model, which provides predictions that are as robust as those achieved using statistical simulations, and hence, can be employed as a general replacement to MC method.

In this work, the main objective is to mitigate those major limitations of the approximation model in [16], by developing generic and robust predictions which can thoroughly replace exhaustive MC method for spur characterization of ECDLL synthesizers. In order to do so, the paper first investigates the behavior of even- and odd-order harmonic spurs at the output spectrum of such synthesizers, and demonstrates that depending on the relations among SPE, DCD, and delay SD values, either of those harmonics can have the largest spur level. This implies that the SCR needs to be accurately characterized and predicted for both the adjacent and alternate harmonics to the carrier. Afterwards, the limitations regarding the approximation model in [16] are elaborated, emphasizing the need for more accurate predictions. Accordingly, based on closed-form expressions, the paper proposes a generic predictive model for ECDLL synthesizers, whose accuracy in

Fig. 3. MC simulation of the analytical mean SCR of (9) for the adjacent ($n = N - 1, f_s = f_c - f_{ref}$) and alternate ($n = N - 2, f_s = f_c - 2f_{ref}$) harmonics as a function of normalized DCD and SPE, using normalized delay SD of (a) 2% and (b) 0.2%.

spur analysis of both the adjacent and alternate harmonics. Note that because in the utilized ECDLL model presented in the previous section, N is assumed to be odd, the adjacent harmonics with $n = N \pm 1$ are of even orders.

For the presented analysis throughout the paper, an ECDLL synthesizer is utilized that is locked to a reference clock of $f_{ref} = 400$ MHz and employs a VCDL with $N = 25$ stages, producing a carrier frequency of $f_c = 10$ GHz. Furthermore, DCD and SPE values are swept from $T_{dcd} = 1$ to 30 ps and $T_{spe} = 0.1$ to 5 ps, respectively. In addition, by choosing two normalized delay SD values of $\sigma_r/\mu_r = \sigma_f/\mu_f = \sigma/\mu = 0.2\%$ and 2%, the synthesizer SCR is simulated for the adjacent ($f_s = f_c - f_{ref}$) and alternate ($f_s = f_c - 2f_{ref}$) harmonics. Thus, four different test scenarios are investigated. Note that the values of non-idealities are selected in such a way that realistic corner cases regarding ECDLL synthesizer implementations are covered.

MC simulations of the analytical model of the synthesizer given in (9) are performed in MATLAB and the mean SCR results are plotted in Fig. 3. The X and Y axes correspond to the normalized SPE and DCD values, respectively. It can be observed from Fig. 3(a) that with a large delay SD of 2% and within the utilized sweep range for SPE and DCD, the SCR of the adjacent harmonic always dominates that of the alternate one. However, it is not the case if smaller values of delay SD are utilized to achieve lower SCR which is required for wireless applications. As shown in Fig. 3(b), for a delay SD of 0.2% (an order of magnitude smaller than the previous case), as SPE increases, the SCR of the alternate harmonic can dominate. This observation indicates that there are dissimilar spurious characteristics for the even- and odd-order harmonics. However, as illustrated in Fig. 3(a), this different behavior is not revealed if SPE and DCD values are absorbed by a large stage-delay mismatch. From Fig. 3(b) it can be perceived that the mean SCR of the adjacent harmonic depends upon both the SPE and DCD values. On the other hand, for the alternate harmonic, the mean SCR is mainly defined by SPE value, and degrades significantly as SPE grows, regardless of DCD value. This behavior can be explained by evaluating the phase misalignment patterns on the transient waveform of the ECDLL output. Each non-ideality parameter (SPE, DCD, or delay SD) generates a unique pattern which results in certain

harmonic behavior.

Distinctive characteristics of adjacent and alternate harmonic spurs in ECDLL synthesizers imply that to ensure a certain spurious performance, the SCR of both the harmonic spurs needs to be maintained below the required value. As a consequence, a generic predictive model should be able to accurately estimate SCR, not only for wide-range values of non-idealities, but also for both even and odd harmonic orders.

IV. LIMITATIONS OF THE APPROXIMATE MODEL

The limitations regarding the approximation model of [16] are addressed in this section by evaluating its accuracy in SCR estimation in four different test scenarios, similar to those of the previous section. Demonstrating that the model can accurately predict the spurious performance only when the SPE and DCD values are sufficiently absorbed by the value of the delay SD, its limitations for being employed as a general replacement to MC method for spur characterization of ECDLL-based synthesizers are clarified.

Assuming that the harmonic Fourier coefficients a_n and b_n of the synthesizer output, expressed by (7) and (8) respectively, are two independently and identically distributed (iid) random variables, they are approximated in [16] as two zero-mean Gaussian variables with equal variances, i.e.,

$$a_n \sim N(0, \sigma_{cof}^2), \quad b_n \sim N(0, \sigma_{cof}^2), \quad n \neq N \quad (10)$$

and hence, the spur magnitude $S_n = \sqrt{a_n^2 + b_n^2}$ is modeled as a Rayleigh random variable [19], whose mean value is

$$\mu_{S_n} = \sigma_{cof} \sqrt{\pi/2} \quad (11)$$

To examine the model accuracy, the simulated and predicted mean SCR values, from the analytical model (9) and the closed-form approximation model of [16], are compared over wide-range values of SPE and DCD. The results are plotted in Fig. 4 and 5 respectively, for a large and small normalized delay SD of 2% and 0.2%. The transparent planes correspond to the MC-simulated SCR and the solid planes depict the predicted results. When delay SD is 2%, the prediction follows the simulation quite closely for both the adjacent and alternate harmonic spurs shown in Fig. 4(a) and 4(b) respectively. Therefore, for the first two scenarios, a quite acceptable accuracy is provided. However, the achieved mean SCR values

Fig. 4. MC simulation of the analytical model (9) versus the approximate prediction model of [16] for mean SCR values as a function of normalized SPE and DCD, using normalized delay SD of 2%: (a) the adjacent, and (b) the alternate harmonic.

Fig. 5. MC simulation of the analytical model (9) versus the approximate prediction model of [16] for mean SCR values as a function of normalized SPE and DCD, using normalized delay SD of 0.2%: (a) the adjacent, and (b) the alternate harmonic.

Fig. 6. MC simulation of the analytical model (9) versus the prediction model of [16] for mean SCR values as a function of normalized delay SD.

(~ -20 dBc) using the delay SD of 2% is not adequate for wireless applications. Hence, similar evaluations for the next two scenarios are repeated using a more practical delay SD of 0.2% and the results are plotted in Fig. 5. It can be observed that the accuracy of the prediction is largely degraded for both the adjacent and alternate harmonics, though with different error characteristics. As shown in Fig. 5(a), the prediction accuracy for the adjacent harmonic spur depends on both the SPE and DCD values, whereas for the alternate harmonic illustrated in Fig. 5(b), the accuracy is mainly dependent on the value of SPE. As it can be seen from Fig. 5, for a very

small non-ideality pair of $T_{spe} = 1$ ps ($T_{spe}/\mu = 10^{-2}$) and $T_{dcd} = 10$ ps ($T_{dcd}/\mu = 10^{-1}$, duty cycle = 49.6%), the prediction error is 0 and 3 dB, for the adjacent and alternate harmonics, respectively. However, since the adjacent spur is larger than the alternate one in this case, the corresponding 3-dB error is not important. On the other hand, for a larger non-ideality pair of $T_{spe} = 5$ ps and $T_{dcd} = 10$ ps, the situation is quite different. The prediction error becomes as high as 5 dB and 15 dB for the adjacent and alternate spurs, respectively. Also, in contrast to the previous test case, the alternate spur is larger than the adjacent one. Note that these errors will be magnified if the delay SD is further reduced. This can be noticed from Fig. 6 which illustrates the mean SCR of the adjacent harmonic with respect to normalized delay SD and for a constant SPE-DCD pair of (5ps, 10ps). The MC simulation results represented by the solid line shows that for small delay SDs the mean SCR is mainly defined by SPE and DCD and not improved by further decreasing the delay SD. However, the prediction results of the model [16] (dashed line) cannot follow that of the MC.

Besides its conditional accuracy, there is another limiting factor concerning this model. It can be concluded by comparing Fig. 4 and 5 that the accuracy conditions are defined by the relations among the values of delay SD, SPE, and DCD. This makes it complicated to define those conditions and bounds in such a generic form which can be utilized for every design scenario without needing to perform

Fig. 7. SCR random variable identification: MC histogram of the analytical model (9), using a delay SD of 0.2% and different (T_{spe}, T_{dcd}) pairs: (a) the adjacent, and (b) the alternate harmonic.

case-specific simulations. This indicates that it is of great importance to develop a more generic predictive model for SCR estimation in ECDLL synthesizers, whose accuracy is independent from the design parameters and non-idealities.

V. A GENERIC PREDICTIVE MODEL

Different approaches can be employed to find the probability density function (PDF) of the SCR random variable defined in (9). An exact solution would be to derive the PDF of Fourier coefficients directly from the random non-idealities and then, by transformation of the resulting PDFs into their root sum square, calculate the PDF of SCR. By solving (7) and (8), and applying Taylor series approximation, expressions for a_n and b_n are derived as

$$a_n = \frac{2A_0}{n\pi} \sum_{m=1}^N \left\{ \alpha_m \kappa_s - \alpha_m \kappa_s \lambda^2 (X_{fm}^2 + X_{rm}^2) + \alpha_m \kappa_c \lambda (X_{fm} - X_{rm}) - \beta_m \kappa_s \lambda (X_{fm} + X_{rm}) - \beta_m \kappa_c \lambda^2 (X_{fm}^2 - X_{rm}^2) \right\} \quad (12)$$

$$b_n = \frac{2A_0}{n\pi} \sum_{m=1}^N \left\{ \beta_m \kappa_s - \beta_m \kappa_s \lambda^2 (X_{fm}^2 + X_{rm}^2) + \beta_m \kappa_c \lambda (X_{fm} - X_{rm}) + \alpha_m \kappa_s \lambda (X_{fm} + X_{rm}) + \alpha_m \kappa_c \lambda^2 (X_{fm}^2 - X_{rm}^2) \right\} \quad (13)$$

where

$$X_{fm} = -\frac{m}{N} \sum_{i=1}^N G_{ri} + \sum_{i=1}^m G_{fi}, \quad X_{rm} = -\frac{m}{N} \sum_{i=1}^N G_{ri} + \sum_{i=1}^m G_{ri}. \quad (14)$$

$$\lambda = \frac{n\pi}{T_{ref}}, \quad \kappa_s = \sin \frac{kn\pi}{T_{ref}}, \quad \text{and} \quad \kappa_c = \cos \frac{kn\pi}{T_{ref}} \quad (15)$$

$$\alpha_m = \cos \left(\frac{n\pi}{T_{ref}} \left[\frac{2m}{N} (T_{ref} + T_{spe}) + \frac{T_{ref}}{2} - T_{dcd} \right] \right) \quad (16)$$

$$\beta_m = \sin \left(\frac{n\pi}{T_{ref}} \left[\frac{2m}{N} (T_{ref} + T_{spe}) + \frac{T_{ref}}{2} - T_{dcd} \right] \right). \quad (17)$$

Deriving PDFs of a_n and b_n requires calculation of PDFs for the elements of (12) and (13), which are in form of time series and would result in complex analysis. In order to avoid dealing with complicated derivations involved in the direct PDF transformation method, another approach is employed in this work. The idea is to associate the SCR random variable to a well-known distribution so as to efficiently characterize the mean and PDF of the synthesizer SCR, based on the properties of that recognized distribution. In order to do so, an

observation is made on different MC histograms of the SCR first. Then, the criteria regarding the identified distribution are inspected for the output Fourier coefficients of the synthesizer, and finally, the model parameters are determined from (12) and (13), using moments methods.

A. Random Variable Identification

To identify the distribution regarding the magnitudes of the harmonic spurs, MC simulations are performed on synthesizer's analytical model of (9), and the resulting SCR histograms are plotted in Fig. 7. For this purpose, a small (and more practical) delay SD of 0.2% is utilized to better observe the effect of SPE and DCD. Also, five different pairs of (T_{spe}, T_{dcd}) are employed for the simulations, i.e., A = (0, 0), B = (1ps, 10ps), C = (2.5ps, 10ps), D = (5ps, 10ps), and E = (5ps, 20ps). By evaluating the plotted distributions in Fig. 7, it can be noted that the SCR exhibits the distribution of Rayleigh random variables for smaller SPE-DCD values, i.e., A and B pairs. Moving towards the largest input pair E, the distribution demonstrates a smooth transition from Rayleigh to Gaussian form. The observed behavior in the simulated distributions is in fact similar to that of Ricean random variables [19]. From the definition of such variables, the spur magnitude $S_n = \sqrt{a_n^2 + b_n^2}$ will have a Ricean distribution if the harmonic Fourier coefficients a_n and b_n represented by (7) and (8), are two normal random variables with equal variances which are expressed as

$$a_n \sim N(\mu_{a_n}, \sigma_{cof}^2), \quad b_n \sim N(\mu_{b_n}, \sigma_{cof}^2) \quad n \neq N \quad (18)$$

where μ_{an} and μ_{bn} are the mean values of a_n and b_n respectively, and σ_{cof}^2 is their variance. Equation (18) should now be investigated by evaluating the variance and mean of the harmonic Fourier coefficients. The variances of a_n and b_n are plotted in Fig. 8(a) for the adjacent harmonic spurs as a function of SPE and DCD values. It can be observed that a_n and b_n variances maintain within a small range and almost close to each other, with a worst-case difference of around 2.5×10^{-5} . Fig. 8(b) shows that the mean values of a_n and b_n are zero for sufficiently small SPE and DCD values. However, for greater values of SPE and DCD, the mean values tend to deviate largely from zero, dissatisfying criteria (10). This, in fact, explains why for non-small SPE and DCD values, the harmonic spur levels cannot be predicted accurately with the approximation model of [16]. Note that the normality

Fig. 8. MC simulation regarding (a) the variance, and (b) the mean of the adjacent harmonic Fourier coefficients ($n = N - 1$) as a function of normalized SPE and DCD, using normalized delay SD of 0.2%.

condition of a_n and b_n in (18) can be verified using graphical tests [16]. Therefore, the harmonic spur magnitudes S_n are modeled as Ricean random variables, with the following PDF and mean expressions [19].

$$p_Z(z) = \frac{z}{\sigma_{cof}^2} \exp\left(-\frac{z^2 + h^2}{2\sigma_{cof}^2}\right) I_0\left(\frac{hz}{\sigma_{cof}^2}\right) \quad z \geq 0 \quad (19)$$

$$E[S_n] = \sigma_{cof} \sqrt{\frac{\pi}{2}} \times e^{\frac{-K}{2}} \times \left[(1+K) I_0\left(\frac{K}{2}\right) + K I_1\left(\frac{K}{2}\right) \right] \quad (20)$$

where h is the magnitude of the vector (μ_{an}, μ_{bn}) , i.e.,

$$h = \sqrt{\mu_{an}^2 + \mu_{bn}^2} \quad (21)$$

and K is the *Rice factor* which is defined as

$$K = h^2 / 2\sigma_{cof}^2. \quad (22)$$

Also, $I_0(x)$ and $I_1(x)$ are the *modified Bessel functions* of the first kind with order zero and one, respectively, and defined as

$$I_0(x) = \frac{1}{\pi} \int_0^\pi e^{x \cos \theta} d\theta \quad (23)$$

$$I_1(x) = \frac{1}{\pi} \int_0^\pi e^{x \cos \theta} \cos(\theta) d\theta. \quad (24)$$

B. Determining Model Parameters

After identifying the harmonic spur magnitudes in ECDLL synthesizers as Ricean random variables, the mean and PDF of S_n in (19) and (20), need to be determined by calculating the values of h and σ_{cof} . Finding the first and second moments of (12) and (13), the mean and variance of a_n and b_n are determined [16] as

$$\mu_{a_n} = E[a_n] = \frac{2A_0}{n\pi} \sum_{m=1}^N \left\{ \alpha_m \kappa_s - \alpha_m \kappa_s \lambda^2 m (\sigma_f^2 + \sigma_r^2) - \beta_m \kappa_c \lambda^2 m \left(\sigma_f^2 + \sigma_r^2 \left(\frac{2m}{N} - 1 \right) \right) \right\} \quad (25)$$

$$\mu_{b_n} = E[b_n] = \frac{2A_0}{n\pi} \sum_{m=1}^N \left\{ \beta_m \kappa_s - \beta_m \kappa_s \lambda^2 m (\sigma_f^2 + \sigma_r^2) + \alpha_m \kappa_c \lambda^2 m \left(\sigma_f^2 + \sigma_r^2 \left(\frac{2m}{N} - 1 \right) \right) \right\} \quad (26)$$

$$\sigma_{cof}^2 \approx \frac{\text{var}[a_n] + \text{var}[b_n]}{2} = \left(\frac{2A_0}{T_{ref}} \right)^2 (\sigma_f^2 + \sigma_r^2) \times \left(\frac{N(N+1)}{4} + \sum_{m=1}^{N-1} m \left(\alpha_m \sum_{i=m+1}^N \alpha_i + \beta_m \sum_{i=m+1}^N \beta_i \right) \right) \quad (27)$$

The value of h can be found by substitution of the numerical values of (25) and (26) into (21).

Now, knowing the Ricean random variable S_n , the ratio random variable SCR_n defined in (9) should be determined. As discussed in [16], it can be shown that the random variable C which represents the carrier magnitude, can be approximated by its mean value $E[C]$, and hence, (9) is simplified to $SCR_n = S_n/E[C]$. This implies that the harmonic Fourier coefficients of S_n , i.e., a_n and b_n , are divided by a constant to form the Fourier coefficients of SCR_n as

$$a'_n \sim N(\mu'_{a_n}, \sigma'^2_{cof}), \quad b'_n \sim N(\mu'_{b_n}, \sigma'^2_{cof}) \quad n \neq N \quad (28)$$

where from linearity,

$$\mu'_{a_n} = \mu_{a_n}/E[C], \quad \mu'_{b_n} = \mu_{b_n}/E[C], \quad \sigma'^2_{cof} = \sigma_{cof}^2/E[C]^2 \quad (29)$$

For small delay SD values, $E[C]$ is simplified [16] to

$$E[C] \approx \frac{2}{N\pi} \left| \frac{\sin(kN\pi/T_{ref}) \sin(T_{spe}N\pi/T_{ref})}{\sin(T_{spe}\pi/T_{ref})} \right| \quad T_{spe} \neq 0 \quad (30)$$

Therefore, it is concluded that SCR_n is also a Ricean random variable with a PDF and mean defined in closed-form as

$$p_Z(z) = \frac{z}{\sigma'^2_{cof}} \exp\left(-\frac{z^2 + h'^2}{2\sigma'^2_{cof}}\right) I_0\left(\frac{h'z}{\sigma'^2_{cof}}\right) \quad z \geq 0 \quad (31)$$

$$E[SCR_n] = \sigma'_{cof} \sqrt{\frac{\pi}{2}} \times e^{\frac{-K'}{2}} \times \left[(1+K') I_0\left(\frac{K'}{2}\right) + K' I_1\left(\frac{K'}{2}\right) \right] \quad (32)$$

where

$$h' = \sqrt{\mu'^2_{a_n} + \mu'^2_{b_n}} = h/E[C] \quad (33)$$

$$K' = h'^2 / 2\sigma'^2_{cof} = h^2 / 2\sigma_{cof}^2 = K \quad (34)$$

VI. VALIDATION OF THE PREDICTIVE MODEL

This section evaluates the accuracy and robustness of the proposed prediction method of spur characterization of ECDLL-based synthesizers, over wide-range values of the system non-idealities. In order to do so, the predicted mean

Fig. 9. MC simulation of the analytical model (9) versus the proposed predictive model (32) for mean SCR values as a function of normalized SPE and DCD, using normalized delay SD of 2%: (a) the adjacent, and (b) the alternate harmonic.

Fig. 10. MC simulation of the analytical model (9) versus the proposed predictive model (32) for mean SCR values as a function of normalized SPE and DCD, using normalized delay SD of 0.2%: (a) the adjacent, and (b) the alternate harmonic.

Fig. 11. MC simulation of the analytical model (9) versus the proposed predictive model for mean SCR values as a function of normalized delay SD.

SCR using the proposed model is compared with that of attained from the MC simulations of the analytical model (9). Furthermore, the accuracy of the proposed model is verified through MC simulations of the SCR for three different test cases, using a transistor-level ECDLL-based synthesizer model which is designed in a standard 65-nm CMOS technology.

A. Behavioral Validation

The mean SCR of the synthesizer as a function of SPE and DCD is illustrated in Fig. 9 and 10, using a normalized delay

SD of 2% and 0.2%, respectively. Fig. 9(a) and 10(a) demonstrate the harmonic spur levels at $f_s = f_c - f_{ref}$, while Fig. 9(b) and 10(b) illustrate the spur levels at $f_s = f_c - 2f_{ref}$. The solid planes represent the MC simulation results of the analytical model of (9), whereas the solid lines with markers depict the predicted mean SCR provided by (32). It can be verified from Fig. 9 and 10 that the predicted results closely follow that of the MC simulations. So as to verify the accuracy of the proposed model against wide-range delay SD values, the mean SCR is plotted in Fig. 11 with respect to normalized delay SD which is swept from 0.01% to 5%. It can be seen that the prediction results closely matches that of the MC simulation with an error of 0 dB for $\sigma/\mu = 0.01\%$ to 1%, 1 dB at $\sigma/\mu = 2\%$, and 2 dB at $\sigma/\mu = 3\%$ ($SCR_{mean} \approx -15$ dBc). Note that to improve the prediction accuracy for very large delay SD values, higher order Taylor series can be employed to better approximate *sine* and *cosine* functions in (7) and (8), and hence, calculate the more exact model parameters, i.e., the mean and variance of a_n and b_n in (25), (26), and (27). Nevertheless, large delay SD values are in fact avoided due to the stringent requirements on the output spur levels in the context of frequency synthesis for wireless applications. Comparing the results in Fig. 9, 10, and 11 with those in Fig. 4, 5, and 6, respectively, reveals the achieved improvements in the prediction robustness and implies that the proposed model

Fig. 12. Schematic of the simulated ECDLL synthesizer in open-loop regime.

can accurately characterize the spurious performance of ECDLLs for both the even and odd harmonic orders, over wide-range values of SPE, DCD, and delay SD.

B. Transistor-Level Validation

In the previous part, it was verified that the proposed predictive model closely matches the behavioral model of the ECDLL-based synthesizer for SCR estimation over wide-range values of the non-idealities. In this part, the validity and accuracy of the proposed model is investigated by comparing the predicted PDFs from the closed-form expression (31), with MC simulation histograms of the transistor-level model of the synthesizer, designed in a standard 65-nm CMOS process. Note that due to the large simulation time which is involved in MC simulations of the transistor-level design, it is not affordable to simulate the SCR for wide-range values of SPE and DCD. As a consequence, three different pairs of (T_{spe}, T_{dcd}) are instead selected for this experiment. Also, note that the reported SCR values in this part correspond to the largest adjacent and alternate harmonics, i.e., $\max(SCR_{N-1}, SCR_{N+1})$ for the adjacent, and $\max(SCR_{N-2}, SCR_{N+2})$ for the alternate harmonic. The simulated schematic of the ECDLL synthesizer is shown in Fig. 12, where 25 phase-shifted outputs of the VCDL are combined using 25 ideal stages of voltage-to-current (V-I) converters to generate the carrier at $f_c = 10$ GHz. Note that in practical implementations [8], [12], an LC-tank load can be used to enhance the ECDLL output impedance and also suppress the spur levels depending on its Q factor [16]. So as to reduce the simulation time, the synthesizer is simulated in an open-loop regime. The effect of mismatch between up and down signals in PD/CP is modeled by manually introducing T_{spe} in this open-loop schematic. Due to the open-loop operation, the actual SPE may slightly deviate from its designated value for each MC sample.

In order to obtain SCR for each MC sample, transient simulations are performed on the testbench of Fig. 12 for duration of 16.6 ns, containing 5 cycles of the reference clock. Discrete Fourier transform (DFT) function is then applied to the synthesized output to calculate the corresponding magnitudes of the carrier and harmonic spurs. Simulations are performed using Cadence Spectre while accelerated parallel simulator (APS) is enabled. Transient noise option of the simulator is not enabled to speed up the MC simulations. However, since the noise will result in random jitter on the DLL output phases which is not identical from cycle to cycle, it does not produce a fixed-pattern periodicity. Therefore, it will give rise to the phase noise rather than the spur magnitude. The employed tolerance options of the simulator are $reltol = 10^{-6}$, $vabstol = 10$ nV, and $iabstol = 100$ fA. Furthermore, the simulations are carried out on a single 2.8-GHz processor core, with 3.7 GB of memory. Considering the utilized configurations, the total simulation time regarding 10^4 MC

Fig. 13. Delay stage. Biasing corresponds to the case of zero SPE.

TABLE I
PREDICTION MODEL PARAMETERS AND THEIR RELATIONS WITH TECHNOLOGY, TRANSISTOR-LEVEL, AND SYSTEM PARAMETERS

Prediction model parameter	Transistor-level and technology parameter	System parameter	Relation
$\sigma_r / \mu_r, \sigma_f / \mu_f$	$\sigma_I, \sigma_{VTH}, V_{TH}, WL, V_{DD}, V_n, V_p, A_\beta, A_{VTH}$	—	(35) – (37)
$\lambda, \kappa_c, \kappa_s, \alpha_m, \beta_m$	—	$T_{dcd}, T_{spe}, n, N, T_{ref}$	(15) – (17)
$\mu_{an}, \mu_{bn}, \sigma_{cof}$	—	—	(25) – (27)
h, K	—	—	(33), (34)

samples is around 238 Ks (23.8 s/sample). On the other hand, the predictions are carried out based on closed-form expressions where no simulation is involved. In order to plot the proposed SCR PDF of (31) for a given harmonic n , Table I summarizes how the prediction model parameters are related to the system, transistor-level, and technology parameters. As shown in Fig. 13, a current-starved delay stage with an output inverter buffer is utilized and carefully designed to provide a mean delay of $\mu = \mu_r \approx \mu_f \approx 100$ ps. Employing the mismatch equations for MOS devices [17], the value of the normalized stage-delay SD for a current-starved delay stage of Fig. 13 is derived [13] as

$$\frac{\sigma}{\mu} = \sqrt{\left(\frac{\sigma_I}{I}\right)^2 + \left(\frac{\sigma_{VTH}}{V_{DD} - V_{TH}}\right)^2} \quad (35)$$

where σ_I and σ_{VTH} are the current and voltage-threshold SDs,

$$\frac{\sigma_I}{I} = \frac{A_\beta}{\sqrt{WL_{CS}}} + \frac{2A_{VTH}}{(V_{GS} - V_{TH})\sqrt{WL_{CS}}} \quad (36)$$

$$\sigma_{VTH} = \frac{A_{VTH}}{\sqrt{WL_B}} \quad (37)$$

Also, WL_{CS} and WL_B are the areas of the current-starved and buffer transistors, and A_β and A_{VTH} are the technology-dependent constants. With the transistor sizing and voltage biasing shown in Fig. 13, and the technology constants of the target standard 65-nm CMOS process, the delay SD values of $\sigma_r / \mu_r \approx 0.27\%$ and $\sigma_f / \mu_f \approx 0.29\%$ are obtained. So as to observe the accuracy of the predictive model when the delay mismatch dominates SPE and DCD values, a SPE-DCD pair of (0, 0) is selected as the first test case. It can be perceived from the SCR distributions in Fig. 14, that both the PDFs of the proposed predictive model (solid line with markers) given by (31), and the approximation model of [16] (dashed line) closely match the histogram of the transistor-level MC simulations (bar chart), for either of the harmonics. It can also be verified that for this test case where the delay SD absorbs SPE and DCD values, the mean SCR of the adjacent harmonic, shown in Fig. 14(a), is larger than that of the alternate

Fig. 14. Predicted PDF versus transistor-level MC histogram of SCR with $(T_{spe}, T_{dcd}) = (0, 0)$: (a) the largest adjacent, and (b) the largest alternate spur.

Fig. 15. Predicted PDF versus transistor-level MC histogram of SCR with $(T_{spe}, T_{dcd}) = (5ps, 9.3ps)$: (a) the largest adjacent, and (b) the largest alternate spur.

Fig. 16. Predicted PDF versus transistor-level MC histogram of SCR with $(T_{spe}, T_{dcd}) = (10ps, 9.3ps)$: (a) the largest adjacent, and (b) the largest alternate spur.

harmonic plotted in Fig. 14(b). The second test is performed using the non-ideality pair (5ps, 9.3ps). Note that the required $T_{spe} = 5$ ps is introduced to both the rising and falling-edge delays, by modifying the bias voltages to $V_n = 851.6$ mV and $V_p = 347.3$ mV in Fig. 13. Moreover, the value of DCD is initially set to $T_{dcd} = 10$ ps by changing the pulsewidth of the square wave input clock source in the schematic testbench of Fig. 12. The effective DCD value however, is about 9.3 ps, according to the transient simulation of the waveforms. A similar SPE-DCD pair has been utilized as the input to the PDF expressions of the predictive models and the comparison results are depicted in Fig. 15. It can be seen that the SCR of the alternate harmonic dominates that of the adjacent harmonic by 4 dB. It can also be perceived that the model of [16] exhibits a prediction error of 2 dB and 12 dB, for the adjacent

and alternate harmonic spurs, respectively, while the proposed model predicts the mean SCR accurately for both harmonics. As the last experiment and to evaluate the accuracy of the model when the delay mismatch is absorbed by relatively large SPE and DCD values, a test pair of (10ps, 9.3ps) is employed. To provide the required $T_{spe} = 10$ ps, the bias voltages of the current-starved delay elements are changed to $V_n = 858.7$ mV and $V_p = 338.1$ mV. It can be noticed from Fig. 16 that in this case, the PDF of the proposed model can follow the histogram of the transistor-level MC simulations for both the adjacent and alternate harmonic spurs, while the prediction error of [16] is magnified to 6 dB and 18 dB.

VII. CONCLUSION

Evaluation of spurious performance in ECDLL-based

frequency synthesizers demands exhaustive statistical simulations using MC method which significantly slow down the iterative design procedure of such synthesizers. Based on the derived closed-form expressions for the PDF and mean of the spur magnitudes, this paper introduces a generic predictive model for characterizing the spurious performance of ECDLL-based synthesizers. The important characteristic of the proposed model is that its prediction accuracy is independent of the design parameters and the system non-idealities. Hence, the model is comparable to MC method in terms of accuracy and robustness, whereas it alleviates the need for exhaustive statistical simulations. The accuracy of the model has been investigated through MC simulations of the behavioral model of the synthesizer, against wide-range values of SPE, DCD, and stage-delay SD. Moreover, the validity of the model has been further inspected by performing MC simulations on a transistor-level model of the synthesizer which is designed in a standard 65-nm CMOS process. Comparison of the simulated and estimated results verifies that the predictive model is generic, and hence, can be considered as a reliable replacement to MC method for characterizing the spurious performance of ECDLL-based frequency synthesizers.

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