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Building Blocks for Low-Voltage Analog-to-Digital Interfaces

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Abstract

In today's system-on-chip (SoC) implementations, power consumption is a key performance specification. The proliferation of mobile communication devices and distributed wireless sensor networks has necessitated the development of power-efficient analog, radio-frequency (RF), and digital integrated circuits. The rapid scaling of CMOS technology nodes presents opportunities and challenges. Benefits accrue in terms of integration density and higher switching speeds for the digital logic. However, the concomitant reduction in supply voltage and reduced gain of transistors pose obstacles to the design of high-performance analog and mixed-signal circuits such as analog front-ends (AFE) and data converters.

To achieve high DC gain, multistage amplifiers are becoming necessary in AFEs and analog-to-digital converters (ADCs) implemented in the latest CMOS process nodes. This thesis includes the design of multistage amplifiers in 40 nm and 65 nm CMOS processes. An AFE for capacitive body-coupled communication is presented with transistor schematic level results in 40 nm CMOS. The AFE consists of a cascade of amplifiers to boost the received signal followed by a Schmitt trigger which provides digital signal levels at the output. Low noise and reduced power consumption are the important performance criteria for the AFE. A two-stage, single-ended amplifier incorporating indirect compensation using split-length transistors has been designed. The compensation technique does not require the nulling resistor used in traditional Miller compensation. The AFE consisting of a cascade of three amplifiers achieves 57.6 dB DC gain with an input-referred noise power spectral density (PSD) of $4.4 \text{ nV}/\sqrt{\text{Hz}}$ while consuming 6.8 mW.

Numerous compensation schemes have been proposed in the literature for multistage amplifiers. Most of these works investigate frequency compensation of amplifiers which drive large capacitive loads and require low unity-gain frequency. In this thesis, the frequency compensation schemes for high-speed, low-voltage multistage CMOS amplifiers driving small capacitive loads have been investigated. Existing compensation schemes such as the nested Miller compensation with nulling resistor (NMCNR) and reversed nested indirect compensation (RNIC) have been applied to four-stage and three-stage amplifiers designed in 40 nm and 65 nm CMOS, respectively. The performance metrics used for comparing the different frequency compensation schemes are the unity gain frequency, phase margin (PM), and total amount of compensation capacitance used. From transistor schematic simulation results, it is concluded that RNIC is more efficient than NMCNR.

Successive approximation register (SAR) analog-to-digital converters (ADCs) are becoming increasingly popular in a wide range of applications due to their high power efficiency, design simplicity and scaling-friendly architecture. Single-channel SAR ADCs have reached high resolutions with sampling rates exceeding 50 MS/s. Time-interleaved SAR ADCs have pushed beyond 1 GS/s with medium resolution. The generation and buffering of reference voltages is often

not the focus of published works. For high-speed SAR ADCs, due to the sequential nature of the successive approximation algorithm, a high-frequency clock for the SAR logic is needed. As the digital-to-analog converter (DAC) output voltage needs to settle to the desired accuracy within half clock cycle period of the system clock, a speed limitation occurs due to imprecise DAC settling. The situation is exacerbated by parasitic inductance of bondwires and printed circuit board (PCB) traces especially when the reference voltages are supplied off-chip. In this thesis, a power efficient reference voltage buffer with small area has been implemented in 180 nm CMOS for a 10-bit 1 MS/s SAR ADC which is intended to be used in a fingerprint sensor. Since the reference voltage buffer is part of an industrial SoC, critical performance specifications such as fast settling, high power supply rejection ratio (PSRR), and low noise have to be satisfied under mismatch conditions and over the entire range of process, supply voltage and temperature (PVT) corners. A single-ended, current-mirror amplifier with cascodes has been designed to buffer the reference voltage. Performance of the buffer has been verified by exhaustive simulations on the post-layout extracted netlist.

Finally, we describe the design of a 10-bit 50 MS/s SAR ADC in 65 nm CMOS with a high-speed, on-chip reference voltage buffer. In a SAR ADC, the capacitive array DAC is the most area-intensive block. Also a binary-weighted capacitor array has a large spread of capacitor values for moderate and high resolutions which leads to increased power consumption. In this work, a split binary-weighted capacitive array DAC has been used to reduce area and power consumption. The proposed ADC has bootstrapped sampling switches which meet 10-bit linearity over all PVT corners and a two-stage dynamic comparator. The important design parameters of the reference voltage buffer are derived in the context of the SAR ADC. The impact of the buffer on the ADC performance is illustrated by simulations using bondwire parasitics. In post-layout simulation which includes the entire pad frame and associated parasitics, the ADC achieves an ENOB of 9.25 bits at a supply voltage of 1.2 V, typical process corner, and sampling frequency of 50 MS/s for near-Nyquist input. Excluding the reference voltage buffer, the ADC achieves an energy efficiency of 25 fJ/conversion-step while occupying a core area of 0.055 mm².

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Preface

Thesis outline

This thesis consists of two parts; Part-I, which provides the background and Part-II, that lists the publications. Part-I is divided into three chapters. Chapter 1 introduces the reader to the challenges posed by CMOS process scaling to the design of accurate, low-voltage analog and mixed-signal circuits. Several design techniques which help to circumvent the impact of low supply voltages are discussed in Chapter 1. The need for multistage amplifiers in deep-submicron CMOS technologies along with frequency compensation techniques is illustrated in Chapter 2. In Chapter 3, the successive approximation register (SAR) analog-to-digital converter (ADC) architecture is described along with the different DAC switching schemes that have been recently published. The design considerations for the key building blocks of the SAR ADC are also discussed. Chapter 4 provides the conclusions and directions for future work.

Publications

Part-II is comprised of three peer-reviewed papers (Paper A, B, C), and a journal paper under review (Paper D) as follows.

- Paper A: **Prakash Harikumar**, Muhammad Irfan Kazim, and J Jacob Wikner, “An analog receiver front-end for capacitive body-coupled communication,” in *Proc. IEEE NORCHIP Conf.*, Copenhagen, Denmark, Nov. 2012.
- Paper B: Syed Ahmed Aamir, **Prakash Harikumar**, and J Jacob Wikner, “Frequency compensation of high-speed, low-voltage CMOS multistage amplifiers,” in *Proc. IEEE Int. Symp. Circuits Syst. (ISCAS)*, Beijing, China, May 2013.
- Paper C: **Prakash Harikumar**, Pavel Angelov, and Robert Hägglund, “Design of a reference voltage buffer for a 10-bit 1-MS/s SAR ADC,” in *Proc. Int. Mixed Design of Integrated Circuits and Systems (MIXDES) Conf.*, Lublin, Poland, June 2014.

Paper D: **Prakash Harikumar**, and J Jacob Wikner, “A 10-bit, 50 MS/s SAR ADC in 65 nm CMOS with on-chip reference voltage buffer,” submitted to *Journal of Analog Integrated Circuits and Signal Processing (Springer)*, Mar. 2014.

Publications not included in the thesis

The following papers contains work done by the author but are not included in the thesis.

1. **Prakash Harikumar**, Pavel Angelov and Robert Häggglund, “Reference voltage buffers for a 10-bit 1-MS/s SAR ADC,” in *Proc. Swedish System On Chip Conf. (SSoCC)*, Ystad, Sweden, May 2013.
2. **Prakash Harikumar**, Anu Kalidas Muralidharan Pillai, and J Jacob Wikner, “A study on switched-capacitor blocks for reconfigurable ADCs,” in *Proc. 18th IEEE Int. Electronics, Circuits and Systems (ICECS) Conf.*, Beirut, Lebanon, Dec. 2011.

Contributions

The main contributions of this thesis are as follows:

- Transistor-schematic design of an analog front-end for capacitive body-coupled communication receiver (**Paper A**). The AFE consists of a cascade of amplifiers followed by a Schmitt trigger. In this work, a two-stage, single-ended amplifier has been designed in 40 nm CMOS. The amplifier employs the indirect compensation scheme utilizing split-length transistors. This helps to eliminate the nulling resistor required in traditional Miller compensation and enhances the power efficiency. The AFE achieves 57.6 dB DC gain with an input-referred noise power spectral density (PSD) of 4.4 nV/ $\sqrt{\text{Hz}}$ while consuming 6.8 mW.
- The frequency compensation schemes for high-speed, low-voltage multi-stage CMOS amplifiers driving small capacitive loads have been investigated (**Paper B**). Existing compensation schemes such as the nested Miller compensation with nulling resistor (NMCNR) and reversed nested indirect compensation (RNIC) have been applied to four-stage and three-stage amplifiers designed in 40 nm and 65 nm CMOS, respectively. The performance metrics used for comparing the different frequency compensation schemes are the unity-gain frequency, phase margin (PM), and total amount of compensation capacitance used. From transistor schematic simulation results, it is concluded that RNIC is more efficient than NMCNR.
- A power efficient reference voltage buffer with small area has been implemented in 180 nm CMOS for a 10-bit, 1 MS/s SAR ADC which is intended to be used in a fingerprint sensor (**Paper C**). Important design parameters of the buffer such as slew rate, DC gain and unity gain frequency have been derived in the context of the SAR ADC to aid the design process. Since the reference voltage buffer is part of an industrial SoC, critical performance specifications such as fast settling, high power supply rejection ratio (PSRR), and low noise have to be satisfied under

mismatch conditions and over the entire range of process, supply voltage and temperature (PVT) corners. A single-ended current-mirror amplifier with cascodes has been designed to buffer the reference voltage. The performance of the buffer has been verified by exhaustive simulations on the post-layout extracted netlist.

- Design and implementation of a 10-bit, 50 MS/s SAR ADC in 65 nm CMOS with a high-speed, on-chip reference voltage buffer (**Paper D**). In this work, a split binary-weighted capacitive array DAC has been used to reduce the area and power consumption. The proposed ADC has bootstrapped sampling switches which meet 10-bit linearity over all PVT corners and a two-stage dynamic comparator. The important design parameters of the reference voltage buffer are derived in the context of the SAR ADC. The impact of the buffer on the ADC performance is illustrated by simulations using bondwire parasitics. In post-layout simulation which includes the entire pad frame and associated parasitics, the ADC achieves an ENOB of 9.25 bits at a supply voltage of 1.2 V, typical process corner, and sampling frequency of 50 MS/s for a near-Nyquist input signal. Excluding the reference voltage buffer, the ADC achieves an energy efficiency of 25 fJ/conversion-step while occupying a core area of 0.055 mm².

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List of Abbreviations

ADC	Analog-to-Digital Converter
AFE	Analog Front End
CMFB	Common-Mode FeedBack
CMOS	Complementary Metal Oxide Semiconductor
CM	Common-Mode
CS	Common-Source
DAC	Digital-to-Analog Converter
DFF	D-type Flip Flop
DNL	Differential Nonlinearity
DSP	Digital Signal Processor
ENOB	Effective Number of Bits
ERBW	Effective Resolution Bandwidth
FOM	Figure of Merit
GBW	Gain Bandwidth Product
INL	Integral Nonlinearity
LHP	Left Half Plane
LSB	Least Significant Bit
MIM	Metal Insulator Metal
MSB	Most Significant Bit
NMCNR	Nested Miller Compensation with Nulling Resistor

NMC	Nested Miller Compensation
OTA	Operational Transconductance Amplifier
PCB	Printed Circuit Board
PM	Phase Margin
PSD	Power Spectral Density
PVT	Process Voltage Temperature
RF	Radio Frequency
RHP	Right Half Plane
RNIC	Reversed Nested Indirect Compensation
RVbuffer	Reference Voltage Buffer
S/H	Sample and Hold
SAR	Successive Approximation Register
SFDR	Spurious-Free Dynamic Range
SMC	Simple Miller Compensation
SMR	Signal-to-Metastability-Error Ratio
SNDR	Signal-to-Noise-and-Distortion Ratio
SNR	Signal-to-Noise Ratio
TG	Transmission Gate

Part I

Background

Introduction

1.1 Introduction

The confluence of technological advancements in the fields of microelectronics, wireless communication, and sensors, coupled with the demand for affordable and intelligent health monitoring systems has engendered the concept of wireless body area networks (WBANs). According to IEEE 802.15.6, WBAN provides an international standard for low power and extremely reliable communication within and in close proximity to the human body supporting a vast range of data rates from 75.9 kbps up to 15.6 Mbps [1]. WBAN encompasses medical applications such as pacemaker, ECG, blood pressure monitoring, and non-medical applications such as streaming music for headsets, gaming applications, social networking, etc. [1]. WBANs are implemented as networks of intelligent, low power sensors that can collect, store, and relay information. Wireless sensor networks also find application in industrial process monitoring, forest fire detection, and military surveillance [2].

For the nodes in the wireless sensor networks, low power consumption is paramount especially since they are powered by batteries or energy-harvesting sources. Hence, the power consumption of the constituent circuits must be minimized. The basic architecture of an intelligent sensor node consists of an analog front-end (AFE), analog-to-digital converter (ADC), a digital signal processor and a short-range radio apart from the sensor itself. Integrating the sensor electronics on a single die with the fewest number of supply voltages is imperative for achieving good performance at low power consumption. Hence, the design of highly power-efficient AFEs and ADCs with suitable performance becomes essential. In this chapter, an overview of the opportunities and challenges presented by CMOS technology scaling for the design of analog and mixed-signal circuits is provided.

1.2 Impact of CMOS Scaling on Analog and Mixed-Signal Circuits

Today's system-on-chips (SoCs) consists of microprocessors, digital logic, memories, analog front-ends (AFEs), and data converters integrated on the same die [3]. CMOS technology is the popular choice for implementing such SoCs owing to its high fabrication density and absence of static power dissipation. The continued scaling of CMOS technology has resulted in very high speeds for the digital circuits. The scaling of the supply voltage with each successive CMOS process node reduces the power consumption of digital circuits. However, process scaling does not benefit analog circuit design to the same extent.

1.2.1 Reduced Supply Voltage

For every new CMOS process node, the gate-oxide thickness is lower and this requires a proportional reduction in the supply voltage in order to maintain device reliability. However, the threshold voltages do not scale at the same rate in order to mitigate leakage. The reduction in supply voltage degrades important analog performance metrics of the transistors such as the intrinsic voltage gain g_m/g_{ds} and linearity. This degradation is caused by the reduced voltage headroom available for biasing the transistors in the desired operating region. The problem is expected to worsen as CMOS scaling progresses rapidly and supply voltages reduce below 1 V.

1.2.2 Increased Speed

The transit frequency (f_T), represents the frequency at which the current gain of a transistor becomes unity. It is given by

$$f_T = \frac{g_m}{2\pi C_g}, \quad (1.1)$$

where g_m is the transconductance and C_g is the gate capacitance of the transistor.

For a given CMOS process node, f_T is a metric for device speed and is inversely proportional to the channel length of the transistor. Thus f_T increases with process scaling which results in larger bandwidth for analog designs.

1.2.3 Higher Leakage

In newer CMOS process nodes, the reduced threshold voltage of the transistors leads to a significant increase in subthreshold leakage current which is given by [4]

$$I_{DS} = \mu_0 C_{ox} \frac{W}{L} (m-1) V_T^2 e^{\frac{V_{GS}-V_{TH}}{mV_T}} (1 - e^{\frac{-V_{DS}}{V_T}}), \quad (1.2)$$

where V_{TH} is the threshold voltage, $V_T = kT/q$ is the thermal voltage, C_{ox} is the gate oxide capacitance, μ_0 is the zero-bias mobility and m is the subthreshold swing coefficient. Another contributor is the gate leakage current which occurs due to the high electric field across the gate oxide and the low oxide thickness. Major constituents of gate leakage are gate oxide tunneling and injection of hot carriers from substrate to the gate oxide [4]. In analog and mixed-signal circuits working at low frequencies, the leakage power forms a significant portion of the total power consumption. Also the leakage mechanism introduces nonlinearities in sample-and-hold circuits as will be discussed in the chapter 3.

1.2.4 Process Variations

Fluctuations in the manufacturing steps cause the transistor behavior to deviate from the nominal. Also, the supply voltage and temperature will vary across the chip [5]. Process variations are classified into two: die-to-die or inter-die and within-die or intra-die. Die-to-die (D2D) affects each transistor in the die in a systematic way [6]. Within-die (WID) variation affects each transistor in the die differently. WID variations are caused by random dopant fluctuations, line-edge roughness or channel-length variations [6]. For analog circuits, the variations in process, supply voltage and temperature (PVT) will have considerable impact on offset, linearity, common-mode rejection ratio (CMRR), power supply rejection ratio (PSRR), etc. For 90 nm and below, layout effects such as well proximity effect (WPE) and shallow-trench isolation (STI) stress will result in bias-point shifts of 20-30% in analog circuits [7]. It is shown in [8] that though STI-stress causes large deviation in drain current and threshold voltage, it does not contribute to random mismatch. Inaccuracies in the photolithographic process will cause random variations in the dimensions of the active and passive components on the chip. With the reducing feature sizes of newer process nodes, limitations of accuracy in the lithography steps aggravate variations in the manufactured circuits [9].

1.3 Challenges in Low-Voltage Design

Today's SoCs contain a large amount of digital logic whose power consumption needs to be minimized for overall power efficiency. The power consumption of digital circuits consists of dynamic and static components. The dynamic power consumption P_{Dyn} is dominated by the switching of the digital gate while the static power consumption P_{st} is caused by the leakage current. For a CMOS logic gate, P_{Dyn} and P_{st} are given by

$$P_{Dyn} = \alpha C_L V_{DD}^2 f, \quad (1.3)$$

$$P_{st} = I_{leakage} V_{DD}, \quad (1.4)$$

where α is the switching activity of the gate, C_L is the load capacitance, V_{DD} is the supply voltage, f is the switching frequency, and $I_{leakage}$ is the leakage

current. From (1.3), it is seen that a lower supply voltage will significantly reduce the dynamic power consumption due to the quadratic dependency of P_{Dyn} on V_{DD} . The static power consumption also decreases with lower supply voltage as seen in (1.4). Migration to a newer CMOS process node with lower supply voltage will thus yield major savings in the power consumed by digital blocks. Since the analog and mixed-signal blocks will need to work with the same voltages, a detailed review of the challenges and available solutions for low-voltage analog design is presented in this section.

1.3.1 Low Overdrive for Switches

The analog switch is a key component in switched-capacitor (SC) filters, $\Sigma\Delta$ modulators and SAR ADCs. The switches are implemented using MOS transistors. In ADCs, the switch forms part of the sample-and-hold circuit. The linearity of the ADC is determined to a large extent by the linearity of the sampling switch. The primary cause of non-linearity in a MOS switch is the non-linear dependency of its ON-resistance (R_{ON}) on the gate overdrive voltage. The ON-resistance of a simple NMOS switch is given by

$$R_{\text{ON}} = \frac{1}{\mu_n C_{\text{ox}} \frac{W}{L} (V_{\text{GS}} - V_{\text{TH}})} = \frac{1}{\mu_n C_{\text{ox}} \frac{W}{L} (V_{\text{DD}} - V_{\text{in}} - V_{\text{TH}})}, \quad (1.5)$$

where μ_n is the electron mobility, W , L are the device dimensions, V_{TH} is the threshold voltage, C_{ox} is the gate oxide capacitance, and $(V_{\text{GS}} - V_{\text{TH}})$ is the gate overdrive voltage of the switch. From (1.5), it is seen that the ON-resistance of the switch varies with the input signal V_{in} thus causing non-linearity. Since simple NMOS, PMOS switches cannot support rail-to-rail sampling of inputs, a common workaround is to use a transmission-gate (TG) switch that uses a parallel combination of NMOS and PMOS switches. The TG helps to lower the effective ON-resistance. A comparison of the R_{on} variation with input voltage of the minimum sized NMOS, PMOS, and TG switches in CMOS 65 nm process is shown in Fig. 1.1. As long as the supply voltage is higher than $V_{\text{TH,N}} + |V_{\text{TH,P}}|$, the TG switch is fully functional. However for lower supply voltages, there will be a region around the middle of the supply voltage where both the NMOS and PMOS devices are OFF. For input voltages lower than $V_{\text{DD}} - V_{\text{TH,N}}$, the NMOS conducts, while the PMOS is ON only for input voltages higher than $V_{\text{TH,P}}$. For rail-to-rail operation in circuits with ultra-low supply voltages, the gate voltage of the switches need to be higher than the rated supply voltage. In modern CMOS processes, low threshold voltage transistors that work at the core supply voltages are available. By using such devices, the limited gate overdrive problem can be mitigated [10].

A drawback of using the low- V_{TH} devices is that they suffer from significant leakage currents. For low-speed ADCs, the signal-dependent leakage in the sample-and-hold block causes non-linearities [11]. An obvious method for reducing the subthreshold leakage current is to use low-width transistors with longer channel lengths. However, this will lead to an unacceptable increase in

Figure 1.1: Variation of R_{ON} vs input voltage for MOS switches.

the ON-resistance of the switch. The analog-T switch (AT-switch) proposed in [12] helps to suppress the subthreshold-leakage in switches that uses low- V_{TH} devices. In [12], the analog ground is set to an intermediate voltage ($V_{\text{DD}}/2$) which causes a reverse V_{GS} voltage during the OFF state. This essentially reduces the first exponential term in (1.2), thus mitigating leakage. In [13], the subthreshold leakage is suppressed by equating the drain and source voltages of the switch. This technique makes $V_{\text{DS}} = 0$ which causes the term $(1 - e^{(-V_{\text{DS}}/V_{\text{T}})})$ in (1.2) to become zero.

A technique that helps to maintain a large, constant gate-overdrive for the sampling switch irrespective of the input voltage is bootstrapping [14], [15]. The basic bootstrapped switch is shown in Fig. 1.2. During the precharge phase ϕ_2 , the bootstrap capacitor C_{boot} is charged to V_{DD} and the sampling switch Sw remains OFF. During the sampling phase ϕ_1 , C_{boot} gets connected between the gate and source terminals of the switch, essentially making $V_{\text{GS}} = V_{\text{DD}}$. The overdrive voltage is thus made constant and equal to the supply voltage which helps to obtain a low and constant ON-resistance. In real circuit implementations, V_{GS} will be lower than V_{DD} due to the voltage division on the parasitic capacitances connected to C_{boot} .

Another remedy for the low overdrive voltage of switches in low-voltage implementations is clock boosting or clock doubling [16], [17]. In [16], non-overlapping clocks charge a capacitor to $2V_{\text{DD}}$ which is then used to drive the gate of the sampling switch. The clock doubling circuit proposed in [17] is shown in Fig. 1.3. When Clk_{in} goes low, M_1 and M_3 turn on while M_2 turns off. The node voltages V_a and V_b reach ground and V_{DD} respectively. The output clock Clk_{out} goes low. When Clk_{in} goes high, M_1 and M_3 turn off while M_2 turns on. The node at V_a gets connected to V_{DD} , thus boosting V_b to $2V_{\text{DD}}$. The output

Figure 1.2: Bootstrapped switch topology.

clock Clk_{out} also becomes $2V_{DD}$.

1.3.2 Reduced Signal Swing

A direct consequence of the reduced supply voltage in advanced CMOS processes is the reduction in available signal swing. Consider an ADC with a supply voltage V_{DD} . Since the ADC is usually preceded by signal conditioning circuits like amplifiers, the input signal range of the ADC will be lower than the rail-to-rail swing. The input signal range of the ADC is assumed to be

$$V_{in} = \alpha V_{DD}, \quad (1.6)$$

where $\alpha < 1$. For a given amount of capacitance in the sample-and-hold block of the ADC, the thermal noise associated with sampling is kT/C . For simplicity, we consider only the sampler noise in the ADC, resulting in an SNR given by

$$SNR = 10 \log \left(\frac{V_{in}^2}{kT/C} \right) = 10 \log \left(\frac{\alpha^2 V_{DD}^2}{kT/C} \right). \quad (1.7)$$

From (1.7), it is seen that SNR degrades with reduction of supply voltage assuming a constant sampling capacitance and constant α . In other words, to maintain the SNR under reduced supply voltages, an increased capacitance is required which inevitably increases the power consumption. The signal swing at the output of analog blocks such as amplifiers is decreased for low supply voltages. Consider the common-source (CS) output stage of an amplifier shown in Fig. 1.4. It is readily seen that the maximum output swing is given by

$$V_{out,pp} = V_{DD} - 2V_{DS,sat}. \quad (1.8)$$

For a supply voltage $V_{DD} = 0.6$ V, and $V_{DS,sat} = 0.2$ V, the output signal swing is only 0.2 V which is insufficient for many applications. It is well known that the linearity performance of amplifiers, which is quantified by HD2 and HD3,

Figure 1.5: Voltage headroom in a single-stage differential amplifier.

From (1.9) and (1.10), it is seen that the minimum supply voltage is limited by $V_{DS,sat}$ while the input common-mode range is limited by V_{TH} . Since $V_{DS,sat}$ does not scale with technology [18] and V_{TH} scales at a lower rate than the supply voltage, the design of analog circuits with large common-mode range and robust operation over PVT corners in low-voltage process nodes constitutes a formidable challenge.

1.4 Low-Power ADCs and AFEs

The proliferation of battery-powered mobile devices supporting numerous multimedia applications and wireless communication standards has spurred the demand for high-performance SoCs with low power consumption. These SoCs incorporate both AFEs and data converters in addition to digital signal processing blocks. This requires amplifiers, ADCs, and DACs to be implemented in the latest CMOS process nodes to achieve high level of integration and low cost. Ultra low-power ADCs and analog blocks are also required in distributed wireless sensor networks [19], [2] and biomedical interface chips [20]. To achieve high power-efficiency while maintaining sufficient analog performance in terms of dynamic range, linearity etc., scaling-friendly ADC architectures such as the SAR ADC and the $\Sigma\Delta$ ADC are becoming increasingly popular. SAR ADCs with extremely high power-efficiency have been published [21], [22]. To realize opamps with sufficient DC gain and linearity, cascoding is becoming less useful especially for 90 nm and below where the supply voltage is around 1 V. Hence, multistage amplifiers without cascoding are used in AFEs [23] and ADCs [24].

1.5 Conclusion

It is found that there is increasing demand for power-efficient AFEs and ADCs in SoCs used in wireless networks. Design trends seek to exploit the advantages offered by CMOS scaling while employing ingenious circuit architectures and techniques to overcome the challenges posed by supply voltage reduction, leakage, and mismatch. Achieving extremely low power consumption has turned to be a critical goal for circuit designers along with other performance specifications. With energy-harvesting and energy-scavenging power sources being employed in distributed sensor networks, the market for low-power SoCs is only set to grow.

Multistage Amplifiers

2.1 Introduction

Many applications such as low-dropout regulators, high-resolution ADCs, sensitive receiver AFEs, etc., require amplifiers with high gain. In advanced process nodes ($L_{\min} < 90 \text{ nm}$), the reduced supply voltages make cascoding of devices difficult in order to enhance gain. For very low supply voltages below 1 V, cascoding is not feasible [25]. The reduced output resistance of transistors in deep-submicron CMOS processes results in lower intrinsic gain of the transistor. For example, in 130 nm CMOS, the maximum intrinsic gain is around 35 [26]. At more advanced process nodes of 65 nm and 40 nm, the plot of intrinsic gain is shown in Fig. 2.1. Hence cascading of amplifier stages has emerged as a viable option to achieve high gain. When two or more amplifier stages are cascaded, cost is incurred in the form of increased circuit complexity, stability issues, and higher power consumption while we benefit from increased gain.

2.2 Stabilization of Amplifiers

Operational amplifiers are mostly used in a feedback configuration. In a feedback loop, the Barkhausen criteria have to be met in order to ensure that the amplifier does not turn into an oscillator. Stability requires that sufficient phase margin (PM) must be achieved for the OTA. In order to accomplish this, any OTA should have a single dominant pole with the non-dominant poles placed at much higher frequencies than the unity-gain frequency. Designers achieve this by frequency compensation topologies which utilize capacitors and resistors for pole-splitting and pole-zero cancellation. In order to understand the stabilization techniques employed in a three-stage amplifier we review the stability aspects of single- and two-stage amplifiers as a preliminary step. In this

Figure 2.1: Transistor intrinsic gain in advanced CMOS process nodes.

chapter, the following assumptions are made to simplify the transfer function analysis of various amplifiers [27] :

- The gains of all stages are much greater than one.
- The loading and compensation capacitances are much larger than the lumped output parasitic capacitances of each stage.
- Inter-stage coupling capacitances are negligible.

For the different amplifiers described in this chapter, A_i and g_{mi} represent the gain and transconductance of the i th stage. R_i and C_i are the resistance and capacitance associated with the i th stage. All the amplifiers discussed in this chapter have only capacitive loads and do not include any buffer stage at the output. Hence they constitute operational transconductance amplifiers (OTAs).

2.3 Single-Stage OTA

A simple common-source (CS) amplifier is shown in Fig. 2.2. The only high-impedance node is at V_{out} . The gain-bandwidth product (GBW) is given by

$$GBW = g_{m1}/C_L. \quad (2.1)$$

The transfer function is given by [27]

$$A_{v\text{single}}(s) = -\frac{g_{m1}R_L}{1 + sC_LR_L}, \quad (2.2)$$

Figure 2.2: Schematic of the CS amplifier.

Table 2.1: Performance summary of the gain-boostered telescopic cascode OTA.

Parameter	Value
Supply voltage	1.2 V
Process node	65 nm CMOS
DC gain	57 dB
Unity-gain frequency	1 GHz
Phase margin	82°
Power	1.65 mW
Load capacitance	1 pF

where g_{m1} is the output stage transconductance, R_L is the load resistance and C_L is the load capacitance. From (2.2) it is clear that the amplifier has no zero and only one left-half-plane (LHP) pole given by $p_{-3dB} = 1/R_L C_L$ in the frequency response. Thus the single-stage amplifier is always stable. Assuming that the GBW is much higher than the pole, the PM is 90°. The gain of the single-stage amplifier is only $g_{m1} R_L$ which proves inadequate for many applications. In switched-capacitor $\Sigma\Delta$ ADCs which support multiple wireless communication standards [28], high gain OTAs are needed to reduce gain error in the integrator and minimize noise leakage. In [28], the unity-gain frequency of the OTA is 1 GHz. In such scenarios, large channel-length of the transistors cannot be employed to enhance gain since it degrades the speed of the OTA. To achieve the requisite DC gain with a single stage, techniques such as cascoding and gain boosting become necessary. A fully-differential, gain-boostered telescopic cascode OTA was designed in 65 nm CMOS. The schematic of the OTA is shown in Fig. 2.3. A switched-capacitor common-mode feedback (CMFB) was utilized to regulate the output CM voltage of the OTA. The simulated performance of the OTA for nominal PVT conditions is summarized in Table 2.1. Even though a DC gain higher than 55 dB is achieved, the gain-boostered telescopic cascode OTA has a limited output swing of 200 mV only making it unsuitable for low-voltage implementations. The gain-boostered telescopic cascode OTA is very power efficient as there is only one stage that draws static bias current.

Figure 2.3: Schematic of the gain-boostered telescopic cascode OTA.

Figure 2.4: Block diagram of the SMC OTA.

2.4 Two-Stage Miller OTA

In order to achieve high DC gain combined with large output swing, two-stage OTAs are used. In a two-stage OTA, gain is distributed between the two stages and the output stage is a CS stage which provides large output swing. However, it should be noted that the two-stage OTA will entail higher power consumption due to static bias currents flowing in the two stages. The block diagram of a two-stage OTA is shown in Fig. 2.4. It has two high-impedance nodes denoted by V_1 and V_{out} . A compensation capacitor C_m is connected between these nodes to provide pole splitting and to generate a dominant pole. The second-stage must be an inverting amplifier to ensure that C_m provides negative feedback. This topology is referred to as the simple Miller compensation (SMC) amplifier. The transfer function of the SMC amplifier is given by [27]

$$A_{v\text{SMC}}(s) = \frac{g_{m1}g_{mL}R_1R_L \left(1 - s \frac{C_m}{g_{mL}}\right)}{(1 + sC_mg_{mL}R_1R_L) \left(1 + s \frac{C_L}{g_{mL}}\right)}. \quad (2.3)$$

From (2.3) we find that there are two LHP poles and one right-half-plane (RHP) zero. The dominant pole is given by

$$p_1 = \frac{1}{C_mg_{mL}R_1R_L}. \quad (2.4)$$

The non-dominant pole and RHP zero are obtained as

$$p_2 = \frac{g_{mL}}{C_L}, \quad (2.5)$$

$$z_1 = \frac{g_{mL}}{C_m} \quad (2.6)$$

respectively. The GBW of the two-stage amplifier is

$$\text{GBW} = \frac{g_{m1}}{C_m}. \quad (2.7)$$

Figure 2.5: Small-signal model of the SMC amplifier.

In order to achieve closed-loop stability, p_2 and z_1 must be placed at higher frequencies than the GBW. If C_m is increased to separate the poles further, the GBW is reduced as evident from (2.7). Hence overcompensation proves to be harmful. To achieve a PM of $\approx 60^\circ$, the GBW is set to half of p_2 . Using (2.7) and (2.5), we get

$$C_m = 2 \left(\frac{g_{m1}}{g_{mL}} \right) C_L. \quad (2.8)$$

Since the GBW is set to half of p_2 , we have

$$\text{GBW} = \frac{g_{m1}}{C_m} = \frac{1}{2} \left(\frac{g_{mL}}{C_L} \right), \quad (2.9)$$

which is half of that of the single-stage amplifier [27]. It is seen from (2.7) and (2.8) that the GBW of an SMC amplifier cannot be increased by increasing g_{m1} since C_m needs to be increased proportionally in order to maintain (2.9). The GBW can be enhanced by either increasing g_{mL} or by decreasing C_L . The expression for PM is given as [27]

$$\begin{aligned} PM &= 180^\circ - \tan^{-1} \left(\frac{\text{GBW}}{p_1} \right) - \tan^{-1} \left(\frac{\text{GBW}}{p_2} \right) - \tan^{-1} \left(\frac{\text{GBW}}{|z_1|} \right) \\ &= 63^\circ - \tan^{-1} \left(\frac{g_{m1}}{g_{mL}} \right). \end{aligned} \quad (2.10)$$

Thus a low g_{m1}/g_{mL} ratio provides higher PM. However, g_{m1} is limited by the bias current and the size of the input differential pair. To achieve high slew rate, a large bias current is required while low offset necessitates wide input transistors. Hence a low value of g_{m1} is often not realized. In such a scenario, the SMC amplifier needs to be designed with large g_{mL} to achieve sufficient PM. This leads to large currents in the second stage degrading the power efficiency of the amplifier.

From (2.10) it is seen that the RHP zero degrades the PM of the SMC amplifier. The small-signal model of the SMC amplifier is shown in Fig. 2.5. The RHP zero occurs due to the feedforward small-signal current that flows from the input to the output through C_m . In Fig. 2.5, the feedforward current flowing into the output node V_{out} is $i_{\text{ff}} = sC_m V_1$ while the current $g_{mL} V_1$ flows out of the output node [29]. Total current at V_{out} is $i_v = (g_{mL} - sC_m) V_1$. A zero

Figure 2.6: Block diagram of the SMCNR amplifier.

exists in the transfer function where i_v becomes zero [29] as evident from (2.3). By increasing the impedance of the capacitive path, the feedforward current can be reduced and the RHP zero eliminated [27]. This is done by inserting a nulling resistor R_m in series with C_m as shown in Fig. 2.6. The amplifier shown in Fig. 2.6 is called the SMC amplifier with nulling resistor (SMCNR). The transfer function of the SMCNR amplifier is given by [27]

$$A_{v\text{SMCNR}}(s) = \frac{g_{m1}g_{mL}R_1R_L \left[1 - sC_m \left(\frac{1}{g_{mL}} - R_m \right) \right]}{[1 + sC_m(R_m + g_{mL}R_1R_L)] \left[1 + s \frac{C_L(R_1 + R_m)R_L}{R_m + g_{mL}R_1R_L} \right]}. \quad (2.11)$$

The dominant pole for the SMCNR amplifier is same as that for the SMC amplifier and is given by

$$p_1 = \frac{1}{C_m g_{mL} R_1 R_L}. \quad (2.12)$$

The non-dominant pole is given by

$$p_2 \approx \frac{g_{mL}}{C_L}. \quad (2.13)$$

From (2.11), it is seen that the RHP zero is located at

$$z_{RHP} = \frac{1}{C_m \left(\frac{1}{g_{mL}} - R_m \right)} \quad (2.14)$$

There are three ways to nullify the effect of the RHP zero. These are

- Move the zero to infinity. This is done by choosing

$$R_m = \frac{1}{g_{mL}}. \quad (2.15)$$

- Move the zero to the LHP. An LHP zero helps to improve PM. This can be done by selecting

$$R_m > \frac{1}{g_{mL}}. \quad (2.16)$$

Figure 2.7: Schematic of a two-stage amplifier with SMCNR.

- The final option is to move z_{RHP} to the LHP and use it to cancel p_2 . By equating (2.13) with (2.14), we find that this can be achieved by choosing

$$R_m = \frac{C_L + C_m}{g_{mL} C_m}. \quad (2.17)$$

To assess the performance of the SMCNR scheme, a two-stage fully-differential amplifier was designed in 65 nm CMOS. The schematic of the two-stage amplifier employing SMCNR is shown in Fig. 2.7. The CMFB control voltage is applied to the tail-current source transistor. A DC gain of 50 dB, a PM of 60° and a unity-gain frequency higher than 1 GHz were targeted. A MIM capacitor and poly resistor from the 65 nm design kit were used to realize C_m and R_m respectively. A load capacitance of 1 pF was used. The values of C_m and R_m were chosen such that the cancellation of the non-dominant pole by the RHP zero is achieved. Table 2.2 provides the values of the small-signal parameters, the values of C_m and R_m and the location of the poles and the zero for the simulation under nominal PVT conditions. A large transconductance is required in the second stage devices M_6 , M_7 shown in Fig. 2.7 to ensure that the non-dominant pole is at twice the unity-gain frequency which leads to higher power consumption.

Compensation of CMOS amplifiers using split-length transistors has been proposed in [30]. In [30], the compensation capacitor is connected to a low-impedance node in the first stage of a two-stage amplifier which eliminates the RHP zero, creates an LHP zero and places the non-dominant pole at a higher frequency than in the traditional Miller compensation scheme. A fully-differential

Table 2.2: Performance summary of the two-stage SMCNR amplifier.

Parameter	Value
Supply voltage	1.2 V
Process node	65 nm CMOS
p_1	32.08 MHz
p_2	2.641 GHz
z_{RHP}	2.641 GHz
R_m	301.3 Ω
C_m	250 fF
DC gain	36.4 dB
Phase margin	73.5°
Unity-gain frequency	1.63 GHz
Power	6 mW
Load capacitance	1 pF

Table 2.3: Performance summary of the two-stage SLCL compensated amplifier.

Parameter	Value
Supply voltage	1.2 V
Process node	65 nm CMOS
DC gain	44 dB
Unity-gain frequency	1.5 GHz
Phase margin	59°
Power	1.1 mW
Load capacitance	1 pF

two-stage amplifier which realizes frequency compensation using split-length transistors was designed in 65 nm CMOS. The schematic of the two-stage amplifier with split-length current mirror load (SLCL) compensation is shown in Fig. 2.8 where nodes A and B are the low-impedance nodes. A DC gain of 50 dB, a PM of 60° and a unity-gain frequency higher than 1 GHz were targeted. The simulated performance of the two-stage SLCL compensated amplifier for nominal PVT conditions is provided in Table 2.3. It is seen that the SLCL compensation technique is more power efficient than the SMCNR scheme for the given design specifications.

2.5 Nested Miller Compensation for Three-Stage OTAs

The three-stage OTA has three high impedance nodes. This in turn spawns additional non-dominant poles which would require more elaborate frequency compensation schemes than the SMC. Nested Miller compensation (NMC) scheme and its variants are often used to stabilize the three-stage OTA. The block

Figure 2.8: Schematic of a two-stage amplifier with SLCL compensation.

diagram of a three-stage OTA with NMC is shown in Fig. 2.9. Before compensation, the poles associated with the nodes 1, 2 and 3 are close to each other. In order to separate these poles and generate a single dominant pole, compensation capacitors C_{c1} and C_{c2} are connected as shown in Fig. 2.9. The second stage should be non-inverting and the third stage inverting to ensure that the capacitors provide negative feedback and achieve pole-splitting.

The small-signal model of the three-stage OTA with NMC is shown in Fig. 2.10. The transfer function is obtained as [27]

$$A_{v\text{NMC}}(s) = \frac{g_{m1}R_1g_{m2}R_2g_{m3}R_3 \left(1 - \frac{sC_{c2}}{g_{m3}} - \frac{s^2C_{c1}C_{c2}}{g_{m2}g_{m3}}\right)}{(1 + sg_{m3}R_3g_{m2}R_2R_1C_{c1}) \left(1 + \frac{sC_{c2}(g_{m3}-g_{m2})}{g_{m2}g_{m3}} + \frac{s^2C_{c2}C_L}{g_{m2}g_{m3}}\right)}. \quad (2.18)$$

For $g_{m3} \gg g_{m2}$, (2.18) can be further simplified as [27]

$$A_{v\text{NMC}}(s) = \frac{g_{m1}R_1g_{m2}R_2g_{m3}R_3 \left(1 - \frac{sC_{c2}}{g_{m3}} - \frac{s^2C_{c1}C_{c2}}{g_{m2}g_{m3}}\right)}{(1 + sg_{m3}R_3g_{m2}R_2R_1C_{c1}) \left(1 + \frac{sC_{c2}}{g_{m2}} + \frac{s^2C_{c2}C_L}{g_{m2}g_{m3}}\right)}. \quad (2.19)$$

We find that the NMC amplifier has two zeros and three poles. The dominant pole is given by

$$p_1 = -\frac{1}{g_{m3}R_3g_{m2}R_2R_1C_{c1}}. \quad (2.20)$$

Figure 2.9: Block diagram of a three-stage OTA with NMC.

Figure 2.10: Equivalent small-signal model of the NMC amplifier.

The GBW of the three-stage OTA is

$$\text{GBW} = \frac{g_{m1}}{C_{c1}}. \quad (2.21)$$

The zeros are obtained by factorizing the numerator of (2.18). There exists an LHP zero and RHP zero given by [29]

$$z_{LHP} = \frac{-g_{m2}}{2C_{c1}} \left(1 + \sqrt{1 + \frac{4g_{m3}C_{c1}}{g_{m2}C_{c2}}} \right), \quad (2.22)$$

and

$$z_{RHP} = \frac{-g_{m2}}{2C_{c1}} \left(1 - \sqrt{1 + \frac{4g_{m3}C_{c1}}{g_{m2}C_{c2}}} \right) \quad (2.23)$$

respectively. Since $|z_{RHP}| < |z_{LHP}|$, the RHP zero appears at a lower frequency than the LHP zero and degrades the PM [29]. The two non-dominant poles are given by

$$p_2 = \frac{-g_{m2}g_{m3}}{(g_{m3} - g_{m2})C_{c2}}, \quad (2.24)$$

$$p_3 = \frac{-(g_{m3} - g_{m2})}{C_L}. \quad (2.25)$$

Different approaches have been presented in literature to stabilize the NMC amplifier based on the arrangement of poles and zeros [31], [32]. The main disadvantages of the traditional NMC technique are :

- Large power dissipation in the third stage as g_{m3} needs to be large.
- The RHP zero degrades PM.
- Since NMC requires the compensation capacitances to be proportional to the load capacitance for stability reasons, large-value Miller capacitors should be used when amplifiers are loaded with large capacitive loads. Larger Miller capacitors lead to GBW reduction and increased chip area.

Numerous compensation schemes for three stage amplifiers that alleviate the disadvantages of NMC have been proposed [33], [34], [35]. In all these works, the objective is to achieve sufficient PM and GBW with low values of compensation capacitance such that power efficiency is enhanced. **Paper B** [36] compares the NMCNR and reversed nested indirect compensation (RNIC) schemes employed on three-stage and four-stage amplifiers.

2.6 Conclusion

In advanced CMOS process nodes, multistage amplifiers are necessary to achieve sufficiently high DC gain. High DC gain helps to suppress nonlinearities and

noise. A large DC gain also improves settling behavior. Since multistage amplifiers consume larger currents due to the static bias currents in each stage, it is important to select the appropriate architecture and frequency compensation scheme such that power efficiency is maximized.

3.1 Introduction

Traditionally, SAR ADCs were confined to low-speed, medium-resolution applications. However, the higher device speeds available in scaled CMOS technologies, the development of power-efficient digital-to-analog converter (DAC) switching schemes, and the fully dynamic nature of the SAR ADC implementation have contributed to its re-emergence in a broad range of applications. Recently, numerous implementations of ultra low-power and very high speed SAR ADCs have been published [21], [37], [38], [39]. SAR ADCs are also foraying into the high resolution domain (> 11 bits) while maintaining high sampling rates of tens of MS/s [40]. In this chapter, an overview of the SAR ADC architecture and the performance specifications of the key sub-blocks are described.

3.2 SAR ADC Architecture

Figure 3.1 shows the block diagram of the basic SAR ADC architecture. It consists of a sample-and-hold block (S/H), a comparator, DAC and a successive approximation register (SAR). Each conversion consists of a sampling phase followed by the bit cycling phases. During the sampling phase, the input voltage is sampled. The successive-approximation register is set such that the output of the DAC is half of the reference voltage V_{ref} . In the initial bit cycle, the comparator compares the input voltage to $V_{\text{ref}}/2$ in order to determine the most significant bit (MSB). The comparator output is stored in the SAR logic. Simultaneously, the SAR controller generates the next bit approximation. The DAC forms the corresponding scaled value of V_{ref} and the comparator compares the input voltage to the new value of the DAC output. The MSB-1 bit is thus determined. The bit cycles are repeated until all the bits upto the least

Figure 3.1: Basic SAR ADC architecture.

significant bit (LSB) are determined. For an N -bit SAR ADC, one complete conversion requires at least N cycles. In Fig. 3.1, if the comparator is implemented by a regenerative latch [41], then no static bias currents are required in the ADC which leads to excellent power-efficiency. Due to the fully dynamic nature of the SAR ADC, the power consumption scales with the sampling frequency. High-performance pipelined ADCs require linear, high gain opamps that are increasingly challenging to design in advanced CMOS process nodes with low supply voltages. Since the SAR ADC does not require opamps, it has proven to be a very scaling-friendly architecture [42]. In the following sections, the key building blocks of the SAR ADC will be described.

3.3 Sample and Hold Circuit

The sample-and-hold circuit plays a critical role in determining the performance of the SAR ADC. The thermal noise associated with the sampling process degrades the SNR of the ADC. Nonlinear variation of the ON-resistance, signal dependent charge injection, and leakage are other non-idealities of the sampling switch that degrade the performance of the ADC. The important design considerations for the sampling circuit are discussed in the following subsections.

3.3.1 Thermal Noise

The basic sampling circuit consists of a MOS transistor switch and a capacitor. During the tracking phase, when the switch is ON, the MOS transistor approximates a linear resistor. The thermal noise of the MOS transistor is sampled on the capacitor. Since the thermal noise is a random process with white spectrum, it cannot be alleviated by calibration. Along with the quantization noise, the thermal noise of the sampling process sets a fundamental limit on the

Figure 3.2: Charge injection and clock feedthrough errors.

SNR of the ADC. For an N-bit ADC with a full-scale input voltage of V_{FS} , the quantization noise power is given by

$$P_Q = \frac{V_{FS}^2}{12 \cdot 2^{2N}}. \quad (3.1)$$

If the thermal noise of the sampler is designed to be equal to the quantization noise power, a 3 dB degradation in SNR will be incurred. In such a scenario, the value of the total sampling capacitance is given by

$$C_s = 12kT \frac{2^{2N}}{V_{FS}^2}. \quad (3.2)$$

Assuming $V_{FS} = 1$ V, and $N = 10$ bits, a minimum sampling capacitance of 52 fF will be needed to satisfy (3.2) at room temperature. However, in reality, the sampling capacitance is chosen such that the thermal noise contribution is much lower than the quantization noise so as to minimize the SNR degradation.

3.3.2 Charge Injection and Clock Feedthrough

Charge injection and clock feedthrough are error sources associated with the sampling switch. When the switch turns off at the start of the hold phase, the charge in the conduction channel of the MOS transistor is injected into the drain and source nodes which perturbs the sampled value on the capacitor. Clock feedthrough refers to the coupling of the gate control signal of the switch through the parasitic capacitance to the output node. Both these error sources are shown in Fig. 3.2. The combined error voltage due to the two phenomena in an NMOS and PMOS switch are given by [43]

$$\Delta V_{err,NMOS} = \frac{-kW_N L_N C_{ox}(V_{DD} - V_{THN} - V_{IN})}{C_s} - \frac{C_{GD,NMOS}}{C_s + C_{GD,NMOS}} V_{DD}, \quad (3.3)$$

$$\Delta V_{\text{err,PMOS}} = \frac{kW_PL_PC_{\text{ox}}(V_{\text{IN}} - |V_{\text{THP}}|)}{C_s} + \frac{C_{\text{GD,PMOS}}}{C_s + C_{\text{GD,PMOS}}}V_{DD}, \quad (3.4)$$

where k is the fraction of the charge injected on the output node, C_{ox} is the gate-oxide capacitance, V_{THN} and V_{THP} are the threshold voltages, and $C_{\text{GD,NMOS}}$, $C_{\text{GD,PMOS}}$ are the gate-drain overlap capacitance of the NMOS and PMOS respectively. In Eq. (3.3) and (3.4), the first part represents the charge-injection error. It is seen that the charge injection error has a linear dependency on the input signal which causes nonlinearity. An obvious way to reduce charge injection error is to use a larger sampling capacitor C_s . However, this impacts the speed and power consumption adversely. Charge injection error can also be mitigated by circuit techniques such as dummy switch and bottom-plate sampling. Clock feedthrough error represented by the second part in (3.3), (3.4) contributes an offset. It can be alleviated by adopting a fully-differential topology for the converter.

3.3.3 Tracking Bandwidth

The sample-and-hold circuit constitutes a low pass filter (RC network) with a -3 dB frequency given by

$$f_{3\text{dB}} = \frac{1}{2\pi R_{\text{ON}}C_s}. \quad (3.5)$$

For an N -bit converter, $f_{3\text{dB}}$ must be sufficiently high so that the sampled voltage settles with an accuracy greater than N bits ($LSB/2$) which requires [11]

$$f_{3\text{dB}} > \frac{(N+1) \ln(2) f_s}{\pi}, \quad (3.6)$$

where f_s is the sampling frequency. In a SAR ADC utilizing a synchronous SAR logic, f_s will be the frequency of the system clock and thus significantly higher than the actual sampling rate of the ADC. Since the R_{ON} varies with the input signal as shown in (1.5), it is important to ensure that (3.6) is satisfied with some margin for the entire input voltage range of the ADC. Bootstrapped switches come handy in attaining small and constant R_{ON} thus enabling high tracking bandwidth for the sampling switch.

3.3.4 Leakage Current

In the SAR ADC, the sampling switch remains OFF during the bit approximation clock cycles. For low-speed SAR ADCs, the bit cycles can constitute a significant time period during which the sampled voltage can experience droop due to leakage current in the OFF switch. From (1.2), it is seen that the leakage current has a nonlinear dependency on the voltage drop across the switch thus introducing nonlinearity. Hence leakage suppression techniques such as longer channel-lengths for the transistors in the switch and device stacking may be required to avoid performance degradation in the sampling switch.

3.4 Capacitive DAC

The capacitive DAC in the SAR ADC provides feedback of the scaled reference voltage based on the control bits from the SAR logic. The capacitive array DAC is preferred to the resistor string DAC because of the improved matching properties of capacitors and the absence of static power dissipation. In a conventional SAR ADC, a binary-weighted capacitor array is used to implement the DAC. Mismatches between the capacitors in the DAC as well as parasitic capacitances in the DAC layout cause nonlinearity at the ADC output and thus limit the INL, DNL performance of the SAR ADC. To reduce layout-induced mismatch effects, the entire DAC capacitor array is constructed using unit capacitors (C_u) laid out in common-centroid configuration. To minimize the impact of parasitic capacitance due to the interconnections, adequate shielding is provided. In most SAR ADCs, the capacitive DAC also performs the sampling of the input signal. The choice of the unit capacitor is primarily determined by thermal noise and matching requirements. Limitations imposed by the process technology on the minimum capacitor value also have to be considered in the choice of C_u .

Though the binary-weighted capacitive DAC provides good linearity, it imposes large area and power penalties for higher resolutions since the total required capacitance in the DAC increases exponentially with the resolution. Hence alternatives such as the two-stage binary-weighted capacitive DAC [44] and the C-2C ladder DAC [45] have been proposed which have significantly lower total capacitance. Another method of circumventing the area and power penalty in the binary-weighted capacitive DAC is to use custom designed unit capacitors with low values (0.5 fF and below) [46].

Recently, several energy efficient DAC switching schemes have been proposed [47], [48], [38]. In [47], the inefficient down transition in the conventional DAC switching scheme is avoided by splitting the MSB capacitor into a binary-weighted array. The monotonic switching scheme proposed in [48] pre-charges the entire DAC array to V_{ref} at the start of the conversion. During the bit cycles, the capacitors need to be discharged to the ground only based on the SAR decision bits. This helps to save switching energy and also significantly relaxes the requirements on the reference voltage buffer. The energy drawn from the reference voltage during the DAC switching constitutes a significant portion of the SAR ADC power budget. In order to assess the energy efficiency of the different DAC switching schemes, a fully-differential 10-bit SAR ADC was modeled in MATLAB. The different DAC switching schemes were modeled to determine the energy consumption involved in one complete conversion (10 bits). In the model, a binary-weighted capacitor array was used along with a reference voltage of 1 V. The entire input range consisting of 1024 levels was applied to determine the switching energy profile of the different DAC switching schemes. Figure 3.3 plots the switching energy for the different DAC switching schemes employed in a fully-differential 10-bit SAR ADC. The switching energy shown in Fig. 3.3 has been normalized to $C_u V_{\text{ref}}^2$. Table 3.1 compares the average switching energy for the different DAC switching schemes. Other important

Figure 3.3: DAC switching energy vs. output code for a 10-bit SAR ADC.

Table 3.1: Average energy consumption for the DAC switching schemes.

DAC switching scheme	Average energy
Conventional	$1363 C_u V_{\text{ref}}^2$
Split-MSBCap [47]	$852 C_u V_{\text{ref}}^2$
Monotonic [48]	$254.5 C_u V_{\text{ref}}^2$
V_{cm} -based [38]	$170.2 C_u V_{\text{ref}}^2$

features of the DAC switching schemes employed in an N -bit SAR ADC are enumerated in Table 3.2. From Table 3.2, it is seen that the monotonic switching scheme causes variation in the input CM level of the comparator which gives rise to signal-dependent offset voltage. This will degrade the linearity of the ADC unless remedial measures are taken [48]. The V_{cm} -based switching method employs an additional voltage V_{cm} [38]. Implementing the additional voltage $V_{\text{cm}} = V_{DD}/2$ will be difficult in ultra low-voltage designs [49].

Table 3.2: Features of the DAC switching schemes.

Parameter	Conven.	SplitMSB	Monotonic	Vcm-based
No. of capacitors	$2N+2$	$4N$	$2N$	$2N$
No. of C_u per array	2^N	2^N	2^{N-1}	2^{N-1}
CM variation	No	No	Yes	No

Figure 3.4: Dynamic comparator.

3.5 Comparator

The dynamic comparator commonly used in SAR ADCs consists of a differential pair loaded by a regenerative latch [50]. In some applications, a preamplifier is used before the dynamic comparator to attenuate the thermal noise and improve the speed. However, many recent works on SAR ADCs employ only the dynamic comparator to achieve moderate resolution with high power efficiency. Consider the dynamic comparator shown in Fig. 3.4. The operation of the dynamic comparator consists of two phases. During the reset phase (*clk* is LOW), the switches M_8 - M_{11} are ON and the outputs as well as the drain nodes of M_1 , M_2 are charged to V_{DD} . In this phase, the comparator is cleared of the previous state. Since the tail-current device M_3 is OFF, no current is drawn. During the evaluation phase (*clk* is HIGH), the input voltage difference at the differential pair causes their drain nodes to be discharged from V_{DD} . The cross-coupled inverters are initially OFF. The input transistors have different drain currents and this causes their drain nodes and the outputs to be discharged at different speeds. Finally, one of the cross-coupled inverters is activated. Strong positive feedback of the regenerative latch amplifies the output voltage difference until one output reaches V_{DD} and the other reaches ground. The important performance specifications of the comparator such as offset, noise, speed and metastability are discussed in the following subsections.

3.5.1 Offset

Offset in the dynamic comparator is caused by mismatches in the threshold voltages, device dimensions, and current factors μC_{ox} [51]. Capacitive load

imbalance on the output nodes also contributes to offset [52]. The offset voltage contribution is usually dominated by mismatches in the input differential pair of the dynamic comparator [51]. An obvious technique to reduce the offset voltage is to increase the size of the input pair. But this method entails high power consumption due to the parasitic capacitances in the input pair. Conventionally, a preamplifier is added before the dynamic comparator to reduce the input-referred offset. In such a case, the preamplifier provides sufficient gain to the comparator inputs so that the offset voltage is overcome. However, a high bandwidth preamplifier will consume large power. Also, attaining sufficient gain in the preamplifier becomes more challenging in scaled CMOS technologies. Intentional capacitor mismatch is often introduced at the comparator output nodes to cancel the input-referred offset [53].

3.5.2 Noise

Even though the dynamic comparator achieves high speed with excellent power efficiency, it suffers heavily from thermal noise. The input-referred noise of the comparator adds directly to the noise budget of the ADC and hence it should be minimized. Noise analysis of the dynamic comparator is rendered difficult by the fact that the operating regions are time-varying. Noise analysis in [54] uses stochastic differential equations. In [54], a number of design guidelines for mitigating noise have been outlined. A linear time-varying model is used in [55] to accurately predict the error probability. It is shown in [55] that the input-referred noise has the familiar kT/C form scaled by $(g_m/I_d)^{-1}$. It is important to note that many design techniques for reducing noise degrade the comparator speed [55].

3.5.3 Speed

The speed of the comparator is determined by the input differential voltage at the start of the regeneration phase as well as the regeneration time constant. The regeneration time constant is given by

$$\tau_{\text{reg}} = \frac{C_c}{g_{m,\text{INV}}}, \quad (3.7)$$

where C_c is the capacitive load on the regenerative nodes and $g_{m,\text{INV}}$ is the total transconductance of the inverter. The regeneration time constant is mainly determined by the transit frequency f_T of the CMOS process. However, τ_{reg} is also impacted by the sizing of the devices in the comparator [56]. In a SAR ADC, the comparator should be fast enough to resolve a differential input voltage of $LSB/2$ within the allotted time under all PVT conditions.

3.5.4 Metastability

Metastability occurs when the input differential voltage is so small that the latch cannot produce acceptable logic levels within the requisite time. Metastability can be caused by low speed of the comparator and/or inadequate time allotted to the regeneration phase. Since the comparator outputs have not attained the proper logic levels, the succeeding digital logic will interpret them differently leading to large errors in the A/D conversion. For SAR ADCs, [57] provides analysis of metastability errors and derives the signal-to-metastability-error ratio (SMR).

3.6 Conclusion

It is seen that the SAR ADC is able to achieve high power efficiency in modern CMOS technology nodes. SAR ADCs are being preferred over pipelined ADCs in many medium-resolution, high-speed applications. Time-interleaved SAR ADCs have helped to push conversion rates beyond 1 GS/s. Designers are also adapting the SAR ADC for low voltage, ultra low power applications. However, achieving the targeted performance relies on the robust design of the analog and mixed-signal blocks such as the S/H, DAC and comparator.

Conclusions and Future Work

4.1 Conclusions

It is seen that CMOS process scaling presents several challenges to the design of high performance analog, and mixed-signal circuits. The reduced supply voltage in advanced CMOS process technologies leads to insufficient gate overdrive voltage for analog switches and reduced dynamic range for amplifiers. Advanced switch topologies such as bootstrapped switches, and clock boosted switches are needed to achieve linearity under reduced supply voltages. Multistage amplifiers are increasingly employed in AFEs, and data converters to achieve sufficient DC gain. Consequently, amplifier topologies and power-efficient frequency compensation schemes suited for low-voltage implementation are being proposed. The SAR ADC has proven to be a power-efficient and scaling-friendly architecture for ADCs. The absence of high gain opamps in the SAR ADC helps to achieve good power efficiency. Energy-efficient DAC switching schemes and the use of custom designed unit capacitors have enabled SAR ADCs to achieve state-of-the art power efficiency at moderate resolutions (8-11 bits) and sampling rates of several tens of MHz.

In Part-II of this thesis, **Paper A** describes an AFE designed in 40 nm CMOS that utilizes two-stage amplifiers incorporating a power-efficient compensation scheme. **Paper B** investigates the frequency compensation of high-speed, low-voltage CMOS multistage amplifiers. Four-stage and three-stage amplifiers designed in 65 nm and 40 nm CMOS are utilized to compare two compensation schemes proposed in literature. **Paper C** describes a power-efficient reference voltage buffer implemented in 180 nm CMOS for a 10-bit 1 MS/s SAR ADC which is intended to be used in a fingerprint sensor. The design and implementation of a 10-bit 50 MS/s SAR ADC in 65 nm CMOS with a high-speed, on-chip reference voltage buffer is presented in **Paper D**.

4.2 Future Work

The design of the following ADCs are planned as future activities:

- Design and implementation of an ultra low-power SAR ADC in 65 nm CMOS for wireless sensor networks.
- Design and implementation of a power-efficient 12-bit 100 MS/s ADC in 65 nm CMOS for a wireless communication SoC.

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Part II

Publications

Publications

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