The design of an all-digital VCO-based ADC in a 65 nm CMOS technology
The design of an all-digital VCO-based ADC in a 65 nm CMOS technology

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Sammanfattning | Abstract
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In this thesis work, the VCO-based ADC design, falls under the category of time-based ADCs which consists of a VCO and an appropriate digital processing circuitry. The employed VCO is used to convert a voltage-based signal into a time signal and thereby it also acts as a time-based quantizer. Then the resulting quantized-time signal is converted into a digital signal by an appropriate digital technique. After different architecture exploration, a conventional VCO-based ADC architecture is implemented in a high-level model to understand the characteristic behaviour of this time-based ADC and then a comprehensive functional schematic-level is designed in reference with the implemented behavioural model using cadence design environment. The performance has been verified using the mixed-levels, of transistor- and behavioural-levels due to the greater simulation time of the implemented design.

ADC’s dynamic performance has been evaluated using various experiments and simulations. Overall, the simulation experiments showed that the design was found to reach an ENOB of 4.9-bit at 572 MHz speed of sample per second, when a 120 MHz analog signal is applied. The achieved peak performance of the design was a SNR of 40 dB, SFDR of 34 dB and an SNDR of 31 dB over a 120 MHz BW at a 1 V supply voltage. Without any complex building blocks, this VCO-based all-digital ADC design provided a key feature of inherent noise shaping property and also found to be well compatible at the deep submicron region.
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This thesis explores the study and design of an all-digital VCO-based ADC in a 65 nm CMOS technology. As the CMOS process enters the deep submicron region, the voltage-domain-based ADCs begins to suffer in improving their performance due to the use of complex analog components. A promising solution to improve the performance of an ADC is to employ as many as possible digital components in a time-domain-based ADC, where it uses the time resolution of an analog signal rather than the voltage resolution. In comparison, as the CMOS process scales down, the time resolution of an analog signal has found superior than the voltage resolution of an analog signal. In recent years, such time-domain-based ADCs have been taken an immense interest due to its inherent features and their design reasons.

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Acronyms

AC  Alternating Current
ADC  Analog-to-Digital Converter
CLA  Carry-Look-ahead Adder
CMOS  Complementary Metal-Oxide Semiconductor
CPA  Carry-Propagate Adder
CSA  Carry-Save Adder
CSEL  Carry-Select Adder
DAC  Digital-to-Analog Converter
dBc  decibels relative to the carrier
DC  Direct Current
DEM  Dynamic Element Matching
DFF  D Flip-Flop
DNL  Differential Non-Linearity
ENOB  Effective Number of Bits
FDC  Frequency-to-Digital Converter
INL  Integral Non-Linearity
LSB  Least-Significant Bit
MSB  Most-Significant Bit
OSR  Oversampling Ratio
PVT  Process Voltage Temperature
RCA  Ripple Carry Adder
RMS  Root Mean Square
SFDR  Spurious Free Dynamic Range
SNR  Signal-to-Noise Ratio
SNDR  Signal-to-Noise and Distortion Ratio
VCO  Voltage-Controlled Oscillator
XOR  Exclusive-OR
Chapter 1

Introduction

In modern wireless communication systems, data converters play a major role in the conversion of electrical signals. In the whole world, analog signal is the most common signal which the human being can sense that physical signal. The analog signal has a continuous-amplitude and continuous-time data. Instead, the digital signal has a discrete-amplitude and discrete-time data. The data converters act as interfaces between the analog and digital. The main purpose of the data converter is to either convert an analog signal into a digital signal or vice versa. In the past years, there are several techniques that have been studied and developed to implement high-speed, low cost, high-accuracy data converters. The data converters are implemented in two ways 1) Analog-to-digital conversion (ADC) 2) Digital-to-analog conversion (DAC). The ADC converts the continuous-time analog signal into an equivalent discrete digital signal. The conversion takes place by sampling the analog signal and then quantized the sampled analog signal. And this digital signal will then convert back to an analog signal by DAC. In the emerging world, the applications of the converters have been increased rapidly, such as digital imaging systems, high quality video system and high performance digital communication systems, which demand the converters to design with high performance.

Most of the conventional ADCs were naturally concentrated on high performance analog components in order to achieve the desired performance. But these ADCs face different difficulties while designing in deep submicron processes. The main disadvantages of using the analog components in the ADC design are as follows.

✓ It is very difficult to quantize accurately in the voltage-domain when the voltage dynamic range decreases.

✓ In deep submicron technologies, the size and supply voltage shrinks, which leads to limited signal swing.

✓ The signal-to-noise ratio will be reduced with lower signal swings.
The difficulty level is higher due to the usage of a large number of analog components while designing in deep submicron complementary metal-oxide semiconductor (CMOS) technology. By keeping these inherent drawbacks in perspective, a flexible system and method are needed as an alternative to enhance the performance. Each ADC has specific characteristics and the design of such a high performance ADCs should be extremely important.

As technology scales, the functionalities of analog components were forced to move towards digital in order to increase their performance. The problems occurred in the digital circuits are minimal and it is easier to eliminate. When technology scales down, the parasitics will be reduced due to the smaller dimension which leads to faster switching; that helps to achieve high resolution. The digital circuits have vast advantages they are highly immune to noise, huge reduction in the design cost, low power consumption, area efficient, etc. In the past decades, analog ADCs such as flash ADC, pipeline ADC are very popular, but their progress in the improvement was not quite comparable to that of digital circuits. The old technologies make use of a large supply voltage (i.e., 2.5 V, 3.3 V and 5 V) in order to achieve a high signal-to-noise ratio. But in a deep submicron process, the available voltage headroom is slightly small with a low supply voltage (i.e., less than or equal to 1.5 V), so the representation of a signal in the time-domain will be more efficient.

### 1.1 All-digital ADC

The new approach of designing an all-digital analog-to-digital converter is an attempt to minimize the RF and analog components as much as possible. So the voltage-controlled oscillator (VCO)-based analog-to-digital converter has gained more popularity among the researchers due to the presence of highly digital components and time-based signal processing. As shown in figure 1.1, the VCO-based ADC’s input analog voltage is first converted into the time-information or time-domain by the use of VCO and then quantization takes place in time. Dealing with time-domain signal processing instead of voltage or current will help to achieve high resolution.

### 1.2 Historical background

In 1999, the idea of the VCO-based quantizer was first proposed and applied in a sigma-delta ADC to improve resolution. Figure 1.2 shows the first architecture of the VCO-based quantizer utilized in a sigma-delta ADC, where a simple digital reset counter used as a time quantizer. This digital reset counter counts the number of VCO transitions within a sampling period, which will represent the VCO’s input analog voltage. It was derived that there is an increase in resolution as a function of oversampling ratio and VCO tuning frequency. Also, the resolution would further increase in the use of multi-phase VCO. The VCO-based quantizer has an inherent first-order noise-shaping property. As opposed to the conventional
1.2 Historical background

Voltage-based quantizer, the VCO-based quantizer has an additional noise-shaping property to enhance the sigma-delta ADC.

The drawbacks of this architecture are the errors occurred due to missing VCO transitions per count caused by the reset operation in the counter and also the occurrence of harmonic distortion due to the non-linearity of the VCO tuning curve [2]. The challenge in designing this architecture is the feedback DAC, since the design gets complicated due to the requirements for non-linearity and mismatch errors and also the dynamic element matching (DEM) leads to one-bit sigma-delta architectures. In the case of multi-bit output, a complicated multi-bit feedback DAC is required. In 2000, a proper solution was found on by replacing the feedback DAC into a frequency detector in the feedback loop, which eliminates the DEM and mismatch errors [3]. But due to the lack of interest in this concept, a further progress did not make. In 2006, the design of ring VCO is used to improve quantizer resolution which provides multi-phase outputs. As shown in figure 1.3 [4], each VCO output requires a counter and the result is then added to improve resolution.
In order to develop a bandpass ADC, a time-interleaved VCO-based quantizer was introduced around the year 2008-2009 to increase the order of noise-shaping property, see figure 1.4 [5] [6].

In the year 2009, another new architecture was introduced with an idea of sigma-delta modulator but without using feedback DAC and the complicated analog circuits. The architecture was designed to utilize the noise-shaping properties of the VCO-ADC. As shown in figure 1.5, the VCO was placed at the front end of the sigma-delta modulator. Except charge pump (CP), this architecture consists of high digital components and gives one more order of noise-shaping characteristics [15]. In the recent years, several techniques have been introduced in standard
CMOS technologies to enhance the circuit performance.

**Figure 1.5.** Second-order noise-shaping VCO-based quantizer.

## 1.3 Thesis Method

The motivation and background study has been briefly described in the preceding sections. This thesis, an all-digital ADC project is a part of another research project, all-digital RF transceivers. The design specifications were targeted at IF frequencies and not the actual RF front-end design. The aim of the work is to understand the functional working of the VCO-based ADC design along with its inherent features and subsequently implement the design using advance CAD tool.

The work method involves with the preliminary study on various architectures and the choice of suitable architecture, followed by implementing the suitable model using verilog-A code and down to schematic design using cadence design environment, i.e., the work flows with a top-down design methodology. The implemented design is simulated with an appropriate design setup and the desired results were captured through comprehensive analysis and different verification methods. The project targets to implement the design through employing possible components in digital domain with basic structures and to deliver the design with high resolution all-digital ADC. The thesis organization with concise explanation is given in the coming section.

## 1.4 Thesis organization

This thesis work is organised with several chapters. The brief introduction to the contents of each chapter is shown below.

Chapter 2 describes the basic understanding of the fundamental concepts of analog-to-digital conversion, the errors involved during the conversion and also the performance metrics for evaluating the ADC performance.

Chapter 3 describes the working principle of different traditional ADCs and the introduction discussed with the glimpse of advantage in using the time-based ADC over the traditional ADCs.
Chapter 4 presents the principle and the inherent characteristic of a VCO-based ADC and towards the end of the chapter, different topologies and limitations on every topology had been precisely given.

Chapter 5 provides the individual block-level introduction to the chosen VCO-based ADC architecture.

Chapter 6 deals with the basics of an oscillator, followed by a clear study of the choice of voltage-controlled oscillator and in Chapter 7, the design, implementation and simulation results of the opted VCO and the differential to single-ended design has been presented.

Chapter 8 concentrates on the design and analysis of the frequency-to-digital conversion, followed by discussion of various adders and a suitable adder design for the opted VCO-based ADC architecture has been implemented and analysed.

In Chapter 9, different experiments and simulation on the VCO-based ADC design in behavioural-level as well as circuit-level has been comparatively verified and reported. At the end of the chapter dynamic performance of the VCO-based ADC has been tabulated.

Chapter 10 describes about the conclusions and future work of the VCO-based ADC.

1.5 Conclusions

This chapter has given a short introduction, thesis organization and historical background studies of the VCO-based ADC. In the following chapters, we are going to see the detailed analysis on the operation and design of the VCO-based all-digital ADC, which helps us to understand deeply about the working principle of VCO-based architecture.
Chapter 2

Fundamentals of ADCs

This chapter deals with the study of the fundamental concepts of ADC and its performance metrics. The basic concepts involved in the converters conversion process and its violation issues are precisely described. The quality of the converters conversion is measured using certain metrics named as performance metrics. Common quantified errors while measuring the performance of ADC have been better illustrated such that any reader could get a clear idea of these described metrics. To start with, the following section will describe about the fundamental concepts of ADC.

Analog-to-Digital Converters (ADC) are used to convert the input analog signal into an output digital form, i.e., the input signal, usually in the form of a voltage or current and continuous in time and amplitude is converted into an output signal which is discrete in time and amplitude. This conversion process consists of two distinct steps, they are sampling and quantization. The sampling process is performed by representing a continuous signal into a discrete or continuous series of samples in time, whereas the quantization process is representing a continuous signal into a discrete or continuous series of sample in amplitude.

The block diagram representation of ADC is illustrated in Figure 2.1, where an input analog signal $v(t)$ is first converted into a discrete-time signal $v'[k]$ using a sampler and then it is quantized into a digital output signal $d[k]$. The sampling
process can be performed either in a discrete-time or in a continuous-time series of samples, a brief understanding of both these techniques are narrated in [1].

2.1 Sampling theorem and aliasing

According to Nyquist sampling theorem, a signal can be reconstructed from its periodic samples only if the sampling frequency is greater than or equal to twice the highest frequency of the signal. Consider an input signal with a highest frequency $f_m$ and a sampling frequency $f_s$, then according to Nyquist-rate the sampling frequency is given as

$$f_s \geq 2f_m$$ \hfill (2.1)

If the sampling signal frequency is lower than twice the input signal frequency, i.e., $f_s < 2f_m$, then an indistinguishable input signals can be reconstructed using the same set of samples. Such an occurrence is called aliasing. In order to reconstruct a given input signal, a minimum sampling rate is called Nyquist-rate. The Nyquist-frequency is known as the highest frequency component that can be reconstructed for a given sampling rate.

![Figure 2.2. Two different sinusoidal signals that fit with the same set of samples due to under-sampling is illustrated in time-domain.](image)

From figure 2.2, it is clear that the two sinusoidal fits into the same set of samples collected, because the highest frequency sinusoidal has not been properly sampled due to the violation in the Nyquist-rate criterion. Hence, another low frequency sinusoidal could fit with the same samples has been interpreted. This can be better viewed in the frequency-domain. Figure 2.3a) shows the frequency-domain representation of an input analog signal with the highest frequency component $f_m$ and figure 2.3b) represents that the signal is sampled at sampling frequency which is greater than twice the input signal. It is known that the original two sided input signal spectrum can be viewed at every multiples of $f_s$ as...
shown. Now considered that the sampling frequency has violated the Nyquist-rate criterion, i.e., if the sampling frequency is less than twice the input frequency, in that case the spectrum is viewed as shown in figure 2.4. The spectrum shows the overlap of spectral images with each other, which relatively lead to a phenomenon called aliasing.

**Figure 2.3.** Sampling in frequency-domain, (a) Input analog signal $f_m$, (b) Analog signal sampled at frequency $f_s$.

**Figure 2.4.** Spectral overlap due to under-sampling is illustrated in frequency-domain.
2.2 Quantization

As discussed before, the quantization involves with the discrete values of amplitude from a continuous analog signal using the finite precision of samples. Figure 2.5a [1], illustrates the ideal transfer characteristic of the three-bit quantizer and its corresponding quantized error function. The minimum successive voltage difference at which the input voltage are quantized is given by $\Delta V$ and that corresponds to the weight of one LSB. For such a conversion, the amplitude of error ranges from zero to $\Delta V$ Volts. The transfer characteristic of three-bit quantizer can be slightly re-mapped as shown in figure 2.5b [1], so that the maximum amplitude of error is reduced from $\Delta V$ Volts to $\Delta V/2$ Volts and now the change in the amplitude of error range is $-\Delta V/2$ Volts to $\Delta V/2$ Volts. This type of mapping is referred as half-LSB-compensated transfer curve.

The quantization noise is referred as the error produced by the quantizer. In reality, a stochastic approach is applied, since the quantization error varies with the input voltage and it could be modelled as a random variable, uniformly distributed between $-\Delta V/2$ Volts to $\Delta V/2$ Volts. The probability density function for both the quantizer will be a constant value as illustrated in figure 2.6 [8]. The rms value of the quantized error voltage for an uncompensated quantizer is expressed as

$$V_{error_{rms}} = \sqrt{\frac{1}{\Delta V} \int_{0}^{\Delta V} V_{error}^2 dV_{in}} = \sqrt{\frac{1}{\Delta V} \int_{0}^{\Delta V} V_{in}^2 dV_{in}} = \frac{\Delta V}{\sqrt{3}} (2.2)$$
Similarly, the rms value of the quantized error voltage for a half-LSB-compensated quantizer is expressed as

\[
V_{error_{rms}} = \sqrt{\frac{1}{\Delta V} \int_{-\Delta V/2}^{\Delta V/2} V_{error}^2 dV_{in}}
\]

where \( V_{in} \) is the input analog voltage. Quantization noise is the only noise present in an ideal ADC. The resolution of ADC is closely related to the minimum successive voltage difference (quantization step or \( \Delta V \)) and the input voltage range. That is, if the input voltage range is resolved uniformly into \( K \)-levels, then the resolution of an ideal ADC can be given as

\[
Resolution_{ideal} = N_{ideal} = \log_2 K \text{bits}
\]  

For an ideal ADC, the signal-to-noise ratio can is given as

\[
SNR_{ideal} = 20 \log_{10} \frac{\text{Signal}_{rms}}{\text{Noise}_{rms}}
\]

where \( \text{Signal}_{rms} \) is the rms amplitude of signal which can be obtained by considering a full-scale sin wave signal as given by

\[
v(t) = \frac{2^{N_{ideal}} \Delta V}{2\sqrt{2}} \sin(2\pi f_m t)
\]

where \( f_m \) is the signal frequency and \( t \) is the time. The rms value of such a sin wave signal is

\[
v_{rms}(t) = \frac{2^{N_{ideal}} \Delta V}{2\sqrt{2}}
\]

by replacing the equation obtained in

\[
SNR_{ideal} = 20 \log 10 \frac{2^{N_{ideal}} \Delta V}{\Delta V} \frac{\Delta V}{\sqrt{12}}
\]
\[ SNR_{ideal} = 20 \log_{10}(2^{N_{ideal}}) + 20 \log_{10}\left(\sqrt{\frac{3}{2}}\right) = (6.02N_{ideal} + 1.76) \text{dB} \quad (2.9) \]

In practical aspects of an ADC, there are several other factors to be considered in order to evaluate the performance of an ADC. They are described in the following sections.

2.3 Performance metrics

The performance metrics used in quantifying the error during the converters conversion process has been given by static and dynamic analysis. The static performance of the ADC is measured by applying a DC input (usually a slow ramp signal) whereas in the dynamic performance, it is measured by applying an AC input (usually a sinusoidal signal). The performance measurements are application oriented where different measurements are required for different application in characterizing the performance of the ADC. In the following section the most common performance metrics involved in static and dynamic analysis have been described.

2.3.1 Static performance metrics

The static performance evaluation of an ADC involves, an application of DC input signal to the ADC. While performing a static performance evaluation, an actual ADC transfer characteristic deviates from an ideal transfer characteristic. This precise measurement towards the variation in the transfer function of practical ADC is known as a static error. Some static errors are discussed in the following section.

Offset error and gain error

Offset and gain errors [1] are measured under the assumption, that the ADC transfer function is linear. Therefore, for a non-linear ADC transfer function, it must involve with some method to approximate the transfer function to a linear or a straight line. This linearity can be obtained by two methods, namely, an end-point method and the best-fit method. The linearity approximation of an ideal ADC is estimated that, it should pass through either zero or a pre-defined value.

Offset error of an ADC is defined as a constant deviation of the measured transfer function from an ideal line, at the first output code. It is clearly shown in figure 2.7 [1].

Gain error of an ADC is referred as a deviation in the slope of the measured response to the slope of the ideal response [9].

Differential Non-Linearity

Differential non-linearity (DNL) is defined as the difference between the width of the actual code and the width of the ideal code. For a range of analog input
2.3 Performance metrics

Figure 2.7. Measurement of offset and gain error.

Figure 2.8. DNL error in an ADC transfer function.

voltage values there produces a digital output code and that is called the actual code width. Figure 2.8 illustrate the DNL measurement.
In an actual code width, for a successive change in the range of input analog voltage, usually that change is denoted in the output digital code as $\pm 1\text{LSB}$. If the lowest digital code-width is zero, then it is denoted as the missing code, it is also illustrated in figure 2.8.

### Integral Non-Linearity

![Figure 2.9. INL error in an ADC transfer function.](image)

INL [1] is defined as the difference between the measured transfer function to the adjusted ideal transfer function. An adjusted ideal transfer function is obtained by the same methods, which is involved in obtaining the measured transfer function from the offset and the gain error. Figure 2.9 illustrate the INL measurement.

#### 2.3.2 Dynamic performance metrics

The most common analysis for evaluating the performance of the ADC is through applying a sine wave input signal. Then the output samples are analysed in the frequency-domain in order to verify the spectral purity of the applied input signal at the output. In this section, the dynamic performance metric has been evaluated by considering the applied signal as a full-scale wave.

### Signal-to-Noise Ratio (SNR)

It is defined as the ratio of the rms amplitude of the output signal to the rms noise power [1]. Where, the noise power is calculated by excluding the harmonics of the output signal and by including only the noise terms.
2.3 Performance metrics

SNR of the ADC is mathematically expressed as

\[ SNR = 10 \log_{10} \left( \frac{P_{\text{signal}}}{P_{\text{noise}}} \right) = 20 \log_{10} \left( \frac{\text{Signal}_{\text{rms}}}{N_{\text{rms}}} \right) \] (2.10)

**Total Harmonic Distortion (THD)**

It is defined as the ratio of the rms amplitude of the output signal to the rms power of the harmonic components [1]. Generally the most-significant harmonics are the first five harmonic components or the required harmonic component is taken for manipulation.

THD of the ADC is mathematically expressed as

\[ THD = 20 \log_{10} \left( \frac{\text{Signal}_{\text{rms}}}{D_{\text{rms}}} \right) \] (2.11)

**Signal-to-Noise-and-Distortion Ratio (SNDR)**

It is defined as the ratio of the rms amplitude of the output signal to the rms power of all other spectral components [1]. Where, the spectral components include both the noise terms and the harmonic components and excludes the DC. Since the noise and distortions are considered in the SNDR relation, this metric is considered as the one of the effective performance metrics in evaluating the ADC.

SNDR of the ADC can be mathematically expressed as

\[ SNDR = 20 \log_{10} \left( \frac{\text{Signal}_{\text{rms}}}{N_{\text{rms}} + D_{\text{rms}}} \right) \] (2.12)

**Spurious-Free Dynamic Range (SFDR)**

It is defined as the ratio of the rms amplitude of the output signal to the rms power of the strongest spurious signal in the spectrum. Where, the spurious signal denotes the noise and that noise can be anything (regardless of whether it is harmonics components or noise term) apart from the fundamental.

SFDR of the ADC can be graphically viewed in figure 2.10 [9].

**Effective Number of Bits (ENOB)**

It is also considered as one of the most important metrics in the ADC specification. ENOB is usually obtained by applying the SNDR in the place of \( SNR_{\text{ideal}} \) (which is obtained in the equation 2.9), then the equation is solved for \( N_{\text{ideal}} \).

ENOB of the ADC can be mathematically expressed as

\[ ENOB = \frac{SNDR - 1.76dB}{6.02} \] (2.13)
2.4 Conclusions

This chapter has given an elaborate definition on the fundamentals of ADC and their performance measures. Each measurement has a greater significance in accordance with the application at which the ADC is involved. There are various types of ADC in which all the ADCs performances can be verified and analysed using these common metrics. And the next chapter will give a study on classification of ADCs.
Chapter 3

Classification of ADCs

This chapter discusses about the different types of ADCs and their approaches at which it differs from each other have been present by describing its working principle. ADCs such as Flash ADC, Successive-Approximation register ADC, Pipelined ADC and sigma-delta ADC have been presented. At the end of the chapter the time-based ADC has been introduced and trendily compared with the other ADCs. The time-based ADC has been mathematically and conceptually explained in the next chapter.

3.1 Classical ADC architectures

ADCs are generalized, based on the relationship between the signal frequency $f_m$ and the frequency at which the signal is sampled $f_s$. ADCs that have the input signal $f_m$ close to half the sampling frequency $f_s$ are called Nyquist ADCs and ADCs that have input signal much less than half the sampling frequency $f_s$ are called oversampled ADCs. The classical ADC architectures explained in the following section can be implemented in both the configurations, i.e., either as Nyquist-rate ADCs or as oversampled ADCs.

3.1.1 Flash ADC

Flash ADCs are the fastest converters to transform an analog signal to a digital sequence and are also known as parallel converters. The flash ADCs can be generalized into two groups namely: voltage mode flash ADC and current mode flash ADC. The generalization depends on the nature of input signal (voltage or current) that needs to be digitized. The current mode digitization is usually accomplished with the help of current mirrors and current comparators while the typical voltage mode digitization can be achieved with the help of resistive divider circuits. The flash ADCs are suitable for applications requiring very large bandwidths and are the most straightforward approach to ADC design. However, these ADCs consume more power than other ADC architectures and can only be suited for
low-resolution applications. Typical applications include data acquisition, satellite communication, radar processing, sampling oscilloscope and high-density disk drives.

The following section describes the traditional voltage mode flash ADC design. The integral part of the flash ADCs are the high-speed comparators and the thermometer to binary decoder (TC to BC). The flash ADC are formed by cascading high-speed comparators. Figure 3.1 shows a classical flash ADC block diagram.

![Figure 3.1. Block diagram of a classical flash ADC.](image)

To design an N-bit converter the flash circuit employs $2^N - 1$ high-speed comparators and a resistive divider circuit with $2^N$ resistors. The reference voltage $V_{\text{ref}}$ applied to resistive divider circuit is divided into different reference voltage levels after every resistor in the divider path. The reference voltage levels across the divider path depends on the resistance offered by the resistors. Thus, suitable resistance values have to be fixed for the resistors across the divider path. It is also advisable to check whether the reference voltages across the divider path falls within the input signal levels (peak-to-peak). The divided reference voltage levels and the $V_{\text{in}}$ are the inputs to the high-speed comparators. $V_{\text{in}}$ represents the input...
signal that needs to be digitized. The function of each comparator is to produce 'logic high' or \textit{vdd} or 'logic 1', when the analog input signal \( V_{in} \) is greater than the reference voltage and if the condition fails then the comparator outputs 'logic low' or \textit{gnd} or 'logic 0'. As an example, if the input signal \( V_{in} \) is between \( V_{x4} \) and \( V_{x3} \), then the comparators from \( X_1 \) to \( X_4 \) produce 'logic 1' and the remaining comparators produce 'logic 0'. The point at which the \( V_{in} \) becomes smaller than the comparator reference voltage levels is referred to as transition point, i.e., transition from 'logic high' to 'logic low'. The output logic levels from the high-speed comparators represents the thermometer codes. These codes act as inputs to thermometer to binary converter (TC to BC). The mathematical function of TC to BC is to add the number of 'ones' or 'logic high' into a decimal value and change it exactly to its binary equivalent. These binary codes are the digitized form of the input signal \( V_{in} \). To ensure that the analog-to-digital conversion is done properly, apply the output binary codes of ADC to a digital-to-analog converter (DAC) and check whether the reproduced signal is same as \( V_{in} \).

Some of the non-linearities that affects the function of flash ADC are metastability, sparkle codes, input offset voltage, clock jitter, etc. Metastability is a state were the comparator digital output is neither at 'logic high' or at 'logic low'. The digital output can be in-between these two states. One way to reduce metastability is to use gray-code encoding technique. Sparkle codes are wrong codes, generated at the comparator output. As an example, if the comparators correct output is 000011 then due to incorrect timing of the comparator, it may cause the output to be 001011, here the out-of-sequence 1 is called a sparkle. The sampling clock applied to ADC must be of low jitter clock otherwise the SNR can be degraded. The input offset voltage error is due to threshold voltage or transconductance parameter mismatch between identical transistors. It is nominal voltage applied at the input terminals to balance the comparator.

**High-Speed Comparators for Flash ADC**

Usually comparators are divided into two groups namely: Open-loop comparators and Regenerative comparators. The open loop comparators are traditional operational amplifiers without compensation. These comparators are not used in high-speed designs since their response time are high. Regenerative comparators consists of low-gain amplifier stage followed by a latch stage. The main advantage of regenerative comparators is the faster response time thereby making them suitable for high-speed applications. The low-gain amplifier stage has the ability to reduce the latch offset voltage by a considerable amount and eliminates the kick back effect from latch stage. To understand kick back effect, it is necessary to know about the function of latch stage. The latch stage operates in two phases namely: track phase and latch phase. The output follows the input during the track phase and comparison operation is done during latch phase. Kick back is the extra charges that are leaked into low-gain amplifier stage when the comparator makes the transition from track phase to latch phase. The faster response time of the regenerative comparator is mainly due to the positive feedback mechanism formed during the latch stage. Thus, regenerative comparators are most suited for
flash ADC design.

The major trade-off with flash ADC is the die size, cost and power increases with resolution. Thus, flash ADCs are usually limited to resolution of 8-bits (255 comparators required). For every bit increase the size of the ADC almost doubles. The resistor tolerance level and component matching also limits the flash ADCs resolution. Nevertheless, their high-speed operation can be exploited in applications like radar, optical communication links, wide-band receivers were the sample rate is in gigahertz. Also, flash ADCs of smaller size can easily be embedded in advanced ADC techniques like sigma-Delta ADC, pipelined ADC, etc.

### 3.1.2 Successive-Approximation Register ADCs (SAR ADC)

The most popular ADCs in the current environment that offers medium to high resolution with a sample rate below 5 mega samples per second (5 MSps) is the successive approximation register ADCs. High performance, low-power consumption, 8- to 18-bit resolution at sample rate below 5 MSps are the key features that makes the SAR ADCs, the architecture of choice in today’s ADC market. Typical applications include data signalling acquisition, portable battery powered instruments, industrial controls, etc. The SAR ADCs accomplishes analog-to-digital conversion by means of binary search algorithm technique. The binary search algorithm searches for the position of a given value within a array that is sorted. At each cycle, the algorithm makes a comparison between the given value with the value present in the middle element of the array that is in sorted order. The search continues until the given value and value present in the middle element matches. If both values are matched then corresponding output is produced and the algorithm repeats itself for the next given value. But if the given value doesn’t match with the middle element of the array and if the given value is less than the value of the middle element, then the algorithm repeats itself on the array elements that are to its left thereby neglecting the elements in the right of the array. This process is continued until the given value matches with the middle value of the sorted array. On the other hand, if the given value is greater than the value present in the middle element of the array then the algorithm performs its operation on the right hand side of the array. Since the binary search algorithm halves the number of elements of the array in each iteration, the time taken to locate a given value in the sorted array is represented in logarithmic time. Similarly, in the case of SAR ADCs, though the internal circuitry runs at some megahertz, the SAR ADCs sample rate is only a fraction of that number.

The integral part of the SAR ADCs are: Track-and-Hold amplifier, Comparator, DAC and SAR block consisting of control logic and N-bit register. Figure 3.2 shows the block diagram of a SAR ADC. Binary search technique is followed by first setting the N-bit register to mid-scale (i.e., '100000' MSB is set to 1) thereby fixing the DAC output voltage $V_{DAC}$ to $V_{REF}/2$, here $V_{REF}$ is the reference voltage of the ADC. The Track-and-Hold amplifier is used for AC signal conversion. The amplifier freezes the input signal $V_{IN}$ during the conversion process. This action is required since the AC input to the comparator has to be of constant value for the comparison to take place. Now if $V_{IN}$ is less than $V_{DAC}$, the comparator
produces logic low. Thus, the MSB of the N-bit register is updated to 'logic 0'.

![Simplified N-bit SAR ADC architecture.](image)

Figure 3.2. Simplified N-bit SAR ADC architecture.

Now the control logic selects the next bit in the register and the conversion is carried out repeatedly. This operation continues all the way down to LSB. Once the conversion gets complete, the bits that remain in the register represents the N-bit digital output.

The DAC and the comparator are the critical components of SAR ADCs. Most of today’s SAR ADCs employs a capacitive DAC at its feedback path. This is because a capacitive DAC offers inherent track and hold function. The analog output voltage generated from a capacitive DAC is based on charge redistribution principle. The linearity of the DAC is of major concern since the overall SAR ADCs linearity depends on the performance of the DAC. Also, linearity of the SAR ADCs is limited by inherent component-matching accuracy. Usually SAR ADCs with more than 12-bits of resolution often require some form of calibration or trimming circuitry. Speed and accuracy are the major requirements of the comparator used in SAR ADCs. The comparator offset is usually reduced using suitable offset-cancellation technique. Noise is a major issue in the comparator thus the input referred noise of the comparator is usually designed to be less than 1 LSB. Above all, the comparator has to detect minimum difference in voltages between \( V_{DAC} \) and \( V_{IN} \).

Low power consumption, high resolution and accuracy are the major advantages of SAR ADCs thereby making them suitable for integration with larger systems. However, speed is a major issue in SAR ADCs and they cannot be used for applications with high sample rates. Also, the linearity of the SAR ADCs is directly related to the accuracy of the DAC and the comparator within the system. Despite of their limitations, SAR ADCs is the best choice for applications with sample rates less than 5 MSps.
3.1.3 Pipelined ADC

Pipelined ADCs are most suited for applications with a sample rates ranging between few mega samples per second (MSps) to 100 mega samples per second (MSps). The resolution obtained from pipelined ADCs will be in the range of 8- to 16-bits. Typical applications include digital receivers, base stations, digital video HDTV, cable modems and fast Ethernet.

![Block diagram of a pipelined ADC with four 3-bit stages.](image)

Figure 3.3. Block diagram of a pipelined ADC with four 3-bit stages.

Figure 3.3 shows the block diagram of a typical 12-bit pipelined ADC with four 3-bit stages. The block diagram in the dashed line of figure 3.3 shows the schematics of each stage of pipelined ADC. The integral part of each stage are, the Sample-and-Hold Amplifier, 3-bit ADC, 3-bit DAC.

The Sample-and-Hold Amplifier works in two phases namely: sampling phase and hold phase. During sampling phase the input $V_{IN}$ is sampled at a given interval and at the next phase the sampled data is held constant. The sampled and held data is then quantized by 3-bit flash ADC. The 3-bit DAC converts the quantized flash ADC output to an analog value which is subtracted from the input using a difference amplifier. The difference amplifier output known as the residue is gained by a factor of four and sent to the next stage. Now the gained up residue is processed through the pipeline stages thereby producing 3-bits per stage. The gained up residue from the last stage is processed through the 4-bit flash ADC which is used to resolve the last 4 LSB bits. Since the bits from each stage are determined at different time points, bits belonging to the same sample has to be time aligned. This can be done using shift registers. Now the time aligned output
is sent to digital error correction block for further calibration.

Pipeline action is accomplished at all stages of the design, i.e., when stage 3 outputs the residue to stage 4 at a given time interval, then at the same interval it starts processing the next sample from Sample-and-Hold embedded within the stage 3. High throughput from pipelined ADCs is because of the pipelining action.

Pipelined ADCs are mostly used in digital communication were dynamic performance (SNR, SFDR, SNDR) is of great importance when compared to static performance (Differential non-linearity, Integral non-linearity). They are used in applications with sample rates ranging from few MSps to 100 MSps. As the resolution and speed increases, linearity becomes a major concern.

3.1.4 Sigma-delta ADC

Sigma-delta ADCs are low in cost and it is also one of the oldest conversion techniques that has been in existence for many years. The converter has become practical in today’s environment due to recent technological advances. These converters provide high dynamic range and flexibility in converting input signals with lower bandwidth. Typical applications include consumer and professional audio, industrial weight scales, precision measurement devices, etc. Sigma-delta ADCs can be classified into three categories based on nature of signal sampling. There are two types of signal sampling technique namely Discrete-time sampling which can be implemented using Switched-Capacitor or Switched-Current Integrator and Continuous-time sampling implemented using Operational Transconductance Amplifier (OTA). This section explains the important features and functions of Sigma-delta ADC.

Before getting into working principle of Sigma-delta ADC, it is necessary to understand few important concepts. They are Noise shaping, Oversampling, Filtering and Decimation. Noise shaping is an act of shaping the noise or pushing the noise into higher frequencies so that it can be easily removed by a digital filter. This is achieved using a noise-shaping filter or integrator inside the sigma-delta loop. Oversampling is one of the key characteristics of Sigma-delta ADC. It helps to reduce the quantization noise within the specified bandwidth and also prevents anti-aliasing effects. Oversampling can be achieved inherently when sampling frequency is greater than twice the bandwidth of the input signal. The shaped noise is attenuated using an on-chip digital filter. Mostly FIR-filters are used for this purpose since they are stable, simple to construct and decimation can be easily implemented within the filter. Finally, decimation is carried out at the end of conversion to eliminate the redundant samples due to oversampling since to reconstruct a signal it is enough that the sample rate has to be equal to twice the bandwidth.

First-order Sigma-delta ADC

Figure 3.4 shows the block diagram of a First-order sigma-delta ADC. The integral parts of sigma-delta ADC are the Noise shaping filter or integrator, ADC, DAC and a on-chip digital filter. The sigma-delta ADC without the on-ship digital filter
is called as sigma-delta Modulator. The output of the Modulator, i.e., from the internal ADC always depends on its previous outputs since its a negative feedback system.

Let $V_{in}$ be the DC input to the modulator. The integrator ramps upwards or downwards depending on the received input signal. The input to the integrator is a analog signal which is a difference in the voltage between the input $V_{in}$ and the voltage from DAC (node B). The output from the integrator (node C) is quantized into digital output (node D) by an internal ADC. The digital out is feed back to DAC for digital-to-analog conversion. The main aim of the negative feedback loop is to reduce the error voltage between $V_{in}$ and node B. The output of the modulator is from the internal ADC. By taking the FFT (fast Fourier transform) of output samples (node D) it is possible to see the signal and shaped noise at the modulator output. Finally, the shaped noise is removed using the on-chip digital filter.

![Block diagram of a first-order sigma-delta ADC.](image)

The important parameters of sigma-delta ADC are resolution, order, sampling speed, input signal frequency, etc. Figure 3.4 is called as First-order sigma-delta ADC since it employs a single feedback loop. As the order of sigma-delta ADC increases its SNR gets increased when compared to its previous counterpart, this because the Second-order Sigma-delta ADC employs double noise-shaping filters or integrators. Usually third-order or higher order sigma-delta ADC are not preferred because of stability issues. Similarly, increase in the resolution also increases the performance of the sigma-delta ADC.

Sigma-delta ADC offers high resolution ($\geq 16$ – bits) when compared to its counterparts. Speed is of concern in sigma-delta ADC. They can be used in applications involving sampling rates less than 1 MSps. Since this type of architecture consumes less power they can be used in low-power and low-voltage applications.

### 3.1.5 Time-based ADC

So far, we have discussed about the principle and application of the classical ADCs which uses voltage resolution of the applied analog signal for conversion process. As the CMOS process enters the deep submicron region, the classical ADCs and the most of the conventional ADCs suffer from delivering their required performance.
One main aspect of such technology is gate length scaling, which decreases the intrinsic gate delay while improving the speed of the circuit and thereby leading to benefit the digital circuits as compared with analog circuits. The other aspect which comes with the technology scaling is supply voltage reduction, which limits the voltage swing of the signal and therefore the signal-to-noise ratio of the ADC gets lowered. As the supply voltage reaches sub-1 V, the analog circuitry which is responsible providing high performance in flash and pipelined ADCs gets affected by these aspects and results in difficulties on improving their performance. Even, sigma-delta ADCs also suffers to a certain extent since they use complex analog circuits such as operational amplifier and DAC. Hence, this increases the attention towards time-based ADCs.

![Figure 3.5. Time-based ADC block diagram.](image)

The basic principle of a time-based ADC consists of two distinct steps, a voltage-to-time conversion step and then from time-to-digital conversion step. Figure 3.5 illustrates a time-based ADC. Depending upon the architecture preferred, sampling and quantization can take place anywhere in-between these two distinct steps. If required, the digital-post correction step can be added to compensate the digital-error occurred during the conversion steps.

Voltage-to-time conversion can also be referred as either pulse position modulator (PPM) or pulse width modulator (PWM). The PPM is the extended modulation of PWM based ADCs [7]. The voltage-to-time converters could be used to produce a series of pulse which is proportional to the applied input signal and it can be achieved using different techniques, like capacitor charging and comparator based techniques, linear voltage ramp and a continuous-time comparator based techniques and current-starved delay element based techniques. Depending on the required speed and resolution of the time-based ADC, any mentioned technique can be opted for the voltage-to-time conversion. As the technology scales down, another major technique for voltage-to-time conversion is the use of digital ring oscillators as VCO has been a recent choice of interest.

The time-to-digital converters (TDC) could be used to produce digital output corresponding to the measured input pulse. The TDC can be achieved using several methods and techniques; one such simplest possibility is by using a counter and could be used to count the time-interval between two pulses or even to count
the pulse itself. In past decades, several architectures and techniques have been employed to covert the time information, one accurate technique is to use delay line architecture and further improvements on the resolution can be provided by the use of vernier delay line based TDC which is an expanded version of simple delay line TDC.

3.2 Conclusions

Since, the CMOS technology moves into deep submicron region, many voltage-based ADCs starts to degrade in their performance due to the use of analog components. In recent years, VCO-based ADC has gathered immense interest due to its digital intense in nature and if it can deliver high performance then it could be possible to replace the VCO-based ADC in the place of a conventional ADC. In summary, this chapter gives a brief idea to the reader in understanding the concepts between voltage- and time-based ADCs and the working principle of classical ADCs. The basic principle with mathematical expressions and the other features of the VCO-based ADC are well described in the next chapter.
Chapter 4

The VCO-based ADC

In the end of the previous chapter, we outlined about the basic approach of a time-based ADC. In this chapter, we present about a conventional VCO-based ADC design, followed by its mathematical model and the inherent advantage of such time-based ADC. Next, an introduction to different topologies of VCO-based ADC and their limitations are discussed. The basics of VCO-based ADC are clearly important to perform an effective logic design. We will start the chapter with the working principle of VCO-based ADC.

4.1 Conventional VCO-based ADC

A time-based ADC has become one of the capable candidates for converting an analog signal into a digital domain, especially in deep submicron CMOS technologies. A conventional VCO-based ADC is illustrated in figure 4.1, which is realised using a VCO and followed by a counter structure. Functionally, the VCO is used to convert the input analog voltage into a time or a frequency information and then from frequency-to-digital using a simple counter.

![Block diagram of a conventional VCO-based ADC.](image)

The VCO produces an output frequency as a function of input voltage, since the input voltage is continuously varying in our case, a corresponding frequency variation is produced at the output. Then the output is fed into a counter struc-
ture, which is clocked at the sampling frequency, is used to count the number of transition edges in between the adjacent sampling instance. The counted value will be the quantized estimation of the applied input voltage of the VCO.

4.2 Basic principle

The VCO-based ADC

\[ x(t) \rightarrow \Phi(t) \rightarrow \Phi_e(t) \rightarrow \Phi_q[k] \rightarrow y[k] \]

Analog signal
VCO
Quantizer
Sampler
Output

Figure 4.2. Basic model for a VCO-based ADC.

The mathematical expression of the basic VCO-based ADC principle is illustrated in figure 4.2 [10]. The VCO is used to convert the input analog voltage \( x(t) \) into a phase information \( \Phi(t) \). The phase quantized output signal \( \Phi_q(t) \) is a multiple of \( 2\pi/N_\Phi \), where \( N_\Phi \) represents the number of output phases of the VCO. Then the quantized output of the VCO is sampled at a sampling rate \( F_s \) to produce \( \Phi_q[k] \). The output \( y[k] \) is obtained by taking the first order difference of \( \Phi_q[k] \), which is given as

\[
y[k] = \frac{1}{(2\pi/N_\Phi)}(\Phi_q[k] - \Phi_q[k - 1]) \quad (4.1)
\]

\[
\Phi_e[k] = \Phi[k] - \Phi_q[k] \quad \text{and} \quad (4.2)
\]

\[
\Phi[k] = \frac{kT_s}{\int_0^\Phi(v) dt} \quad (4.3)
\]

\[
\Phi_q[k] = \Phi[k] - \Phi_e[k] \quad (4.4)
\]

\[
\Phi_q[k] - \Phi_q[k - 1] = \Phi[k] - \Phi_e[k] - \Phi[k - 1] + \Phi_e[k - 1] \quad (4.5)
\]

\[
= \Phi[k] - \Phi[k - 1] - \Phi_e[k] + \Phi_e[k - 1] \quad (4.6)
\]

\[
= \{\Phi[k] - \Phi[k - 1]\} - \{\Phi_e[k] - \Phi_e[k - 1]\} \quad (4.7)
\]

\[
y[k] = \frac{N_\Phi}{2\pi} [\nabla \Phi[k] - \nabla \Phi_e[k]] \quad (4.8)
\]

here \( \nabla \) is the backward difference operator. The function \( \Phi(v) \) describes the voltage-to-frequency relation.
4.3 Inherent properties

The VCO-based ADC has found to provide an inherent feature due its own design nature. Two interesting features of the design are first-order noise-shaping property and sinc filter property. In other ADCs, they could need a special or complex circuitry to provide this interesting feature. The following section will provide a mathematical explanation of these inherent features.

4.3.1 First-order noise-shaping property

As mentioned, the VCO produces a continuous output in accordance with the applied control voltage input, therefore the VCO quantizes the input signal, as a result the quantization error (i.e., residual phase) occurs. Figure 4.3 [11] depicts the signal waveform of the VCO-quantizer, in which the counter is used to count both the transition edge of the VCO output. The quantized phase $\Phi_q[k - 1]$ in the previous sampling interval has become the initial phase $\Phi[k]$ for the current sampling instance, then the VCO-quantizer output $y[k]$ is given by

$$y[k] = \frac{N_\Phi}{2\pi} \{\Phi[k] - \Phi_q[k] + \Phi_q[k - 1]\}$$ (4.9)

taking Z-transform,

$$Y(z) = \frac{N_\Phi}{2\pi}(\Phi(z) + (z^{-1} - 1)\Phi_q(z))$$ (4.10)

where $\Phi_e[k]$ denotes the phase quantized error in $k^{th}$ sample and the overall quantized error is given as $\Phi_e[k] - \Phi_e[k - 1]$. The equation of VCO-quantizer output clearly illustrate a Noise Transfer Function (NFT) of $(1 - z^{-1})$, thus signifies first-order noise-shaping property and the same behaviour can be observed in a first-order sigma-delta converters. Since the VCO output and the sampling clock are uncorrelated, the noise is uniformly distributed in the interval from 0 to $2\pi/N$. Hence the $\Phi_e[k]$ is assumed to be white noise. This noise-shaping property has been one of the inherent feature of VCO-based ADC models. In order to perform such a noise-shaping property in a convention delta-sigma ADC, it needs an op-amp and a digital-to-analog converters, whereas in VCO-based ADC, it can be obtained by designing a VCO and appropriate digital circuits. Therefore, the design complexity is less in VCO-based ADCs and also the post processing can be done much easier in the digital world relatively than in an analog world. Beside quantization noise, there are other non-idea effects of VCO which can degrade the performance of VCO-based ADC, such as mismatch in the delay cells, clock jitter and phase noise.

4.3.2 Inherent anti-aliasing property

The second feature of the VCO-based ADC is an inherent sinc filter property [12]. As already mentioned, the VCO act as periodic continuous-time voltage-to-phase
The VCO-based ADC

Figure 4.3. Input and output waveform of a VCO-based ADC.

integrator. Where the quantized output phase of VCO at a sampling interval (for instance let’s take $k^{th}$ sample) can be described by

$$\triangle \Phi[k] = \int_{(k-1)T_s}^{kT_s} \Psi(v)dt$$ (4.11)

Considered an ideal linear VCO, then

$$\Psi(v) = 2\pi(f_0 + K_{vco}x(t))$$ (4.12)

where $K_{vco}$ and $f_o$ are the gain and the centre frequency of the VCO respectively and $T_s$ is the sampling period. Now considered $x(t)$ is a sinusoidal, given by $x(t) = A\cos(w_{in}t)$ and $w_{in} = 2\pi f_{in}$. Then it becomes,

$$\triangle \Phi[k] = A_{\phi} \cos\left(\frac{w_{in}T_s}{2}(2k-1)\right) + f_0T_s$$ (4.13)

where

$$A_{\phi} = 2\pi K_{vco}AT_s\text{sinc}(f_{in}T_s)$$ (4.14)

It could be seen that the $\text{sinc}$ function is the output phase of the VCO in any sampling intervals, in other words $\text{sinc}$ function is the amplitude of the input
signal in the phase-domain. These are the two very interesting inherent features of VCO-based ADC. There are different topologies in which such a VCO-based ADC design can be built. The following section gives you a brief overview of topologies involved.

4.4 Topologies

The attractive features of the VCO-based ADC has recently developed various research over this topic, which exhibited different architectures. The most-significant VCO-based ADC topologies are listed in the following section.

4.4.1 Single-phase architecture

A simple VCO-based ADC architecture is illustrated in figure 4.4 [1] which is realised using a single-phase of VCO. The VCO is commonly implemented as a ring oscillator structure with simple inverter or custom delay cells. The counter is used to count the number transition edges occurring at the VCO output. Careful measurement should be taken for such design, since counter may wrap around within a clocking instance. A reset counter can be used as an alternative architecture, in which the adder can be eliminated. The precision of the ADC can be increased by the counter which counts both the transition edges.

![Figure 4.4. A single-phase VCO-based ADC architecture.](image)

For the implementation of a single-phase architecture the minimum sampling frequency can be given by

\[
F_s > \frac{\max(f_{VCO})}{2K_{CNTR} - 1}
\]  

(4.15)

where \( f_{VCO} \) is the oscillating frequency of the VCO and \( K_{CNTR} \) is the counter word-length. The single-phase architecture is less complex in the design perspective and the power could be less consumed. But the effective resolution of such a design is restricted by the number of delay cells used in the VCO. At the same time, decreasing the sampling period may results in very good resolution. There is always a trade-off between the VCO frequency and the number of delay elements used in the VCO, the sampling frequency and the maximum oscillating frequency.
4.4.2 Multi-phase architecture

![Figure 4.5. A multi-phase VCO-based ADC architecture.](image)

A conceptual view of using the multi-phase VCO is illustrated in figure 4.5. Each output phase of the VCO is processed by a quantizer, a sampler and a differentiator (QSD). The QSD can be implemented by a single-bit quantization or a multi-bit quantization [10].

![Figure 4.6. Single-bit QSD structure.](image)

Single-bit quantization is illustrated figure 4.6 consists two flip-flops and an XOR. In single-bit quantization, the counter should ensure that only one transition edge can be captured in a sampling interval. Therefore, the minimum sampling frequency can be given by

\[ F_s \geq 2 \max(f_{VCO}) \]  \hspace{1cm} (4.16)

Multi-bit quantization is shown in Figure 4.7 consists of an asynchronous counter of width \( M_c \) processed by \( 2M_c \) flip-flop and a subtractor. In multi-bit quantization, a phase difference of VCO should be higher than \( 2\pi \) within a sampling interval. Therefore, the minimum sampling frequency can be given by

\[ F_s \geq \frac{\max(f_{VCO})}{2K_{CNTR} - 1} \]  \hspace{1cm} (4.17)

In other words, the asynchronous counter in multi-bit quantization should ensure that the multiple transitions can be captured in a sampling interval. The
4.5 Conclusions

Figure 4.7. Multi-bit QSD structure.

quantization circuitry in multi-bit design has more devices in compared with a single-bit, as result multi-bit quantization leads to increased hardware cost.

4.4.3 Multi-phase ADC with coarse-fine quantization

Figure 4.8 illustrate multi-phase VCO-based ADC with the coarse-fine quantization which consists of a counter, phase detector and a differentiator. The same counter used in a multi-phase multi-bit architecture can be used, but the counter is processed by only one VCO output phase and thereby providing coarse quantization of the phase accumulation. The phase detector is clocked at the sampling frequency and it estimates the process of the VCO during the sampling interval and thus decodes the fractional part of the phase accumulation. The coarse-fine quantization was mainly designed in order to reduce the hardware used in the quantization circuitry. The minimum sampling frequency is the same as in the multi-phase multi-bit VCO-based ADC architecture.

4.4.4 Sigma-delta ADC with VCO-based quantizer

The VCO-based ADC is described as VCO-quantizer in Sigma-delta ADCs, thereby it allows the Sigma-delta to achieve higher order by the simplest design. Several researches can be found in this topic [12], [13], [14], [15], etc.

4.5 Conclusions

The traditional working of the VCO-based ADC and the basic topologies has been studied, such that it leads to choose an appropriate architecture for this thesis work. In summary, a reader could have a glimpse of an idea to distinguish between the basic topologies and their design constrains. The choice of architecture will be explained with the gained knowledge in Chapter 5.
Figure 4.8. Block diagram of a multi-phase VCO-ADC with coarse-fine quantization architecture.
Chapter 5

The architecture of VCO-based ADC

This chapter gives you an introduction and the study of the chosen VCO-based ADC architecture. Each individual blocks of the choice of architecture has been studied clearly and a much specific analysis of their design implementation is given in the following chapters. The design was implemented at the high-level and also at schematic-levels using cadence design tool. The complete circuit-level of the VCO-based ADC design was implemented using a 65 nm CMOS process and their considerable experiments and simulations along with their results have been reported in Chapter 9. The different topologies explained in the previous chapter will allow the user to understand the terms and constrains used in this chapter.

5.1 Choice of architecture

The architecture chosen was a conventional VCO-based ADC with multi-phase single-bit quantization architecture, where the design uses a VCO to produce multi-phase outputs and each output phases are processed by single-bit quantization units. Usually this type of architecture can operate at high speed, but an experiment has been taken in order to get high resolution with the chosen architecture. In the VCO-based ADC design, the applied input analog voltage is converted into corresponding frequency and then, from frequency to corresponding digital output codes. Therefore, in this thesis work the frequency-to-digital conversion block is named as FDC. The functionality of this design has been implemented using a multi-phase VCO, differential to single-ended, FDC and an adder circuit respectively. Figure 5.1 illustrates the implemented VCO-based ADC design.

5.2 Block description

Since the VCO produces a multi-phase output, each output phase is processed by a FDC, therefore the required number of FDC depends upon the number of output
The architecture of VCO-based ADC

5.2.1 Voltage-controlled oscillator

Considering the design requirement for producing a multi-phase output, a much suitable VCO architecture has to be chosen. Before choosing the required VCO, the working principle of an oscillator and the path to choose a required VCO for an ADC should be clearly studied, which is described in Chapter 6. Generally, a VCO used in VCO-based ADC suffers from high non-linearity, considering that a differential structure could be opted, so that certain non-ideal effects can be inherently reduced. The control over the frequency of oscillation should be clearly known and the type of control can also vary. However, the VCO should have a wide tuning range in order to have a high resolution VCO-based ADC. The characteristic of an oscillator, different types and suitable oscillator for a VCO-based ADC design has been clearly described in the coming chapter.
5.2.2 Differential to single-ended

The purpose of a differential to single-ended converter design is to convert the VCO’s differential output into a single-ended output. Since the induced differential output signals of the VCO are $180^\circ$ out of phase with each other, any one of the signal can be processed for further conventions. Also, the chosen schematic of differential to single-ended can act as level shifter, so that it relaxes the output swing for the differential VCO. The circuit-level explanation and the simulation results of the chosen VCO and the differential to single-ended designs have been discussed in Chapter 7.

5.2.3 Frequency-to-digital conversion

The simplest way to convert frequency-to-digital domain can be realized using a counter. A synchronous counter is usually preferred for the single-bit quantization, such a counter consists two flip-flops coupled with a XOR gate. Figure 5.1, illustrate the counter structure as FDC block. In this case, a criteria occurs for the clock frequency, that the minimum sampling frequency should be chosen at-least twice the maximum oscillating frequency, such that it captures at-most a transition edge within the sampling interval. Mathematically the minimum sampling frequency can be given as

$$2 \max(f_{VCO}) < f_s$$  \hspace{1cm} (5.1)

More detailed working explanation and implementation is given in Chapter 8.

5.2.4 Adder

The adder is used to add all the single-bit digital value produced by the FDC. The purpose for adding is to produce a multi-bit quantization since the FDC is a single-bit quantizer. The adder is realized using a parallel-counter with the help of carry-save logic. The brief description of the adder is given in Chapter 8.

5.3 Conclusions

Certainly the chosen VCO-based ADC architecture will operate at high speed, but obtaining a high resolution should be verified through the simulation and the experiment results. After, obtaining conceptual understanding on the working of VCO-based ADC architecture, the behaviour-level and circuit-level design has been implemented in the next phase of this thesis work. The preceding chapters will provide details about the theoretical explanation, design implementation and experimental verification of each sub-blocks of the VCO-based ADC design.
Chapter 6

Basics for the choice of VCO

This chapter will describe about the fundamental principle of the oscillators and the direction towards the choice of a suitable oscillator. A much descriptive knowledge about the oscillators and different types of VCO in perspective with the requirement of the VCO-based ADC design have been presented. It is necessary to understand the basics of the oscillator so that a clear view on the quantization process can be evolved. The VCO is considered as the essential part and also act as time-based quantizer in this VCO-based ADC design.

6.1 Oscillators

Oscillators are one of the most essential parts of numerous electronic devices. Oscillator produces cyclic variation, typically in a time, of some measure. It is widely used in various applications ranging from the clock generation in the microprocessor to the carrier synthesis in the mobile phones. There are many implementations of oscillators, before venturing into the operation, a general study of oscillation in the feedback systems is necessary.

6.1.1 Fundamentals of oscillators

An oscillator is a simple circuit which produces a periodic output, usually in the form of a voltage for an appropriate input signal. Ideally the output signal is of constant amplitude with a specific frequency. But practically something less than this is obtained. In order to make the circuit oscillate, it is necessary to satisfy Barkhausen stability criterion [16]. Considering a negative feedback system, as shown in figure 6.1, the unity-gain or the voltage transfer function is given as

\[
\frac{V_{out}(s)}{V_{in}(s)} = \frac{H(s)}{1 + H(s)}
\]

where \( s = j\omega \) and \( \omega \) is the angular frequency. Usually, we want a feedback system to be stable and now we want to ensure sustained oscillation at a fixed frequency.
for the same system. For a steady oscillation to occur, the circuit must satisfy two conditions

$$|H(s)| \geq 1$$

$$\angle H(s) = 108^\circ$$

called Barkhausen criteria. The Barkhausen stability criterion is necessary, but it is not sufficient for oscillation [16].

![Negative feedback system](image)

**Figure 6.1.** Negative feedback system.

### 6.2 Overview of VCO

Oscillators can be classified into two broad categories according to their output wave shape, sinusoidal and non-sinusoidal. Different applications have different requirements for different types of oscillators. Practically any of the oscillator type could be modified into a voltage-controlled oscillator. In current technology, CMOS based VCO design has greatly induced into two typical choices of LC VCO’s and ring based VCO’s [16]. Each one has their own advantage over each other, when comparing noise characteristics, the LC oscillator is found superior over the ring oscillators while comparing phase and jitter noise. On the other hand, the LC oscillators have small tuning range, larger layout area and possibly higher power. For this reason and also considering the simplicity in design, cost effectiveness, a ring oscillator is commonly used for this purpose of VCO-based ADC. At first, a quick overview of the LC oscillator is demonstrated and then we present about the ring oscillator.

#### 6.2.1 LC oscillators

In high frequency circuits, the LC oscillator is more significant than the ring oscillator due to relatively good phase noise, cross-coupled inductance and capacitance. Basically from the name, the LC oscillator merely consists of inductance and capacitance. When the reactance of both the components are equal to each other, then it is called as a resonant tank circuit. The working principle of the LC oscillators is phenomenal, because through the appropriate sources, the inductor and
the capacitors are charged and then they are disconnected. Later the charging and discharging of the components results in the oscillation. Ideally this happens only when both these components are lossless, practically after certain periods the energy dissipates and do not provide a sustained oscillation. Therefore, a negative resistance is needed to compensate the loss and also to cancel the resistance produced by both the components [17]. Such model can illustrate as shown in figure 6.2.

Figure 6.2. LC tank with active gain.

There are several combinations of CMOS device available to provide the required negative resistance of the LC oscillators. Due to the passive element in the circuit it occupies a very large area when compared to the ring structures and also results in a very low quality factor which eventually leads a slow drop in the oscillation. However, the LC oscillators have better phase noise in comparison with the ring oscillators.

As discussed previously, many types of oscillators are available based upon the output waveforms. Depending upon the function required, the frequency band of oscillation and their unique response to noise/perturbation, each oscillator differ from each other. Recently, the ring oscillator has achieved more significance due to its vast feature, as compared to other monolithic oscillators [19]. We shall see the basic principle of the ring oscillator in the following section.

6.2.2 Ring oscillators

A Ring oscillator consists of multiple delay stages in a closed loop. Each delay stage can be realized as a simple inverting circuit. For a sustained oscillation the circuit should satisfy the Barkhausen criteria. The ring oscillator design has many useful and attractive features like, oscillation is achieved even at very low input voltage, dissipation of power is low at high frequency of oscillation, wide tuning range of given control voltage and because of its design nature, multiple output phases can be very easily achieved.

To gain more insight, let’s realize a basic single common-source feedback circuit in the place of a delay stage. Considering the common-source stage as an open-loop circuit as shown in figure 6.3, which contains only one pole, thereby providing a frequency-depended phase shift of 90° and also gained a DC phase shift of 180°
due to signal inversion at the output in accordance to the applied input signal. It is clear that, a system like this should provide $180^\circ$ of DC phase shift and $270^\circ$ frequency depended phase shift for a sustained oscillation. Therefore, the circuit fails to fulfil the oscillating condition.

![Common-source amplifier with feedback.](image)

In this case, any odd number of open-loop stages with a feedback and sufficient loop gain is required for a steady oscillation of the circuit and note, this only applicable for single-ended stages.

Consider a common-source stage is replaced by a simple digital inverter. As shown in figure 6.4 this system consists of an odd number of digital inverters which is cascaded and connected in a closed loop chain with sufficient gain, so that the system may oscillate as per the criterion. Basically, for each half cycle, the signal will be inverted from its state and propagate around the chain of inverters. At time $T/2$, all the inverters in the chain will go through this inverting transition state. Assuming $\tau_p$ is propagation delay (from the input of a single inverter stage to its output) of the signal, then the total propagation delay of the complete system is given as $N \cdot \tau_p$, where $N$ is the number of inverter stages used in the chain. In other words, at time $T$, the signal should propagate twice through the entire chain of inverters for a complete transition of its state. Then we have

$$\frac{T}{2} = N \cdot \tau_p \quad (or) \quad T = 2 \cdot N \cdot \tau_p$$

thus

$$F_{osc} = \frac{1}{2 \cdot N \cdot \tau_p} \quad (6.2)$$

where $F_{osc}$ denotes the frequency of oscillation.

The ring oscillators of $N$ inverting stages can be realized by many types of inverter stages. The single-ended and differential topology are the most common categories at which it differs from each other in the inverter stages. Before getting to the different categories, it is wise to understand the different ways at which the frequency of oscillation can be controlled through a particular design parameter of a circuit.
Figure 6.4. A chain of inverter in a closed loop.

A simple CMOS inverter comprises of NMOS transistor and PMOS transistor, conversely, this design does not have any parameter to control the oscillating frequency. Therefore, a control method is required and it can be given to the design by, by modulating the strength of an inverter in the chain or by having a variable load or by varying the power supply. It is difficult to implement the controllable capacitors or the resistors in advance technologies; therefore it is not extensively applicable and also varying the power supply has a trade-off in the performance and the DC level shift is undesirable [20]. Such designs are shown in figure 6.5 and 6.6.

Figure 6.5. Inverter circuits tunable by capacitive and resistive load controls.

Generally differential topologies are chosen due to the inherent advantages over the single-ended circuits. Differential ring oscillators are mostly preferred because of common-mode noise rejection due to its differential outputs, in a large amount of digital circuitry, it produces a lower noise injection into other circuits on the same chip and also lower sensitivity to the substrate and the supply noise [20]. In contrast to that, total power dissipation, phase noise and jitter noise are found
Figure 6.6. Inverter delay element tunable by power supply control.

Figure 6.7. Current starved inverter structure with control circuitry.

less in the single-ended topologies with respect to differential topologies. But still designers use differential over the single-ended circuits in many digital scopes.
Differential Ring oscillators

In order to sustain oscillation, usually the single-ended topologies need an odd number of stages or at least three stages, while the differential ring topologies can have either odd or even number of stages. Considering two stages, an additional phase shift is required, where it can be provided by crossing the output of the last stage and feeding back to the input of the first stage as shown in figure 6.8. This part of this chapter will give you few glitches in different topologies of differential circuits used.

![Two-stage differential ring oscillator block diagram.](image)

A basic or a simple differential circuit is shown in figure 6.9, can be constructed by differential amplifier with active load and while frequency or tail current of the system can be controlled by the voltage applied through an M1 NMOS control transistor. Since, the gate and the drain of the M4 and M5 PMOS transistor are coupled, the operating region of both the active device is always in saturation mode, hence it act as active load. Changing the gate voltage of the control transistor will not provide an appropriate change in the current level due to the node $V_p$, due to this, achieving a wide tuning range is difficult.

Therefore, a current mirror is used in practice, to control the stages using mirrored current, as shown in figure 6.10. By doing so, the frequency of oscillation can be much easily controlled by varying the mirrored current. But the output swing of the oscillator will be undesirable, since this system does not provide any control over it. Considering this impact, a simple enhancement has been made to this circuit as given in figure 6.11.

This differential circuit has a symmetric load element consists of diode connected M6 and M9 PMOS device in shunt with the equally sized PMOS biased device. Since, the $I-V$ characteristic of the load provides a symmetric behaviour, the load provided by such a structure is called symmetric load [21]. It also provides high gain resulting in wider frequency range. Due to the symmetric load, a load resistance is seen and causes decrease in the voltage swing from $V_{dd}$ to $V_{bias}$. Also, note that in order to provide a bias current for M1 NMOS device, a self-biased current source bias circuit is required. Therefore, an improved circuit was desired.
Figure 6.9. Basic differential amplifier circuit with active loads.

Figure 6.10. Basic current mirror circuit.
In order to provide better voltage swing, an additional active device is much needed. By doing so, the differential circuit made bit complex as shown in figure 6.12. The lower and upper voltage swing is controlled by $V_{bias1}$ and $V_{bias2}$ respectively, and the voltage swing was between $V_{bias2} + V_{tp}$ and $V_{bias1}$ [19]. Achieving voltage swing, the circuit suffered from increased noise characteristic and also wide range oscillating frequency is decreased due to the added active devices. Most certainly this structure required more area and high-quality resistors.

Addressing these many issues of the differential circuit, at least a circuit which over come certain requirement needed for the VCO-based ADC has to be opted. But still there are several parameters to be considered for evaluating the performance of the oscillators and only few parameters required for VCO-based ADC performance has been explained in following section.

6.3 VCO performance metrics

To measure the performance of an oscillator, there are some important parameters to be considered. They are center frequency, tuning frequency range, gain, output amplitude and noise. Oscillators are applied in several applications as tunable oscillators, i.e., for a particular control input an appropriate output frequency
is produced. As described before the control input is usually given as voltage. Consider a ideal voltage-controlled oscillator, the frequency obtained at the output is a linear function of control signal and it given as

\[ \omega_{out} = \omega_0 + K_{vco} V_{ctrl} \]  \hspace{1cm} (6.3)

where, \( \omega_0 \) is output frequency which corresponds to \( V_{ctrl} = 0 \) and \( K_{vco} \) is called gain of the system. Figure 6.13 depicts the exact definition of VCO. With this, we start describing the parameter of VCO [16].

### 6.3.1 Center frequency

The center frequency is mid range value between the maximum and minimum oscillating frequency. The reader should not confuse this frequency with \( \omega_0 \).

### 6.3.2 Tuning characteristic

Tuning range is the difference between the maximum and minimum oscillating frequency. As shown in figure, where \( \omega_1 \) is the output frequency correspond to a control voltage \( V_1 \) and \( \omega_2 \) is the output frequency correspond to a control voltage
6.3 VCO performance metrics

V\textsubscript{2} and if, the allowed V\textsubscript{ctrl} range is V\textsubscript{1} to V\textsubscript{2}, then the tuning rage achieved is the difference between ω\textsubscript{2} and ω\textsubscript{1}.

6.3.3 Tuning range

Gain is defined as the ratio of tuning range to control voltage range. It can be expressed as given in the equation 6.4 [16].

\[ K_{vco} \geq \frac{\omega_2 - \omega_1}{V_2 - V_1} \]  

(6.4)

6.3.4 Output amplitude

The output voltage of the voltage control oscillator will swing to minimum and maximum voltage which determines output amplitude. It is more desirable to achieve proper output swing in order to make less sensitive to noise and also to insure an appropriate input for the driving stage.

6.3.5 Noise source in MOSFET’s

Generally, the inherent noise is produced by active and passive devices. The noise sources in active device are thermal noise in channel, flicker noise, short noise and substrate resistance noise. For normal measurements, only thermal and flicker noise plays a dominant role and they have been studied for more than two decades in different perspective.

Thermal noise

Thermal noise can be seen in even good quality components. It is emitted due to the temperature and the quality of the device. Thermal noise in conductor is independent random movement of electrons caused by thermal agitation. In MOSFET’s, thermal noise have been viewed in two cases, strong and weak inversion.
[22], basically it is derived from the resistive channel of a device in active region. Overall the spectral density of noise voltage and noise current is given by

\[ V_n^2(f) = 4kt\gamma \frac{1}{g_m} \]

\[ I_n^2(f) = 4kt\gamma g_m \] (6.5) (6.6)

**Flicker Noise**

Flicker noise can be seen only, when a DC current flows through an active device. Usually flicker noise occurs due to the trap in the gate dielectric. It is commonly referred as 1/f noise and it is clear that it is naturally dominant at low frequencies. For this reason, the thermal noise is considered as very important noise source in MOSFET’s [8]. It is given as a voltage source in series with the gate value

\[ V^2 g(f) = \frac{K}{WLC_{ox}f} \] (6.7)

where \( K \) is constant, dependent on device characteristics and the variables \( W, L \) and \( C_{ox} \) is the Width, Length, and gate capacitance per unit area, of the transistor respectively.

**Phase Noise**

Undesirable variation at the output of the oscillator can be expressed in terms of time- and frequency-domain. Typically, phase noise is described in term of frequency-domain. Many theories have been proposed in order to measure the phase noise of a VCO in different perspective. A very basic understanding of phase noise can acquired from figure 6.14 shown.

Consider a voltage-controlled oscillator, oscillating at carrier frequency \( \omega_0 \). An ideal spectrum of the oscillator may be seen as in figure 6.15a, but in reality, the spectrum exhibit "skirts" like view as depicted in figure 6.15b. To measure the phase noise, the noise power at certain offset away from the carrier power is
6.3 VCO performance metrics

measured and divided by the carrier power. Usually the offset is 1 MHz from the carrier frequency, mostly depends upon the requirement of an application [23]. The phase noise expression can be given as

\[ P_{\text{phaseNoise}}(\delta_\omega) = 10 \cdot \log \frac{P_{\text{sideband}}(\omega_o + \delta_\omega, 1 \text{ MHz})}{P_{\text{carrier}}(\omega_o)} \]  

(6.8)

where \( P_{\text{sideband}}(\omega_o + \delta_\omega, 1 \text{ MHz}) \) represents the single sideband power at frequency offset \( \delta_\omega \) in the spectrum.

\[ \begin{align*}
\text{Ideal oscillator} & \quad \omega_o \\
\text{Actual oscillator} & \quad \omega_o
\end{align*} \]

Figure 6.15. Ideal and actual spectrum of the oscillator with frequency component \( \omega_o \).

Jitter

Basically jitter is merely phase noise by a different term and different names. Jitter is termed as an undesirable variation of the output signal in time-domain. The major source of the jitter is injection of fluctuated signal from the other parts or devices present in the same chip through the power supply. However, they are often minimized to an extent by differential circuit topologies. Considering an optimized circuitry, the sources of jitter are power supply variation, loading condition and so on, but the significant source is the inherent noise, such as flicker noise and short noise.

Types of jitter

Jitter can be measured in several ways. The two most quantifying ways are

1. Cycle-to-Cycle jitter
2. Long term jitter

These jitter metrics have different measurement mechanisms and they also generate differently circuit effects. In order to clearly differentiate, mathematical definition of these jitter metrics has been given in the following sections.

Cycle-to-Cycle Jitter

It is termed as unwanted variation in complete cycle time of signal with respect to adjacent cycle. For better understanding, it can be defined as change in the
period with respect to change in the adjacent cycles over a certain number of cycles. Mathematically, Consider a period, in which the \( n^{th} \) cycle of the period is defined as \( T_n = t_n + 1 - t_n \), then the cycle-to-cycle jitter \( (J_{cc}) \) can be given as

\[
J_{cc}(n) = \sqrt{\text{var}(T_n + 1 - T_n)}
\]  

(6.9)

![Figure 6.16. Measure of cycle-to-cycle jitter [24].](image)

It adds greater significance towards the stability of spectrum. This type of jitter measurement is difficult to measure. Large error or increased cycle-to-cycle jitter can make even a system to fail. Therefore, it is an important measurement of jitter.

**Long term Jitter**

It is termed as the maximum variation in the output signal from its ideal position for a large number of consecutive cycles. Mathematically, it is defined as the standard deviation of \( t_n + k - t_n \),

\[
J_k(n) = \sqrt{\text{var}(T_n + k - T_n)}
\]  

(6.10)

Measuring the types of jitter in the time-domain can be opted in numerous ways depending upon the application required. The mentioned types of jitter play a vital role in measuring the jitter of ring oscillators.

### 6.4 Conclusions

This chapter explained about the essential principle of the oscillators as well as the different types of voltage-controlled oscillator in accordance with the VCO-based ADC design. The basic explanation given here is always précised, considering it in a future perspective for choosing a suitable VCO and also, VCO is considered as the most essential part of this ADC design. The chosen VCO design and the simulation results are described in Chapter 7.
Figure 6.17. Measure of long term jitter.
Chapter 7

Design and simulation of the VCO

After exploring different architectures, a much suitable circuit of a voltage-controlled oscillator (VCO) is chosen and then implemented. The theoretical explanations of the chosen VCO, circuit implementation, suitable simulations and their results have been given in this chapter. Since the VCO is used in an analog-to-digital converter, particularly for time-to-digital conversion, only certain significant metrics have been measured for the performance analysis. Next, a driving circuit for processing the VCO output has been designed and their simulation results have also been reported.

7.1 Choice of voltage-controlled oscillator (VCO)

The design specification of the ADC is to get high resolution by employing a VCO for voltage-to-time conversion and the possible digital components for time-to-digital conversion. By the previous chapter, the study on fundamentals of oscillators and their types have given an idea to choose a suitable type of VCO. The literature study on different VCO architectures has given an understanting to summarize the design requirement of VCO which could be employed for the VCO-based ADCs. To summarize the requirement of an VCO, i.e.,

1. A wider frequency range.
2. A linear frequency output.
3. A full-swing voltage at the VCO output.

In comparison, between LC and ring oscillators, a ring oscillator can be chose for larger tuning range. In order to obtain ADC with high resolution, a ring oscillator with multiple-phases architecture could be employed. A differential VCO architecture has been chosen, that it could achieve a linear frequency range while tuning the applied input voltage. Figure 7.1 illustrates the structure of differential architecture.

The differential structure consists of an even number of delay elements. The
number of delay elements required was determined by the choice of VCO-based ADC architecture. Since, the choice was multi-phase single-bit quantization architecture; the required number of output bits will determine the number of delay elements needed. Each element in the delay unit produces a unique differential phase and thereby, if a VCO-based ADC is designed for $Z$ effective bits then the number of phases required is $2^Z$ which results in the same number of differential delay elements.

The specification of the VCO-based ADC design was to obtain a resolution of 8-bits and relatively, the selected architecture was multi-phase single-bit architecture which was favouring high speed and obtaining high resolution was a challenge. In the previous chapter, different delay element architectures are realized and discussions have been narrow downed. Therefore, in order to obtain high resolution, the selected architecture resulted in a large chain of delay stages in a delay unit which was not a usual case. From the obtained equation at 6.2, one can clearly notice that there is always a trade-off between the frequency and the number of delay stages, i.e., in the design implementation, as the number of phases increases or in other words as the number of delay element increases it will decrease the frequency of VCO oscillation. The decrease in the tuning range will degrade the performance of the VCO-based ADC and as a result, the output resolution will also be degraded. This trade-off factors on the VCO design is considered as one of the really challenge while implementing the ADC design. The following section will discuss about the selected VCO architecture and its working principle.

\section*{7.2 Theoretical description}

In the previous chapter, VCO basics and their types have been clearly discussed. An appropriate VCO architecture could be effectively choose by the knowledge gained. The working details of the selected architecture is given below and followed by a theoretical explanation of the driving circuit.

\subsection*{7.2.1 PMOS cross-coupled ring oscillator}

The design of each VCO’s delay cell was implemented using the PMOS cross-coupled structure as shown in figure 7.2. Since the target resolution was 8-bits, around 256 delay elements were designed in a closed chain.

Basically the delay cell consists of four PMOS transistors (M3, M4, M5 and M6).
and two NMOS transistors (M1 and M2). The bias tail-current which is commonly used in the differential oscillators (which we have discussed in the previous chapter) have been ignored due to the use of cross-coupled connection of the transistors. This cross-coupled fashion is accomplished by the PMOS transistors (M4 and M5) and it also guarantees a differential operation [25].

The latch is configured with the cross-coupled PMOS transistors (M4 and M5). The oscillation may not be sustained due to the latch formed by the cross-coupled transistors. Consequently, the NMOS transistors (M1 and M2) should be large enough to break the latch [26].

The NMOS transistors (M1 and M2) are considered as the input transistors of the delay cells and the auxiliary PMOS transistors (M3 and M6) are applied with the control input voltage. The width of the control transistors, i.e., width of PMOS transistors (M3 and M6) should be sufficiently large and the maximum operating region should be in linear region so that VCO produces a wide tuning range.

This differential circuit produces a differential output, as a result a differential to single-ended design was required to process the output of the VCO to the next driving circuit. The circuit-level differential to single-ended design working has been briefly explained and then followed by the analysis and the simulation result of both the circuits have been presented in the following sections.

### 7.2.2 Differential to single-ended converter

The differential to single-ended circuit has been designed and implemented as shown in figure 7.3. Single-ended CMOS output level has been efficiently obtained through this design.
This model consists of four PMOS transistors (M4, M5, M6 and M7) and three NMOS transistors (M1, M2 and M3). Basically this circuit converts the applied differential signal into single-ended signal and also acts as a level shifter which provides high gain for low input swing [27].

The NMOS (M2 and M3) are considered as the input transistors and the gate of PMOS transistors (M5 and M6) are tied to ground, thereby it acts as pre-charged device. The PMOS transistors (M4 and M7) are diode connected, as a result the operating regions of these transistors are always in saturation mode. The gate and the drain of the NMOS transistors M1 and M2 are coupled to the node $V_p$, respectively. Similarly, the gate and the drain of PMOS transistors M4 and M5 are also coupled to the node $V_p$ respectively. Therefore, this node $V_p$, which connects the gates of the NMOS M1 and PMOS M4, provides a feedback control to NMOS transistor [27].

As the voltage increases on the gate of the input NMOS transistor M1, it starts to conduct and pulls the drain voltage of the NMOS M1. This fall in the voltage, leads to the drop in the gate voltage on NMOS M1 as more current draws through PMOS M5 and M6 and also less current flows through the NMOS M1. Eventually it increases the current through the NMOS M1 simultaneously combines and decrease the current through NMOS M3. This reasons provide an amplitude rise at the NMOS M3 source (output).

If the voltage decreases on the gate of the input NMOS transistor M1, the current through the NMOS M3 changes hugely which results in the decrease of voltage at the source of NMOS M3 [28]. The basic working of the circuit is explained and the design also gives enough voltage swing for the driving circuit. Both discussed circuits have been implemented, simulated and their significant results have been given in the following sections.
7.3 Practical experiments

After understanding the working principle of the chosen circuits, both the circuit design has been implemented in the transistor-level using cadence design environment. Specific experiments have been carried out to estimate the performance of the employed circuits. The following sections will present about the simulation result of the opted circuits.

7.3.1 Ring oscillator

The VCO design is implemented and verified in the behavioural-level, as well as in the transistor-level. As explained, in the transistor-level a PMOS cross-couple differential architecture is adapted for a single delay cell in the chain of a delay unit. In order to design an 8-bit multi-phase VCO-based ADC, a ring oscillator consists of 254 cells have been implemented. The process type involves in the design of the VCO-based ADC is the CMOS 65 nm transistor from standard library in cadence design environment.

Initially, the width of the transistors in the PMOS cross-coupled VCO design where tweaked such that, the design satisfies the oscillation conditions and also noted, for the design to produce a sustained oscillation. Then, the design is mainly concentrated for characterising the required delay of the delay element and also for attaining a wide tuning range of the VCO. The rail-to-rail voltage was never a concern, because attaining a wide tuning range was very much necessary to get the higher resolution. Therefore, after deep study and different experiments on the implemented design, the width of the transistors where comparably sized, so that the VCO design has its maximum tuning range. As we know from the frequency of oscillation equation 6.2, the VCO transistors where sized to have a necessary delay over the applied control voltage, such that the transistor tweaking results in the wide frequency of oscillation. Figure 7.4 illustrates the transfer characteristic of the propagation delay of a single cell versus applied control voltages (DC voltages).

![Output waveform of VCO showing delay versus control voltage.](image)
Table 7.1. VCO control voltage with corresponding delay values.

<table>
<thead>
<tr>
<th>DC input voltage (V)</th>
<th>Delay (ps)</th>
</tr>
</thead>
<tbody>
<tr>
<td>0</td>
<td>7.08</td>
</tr>
<tr>
<td>0.25</td>
<td>9.58</td>
</tr>
<tr>
<td>0.50</td>
<td>14.86</td>
</tr>
<tr>
<td>0.75</td>
<td>22.62</td>
</tr>
<tr>
<td>1</td>
<td>24.24</td>
</tr>
</tbody>
</table>

Table 7.2. Comparison between theoretical values and simulation results of VCO output frequency.

<table>
<thead>
<tr>
<th>DC input voltage (V)</th>
<th>Delay (ps)</th>
<th>Frequency of oscillation (MHz)</th>
</tr>
</thead>
<tbody>
<tr>
<td></td>
<td></td>
<td>Theoretical values</td>
</tr>
<tr>
<td>0</td>
<td>7.08</td>
<td>278</td>
</tr>
<tr>
<td>0.25</td>
<td>9.58</td>
<td>205</td>
</tr>
<tr>
<td>0.50</td>
<td>14.86</td>
<td>132</td>
</tr>
<tr>
<td>0.75</td>
<td>22.62</td>
<td>87</td>
</tr>
<tr>
<td>1</td>
<td>24.24</td>
<td>81</td>
</tr>
</tbody>
</table>

Table 7.1 will give a clear number of the applied control voltage values and their appropriate delay values obtained through the simulations. The theoretical values for the oscillation of frequency can be calculated by applying the achieved delay values in the equation 6.2. Table 7.2 depicts and compares the calculated theoretical values versus the achieved practical values for the frequency of oscillation.

The tuning characteristic of the PMOS cross-coupled VCO has been plotted in figure 7.5. It describes, by slowly varying the applied DC input, the VCO produces an appropriate output frequency at each applied voltage. When the input control voltage increases, there is a decrease in the frequency of oscillation due to the PMOS cross-coupled structure and also the obtained tuning characteristic shows an inverse function, while we considered an ideal tuning characteristics of a VCO.

The process corner variations are one of the design experiments, in which the variation in the fabrication parameters will degrade the performance of any device. The tuning range could also vary with different process parameters. In order to guarantee the VCO tuning range, simulation for different process values have been carried out and listed as shown in table 7.3. It was identified, that the tuning range has significantly varied with the process variations. Figure 7.6 clearly illustrate the plot for tuning range versus process.

The noise measurement is the other significant test in the implemented design. The noise in the design could be introduced due to the instability in the frequency of VCO oscillation. Therefore, the noise measurement is a significant performance
Table 7.3. Process corner simulation and corresponding values of VCO output frequency.

<table>
<thead>
<tr>
<th>Process type</th>
<th>Frequency of oscillation (MHz)</th>
<th></th>
<th></th>
</tr>
</thead>
<tbody>
<tr>
<td></td>
<td>When DC input = 1</td>
<td>When DC input = 0</td>
<td></td>
</tr>
<tr>
<td></td>
<td>Fmin(MHz)</td>
<td>Fmax(MHz)</td>
<td></td>
</tr>
<tr>
<td>0-Typical</td>
<td>81</td>
<td>279</td>
<td></td>
</tr>
<tr>
<td>1-Fast/Fast/Fast</td>
<td>110</td>
<td>352</td>
<td></td>
</tr>
<tr>
<td>2-Slow/Slow/Slow</td>
<td>55</td>
<td>204</td>
<td></td>
</tr>
<tr>
<td>3-Fast/Slow/Typical</td>
<td>79</td>
<td>260</td>
<td></td>
</tr>
<tr>
<td>4-Slow/Fast/Typical</td>
<td>81</td>
<td>299</td>
<td></td>
</tr>
<tr>
<td>5-Fast/Slow/Slow</td>
<td>79</td>
<td>260</td>
<td></td>
</tr>
<tr>
<td>6-Slow/Fast/Slow</td>
<td>81</td>
<td>299</td>
<td></td>
</tr>
<tr>
<td>7-Fast/Slow/Fast</td>
<td>79</td>
<td>260</td>
<td></td>
</tr>
<tr>
<td>8-Slow/Fast/Fast</td>
<td>81</td>
<td>299</td>
<td></td>
</tr>
</tbody>
</table>

Figure 7.5. Transfer characteristics of a PMOS cross-coupled VCO.

Considering this, jitter is a vital noise source and also an important performance metrics in measuring the performance of the complete design. Figure 7.7 gives you the measured value of jitter at one particular frequency. Table 7.4 shows the measured jitter values at different frequency with respect to the applied input voltages. The measured values were then related with the frequency of oscillation and found to be reasonable. Also, the achieved jitter values were found to much
smaller and ensured that the desired edge will certainly fall within the sampling window.

<table>
<thead>
<tr>
<th>DC input voltage (V)</th>
<th>Oscillating frequency (MHz)</th>
<th>Long term jitter (ps)</th>
</tr>
</thead>
<tbody>
<tr>
<td>0</td>
<td>279</td>
<td>3.891</td>
</tr>
<tr>
<td>0.5</td>
<td>131</td>
<td>7.10</td>
</tr>
<tr>
<td>1</td>
<td>81</td>
<td>16.09</td>
</tr>
</tbody>
</table>

The VCO output is a pulse width modulated signal. If the transistors are reasonably sized then this topology can provide a rail-to-rail voltage swing. But
in the implemented VCO design, the transistors were tweaked only to provide a wide tuning range rather than the rail-to-rail voltage. Therefore, the output of the implemented VCO is a pulse width amplitude modulated signal. Since the output produced from the VCO is a differential output, a differential to single-ended design have also been implemented in the VCO-based ADC design. The experiment on the differential to single-ended design and their simulation results have been given in the following section.

7.3.2 Differential to single-ended

This design is implemented in the circuit-level with the same process type (typical), as used in the VCO circuit design. The transistors width has been sized such that the transistors employed has to perform their appropriate functions, i.e., their width of the transistors has been nominally sized to predominantly perform a proper pull up and pull down working. Figure 7.8 illustrate the differential input and single-ended output.

Figure 7.8. Input and output waveform of differential to single-ended converter.

From the waveform (figure 7.8) it is clear that the input and the output frequency of the differential to single-ended circuit has to be measured. Measure have been taken to size the transistors such that the frequency at the input and the output are same. Added to this, the circuit also acts as a level shifter to certain extent. The voltage range at the VCO output varies with the applied input voltage. Table 7.5 shows the DC input voltage and their corresponding output voltage range of the VCO. There is a voltage drop in the VCO output swing at minimum input voltage, where it is corrected by differential-to-single ended circuit and it can also be seen in figure 7.8. The minimum and maximum output voltages of the single-ended outputs are 0.03 to 1 V respectively, and the analysis has been found that this range is enough to drive the next circuit, FDC.
Table 7.5. Achieved output values at each sub-blocks for applied DC input voltage.

<table>
<thead>
<tr>
<th>DC input voltage (V)</th>
<th>0</th>
<th>0.5</th>
<th>1</th>
</tr>
</thead>
<tbody>
<tr>
<td>VCO output frequency (MHz)</td>
<td>279</td>
<td>131</td>
<td>81</td>
</tr>
<tr>
<td>VCO output voltage swing (V)</td>
<td>0.17 to 0.97</td>
<td>0.03 to 0.99</td>
<td>0 to 1</td>
</tr>
<tr>
<td>Differential to single-ended output frequency (MHz)</td>
<td>279</td>
<td>131</td>
<td>81</td>
</tr>
<tr>
<td>Differential to single-ended output voltage swing (V)</td>
<td>0.03 to 1</td>
<td>0.03 to 1</td>
<td>0.03 to 1</td>
</tr>
</tbody>
</table>

7.4 Conclusions

This chapter has discussed about the theoretical working, circuit implementation and simulation results of chosen VCO and its driving circuit. The processing blocks of the VCO-based ADC design are explained in chapter 8 with much theoretical descriptions and practical implementations. The complete simulation of the VCO-based ADC design is presented in chapter 9.
Chapter 8

Frequency-to-digital converter and Adder

This chapter focuses on the frequency-to-digital conversion and the various types of the adder. The study on the working principle of conversion subsystems and the design implementations are explained. The design approach of the adder has been much descriptively explained in the next section. They are modelled and designed in both behavioural- and transistor-levels in order to analyse their performance and functionality.

8.1 Frequency-to-digital converter

The basic principle of the frequency-to-digital-converter (FDC) is to calculate the difference in phase by comparing the samples caused due to the VCO output signals with the help of the XOR gate and the set of registers. Also, we can measure the number of transitions that take place within the given sampling periods. The implementation of the frequency-to-digital-converter is as follows

8.1.1 D flip-flop

The D Flip-Flop (DFF) is a memory element used to sample the signals from the different VCO phase output. The positive edge triggered D flip-flop has one data signal \(D\) with the clock signal \(clk\). If the input data signal is high with rising clock pulse, the output \(Q\) becomes one. If the input data signal is low with the rising clock pulse, then the output \(Q\) becomes zero. The positive edge triggered D flip-flop detects samples only at each rising edge. The block diagram, truth table and the waveform of the D flip-flop are shown in figure 8.1 [29].

8.1.2 XOR gate

The purpose of the XOR gate is to compare the current samples with the previous one to find whether the VCO phase has undergone transition. The logical
operation of the XOR gate states that the output will be 1 if both the inputs are different and the output will be 0 if both the inputs are same. Figures 8.2 and 8.3 shows the symbol and waveform of the XOR gate.

![XOR gate symbol](image1)

**Figure 8.2.** XOR gate symbol.

![XOR output waveform](image2)

**Figure 8.3.** XOR output waveform.
8.1.3 FDC implementation

The frequency-to-digital converter can be realized by using two D flip-flops and one XOR gate. The FDC block diagram is shown in figure 8.4 [30].

![Figure 8.4. FDC block diagram.](image)

The first D flip-flop collects the VCO phase samples at each rising edge. The first D flip-flop’s output is connected to the second D flip-flop in order to detect the previous sample at each rising clock edge.

![Figure 8.5. FDC waveforms (a) FDC input signal; (b) Sampled output waveform of DFF 1 and 2; (c) Sampling clock; (d) FDC output waveform.](image)

The XOR gate then measures the phase difference between both these two D flip-flop’s output samples. Thus, FDC detects both the rising edge and the falling edge within one sampling clock period. This implies that FDC works as an
edge detector. The quantization error occurs with half a clock period due to the difference in VCO phase and the FDC output. Figure 8.5 shows the waveform of FDC at each stage.

8.2 Adder

The main purpose of the adder is to form a multi-bit quantizer by adding 256 FDC’s output signal operating in parallel. This adder can be realized by using (256:9) Parallel-counter. The parallel-counter consists of a carry-save adder and a vector-merging adder. The explanation of the carry-save adder and different types of vector-merging adders are as follows.

8.2.1 Carry-save adder

The carry-save adder (CSA) is mainly used for adding three or more operands with low propagation delay [31]. The delay of the adder is very high when using two-operand adder repeatedly to add multi-operand data. As shown in figure 8.6, the CSA has set of the full adders placed in parallel where there is no connection in the carry with any of the full adders placed in the horizontal row. Instead of propagating the carry to the next higher order adder, the carry is saved as an output. The carry propagation occurs only at the last level in the carry-save addition. In all other levels, it produces the partial sum and the sequences of the carry independently.

![Figure 8.6. Block diagram of a carry-save adder.](image)

The propagation delay of the carry-save adder is same as the full adder delay. Each full adder compresses its three inputs into two-bit output. Since the CSA is used for the multi-operand operation, the cost of the circuitry is very low when compared to all other adders such as the carry-select adder, the carry-look-ahead adder, etc. Most of the adders are designed for adding two-operand data. Due to this, the CSA is not familiar because it requires at least three input integers for adding rather than two. It can reduce the n-digit number to the two-digit number. It reduces the delay without an increase in hardware cost. The main application of the CSA is to add partial products in the multiplier.
8.2 Adder

\[ A + B + C = (2 \cdot Carry) + Sum \]  

(8.1)

The basic component used for CSA is the full adder with inputs A, B and C produces sum and carry. The values of

\[ Sum = (A + B + C) \mod 2 \quad \text{and} \quad Carry = \left(\frac{A + B + C - Sum}{2}\right) \]

(8.2)

8.2.2 Vector-merging adders

The final stage to compute the parallel-counter is to add the 2-bit data by the use of carry-propagate adder or any type of fast adders. There are different types of adders to merge the vector, such as

1) Ripple-carry adder
2) Carry-look-ahead adder
3) Carry-select adder

These adders will be discussed in the following sub sections.

Ripple-carry adder (RCA)

The ripple-carry adder is the basic adder designed by cascading the n-full adders in series, see figure 8.8 [33]. The carry-out of the full adder is fed into the carry-in of the next full adder. The output of the each carry ripples through each full adder. The functionality of the RCA is easily understood by the truth table shown in figure 8.9. The main disadvantage of the RCA is that the delay will be very high when the word-length increases. This adder is very slow for high word-length since the carry will propagate through all the full adders to reach the output. The mathematical functions of the adder are

\[ Sum = A \oplus B \oplus C \]

(8.3)

\[ C_{out} = A \cdot B + A \cdot C_{in} + B \cdot C_{in} \]

(8.4)
Figure 8.8. Block diagram of an n-bit ripple-carry adder.

Figure 8.9. Symbol and truth table of the full adder.

Carry Look-Ahead Adder (CLA)

The carry-look-ahead adder is mainly used to avoid the rippling effect caused by the carry [33]. The main aim of the CLA is to generate the carry signal in parallel. By doing so, we can avoid the delay caused by carry-propagation. This circuit is implemented by two main signals, called carry-generate and carry-propagate. These signals are computed as

\[ G_i = A_i \cdot B_i \]  

\[ P_i = A_i \oplus B_i \]
The carry is calculated in advance on by the fact that carry will be generated in two conditions: (1) when both input bits $A_i$ and $B_i$ are 1 or (2) when any one of the input bit is 1 and the carry of the previous stage full adder is 1. This can be expressed as

$$C_{i+1} = A_i \cdot B_i + A_i \oplus B_i \cdot C_i$$  \hspace{1cm} (8.7)

, this expression can be also written as

$$C_{i+1} = G_i + P_i \cdot C_i$$  \hspace{1cm} (8.8)

It should be noted that the carry signal depends only on the input bits. So it does not need to wait for the carry to propagate through all stages of full adders. By using this technique, the carries of the 4-bit CLA can be written as

$$C_1 = G_0 + P_0 \cdot C_0$$  \hspace{1cm} (8.9)

$$C_2 = G_1 + P_1 \cdot G_0 + P_1 \cdot P_0 \cdot C_0$$  \hspace{1cm} (8.10)

$$C_3 = G_2 + P_2 \cdot G_1 + P_2 \cdot P_1 \cdot G_0 + P_2 \cdot P_1 \cdot P_0 \cdot C_0$$  \hspace{1cm} (8.11)

$$C_4 = G_3 + P_3 \cdot G_2 + P_3 \cdot P_2 \cdot G_1 + P_3 \cdot P_2 \cdot P_1 \cdot G_0 + P_3 \cdot P_2 \cdot P_1 \cdot P_0 \cdot C_0$$  \hspace{1cm} (8.12)

In the same way, the carry of the n-bit CLA can be written as

$$C_{i+1} = G_i + P_i \cdot (G_{i-1} + P_{i-1} \cdot C_{i-1}) = G_i + (P_i \cdot G_{i-1}) + (P_i \cdot P_{i-1}) \cdot (G_{i-2} + P_{i-2} \cdot C_{i-2})$$  \hspace{1cm} (8.13)

The sum signal can be expressed as

$$Sum_i = P_i \oplus C_i$$  \hspace{1cm} (8.14)

The CLA can be implemented by two blocks:
1. The adder block used to find Generate ($G_i$), Propagate ($P_i$) and Sum signal ($S_i$).
2. The CLA logic block used to compute the carries for the n-bit CLA.

The logical design for the 4-bit CLA shown in figure 8.10.

**Carry-Select Adder (CSEL)**

Based on the assumption by giving two different carry inputs (i.e., zero or one), the carry-select adder calculates with these two inputs and produces two results in parallel. The calculated carry is then passed into the 2:1 multiplexer and selects the correct value. Except the least-significant bit, the two addition operation occur in parallel on all other bits. The selection of carry to the multiplexer enables any one of the two adders. If the carry is selected as one, then the bottom addition operation passes the sum signal and the carry-out signal. If the carry is selected as zero, then the top addition operation passes the sum signal and the carry-out signal. The basic structure of the n-bit carry-select adder is shown in figure 8.11.

Instead of waiting for the carry signal, the addition operation occur with the assumed carry. The CSEL is very fast when compared to the RCA since addition
performs in parallel. There are two different ways to implement CSEL 1) Linear carry-select adder 2) Square root carry-select adder. The propagation delay of the N-bit adder with M number of stages is determined as

$$T_{add} = t_{setup} + M \cdot t_{carry} + \left[ \frac{N}{M} \right] \cdot t_{mux} + t_{sum}$$

(8.15)
Comparison of vector-merging adders

The main aim is to design an 8-bit vector-merging adder with less propagation delay. The ripple-carry adder increases its propagation delay when the word-length increases, which makes us to move towards fast adders. The ripple-carry adder is approximately four times greater in delay when compared to the CLA. So the ripple-carry adder is not mostly applicable in real time use. The comparison between the adders on delay and power consumption is shown in table 8.1. The power consumption of the CLA is very high compared to RCA, but it is very low when compared to all other fast adders [34]. And the carry-look-ahead adder is very good with low propagation delay, which makes us to choose as a vector-merging adder.

<table>
<thead>
<tr>
<th></th>
<th>Delay (ps)</th>
<th>Power consumption (uW)</th>
</tr>
</thead>
<tbody>
<tr>
<td>Ripple-carry adder</td>
<td>284.2</td>
<td>409.2</td>
</tr>
<tr>
<td>Carry-look-ahead adder</td>
<td>62.89</td>
<td>1168</td>
</tr>
</tbody>
</table>

8.2.3 Dot notation

Figure 8.12 shows the representation of dot notation for carry-propagate adder and carry-save adder. Instead of using values, dot notation is used for positioning and aligning the bits. Each digit is represented by a dot. We can add any of the dot in the input since each column of the dots has an equal positional weight. The sum and carry of the each full adder are divided in the diagonal line.
8.2.4 Parallel-counter

It is a multi input circuit used to count the number of one’s in the input. A single full adder is also represented as a (3:2) Counter. Since it counts the number of one’s in those three inputs and produces two-bit output. In other ways, we can generalize it as an n-input Counter produces $\log_2(n+1)$-bit output (i.e., $(n : \log_2(n+1))$ Counter).

The dot notation and the circuit diagram of the (10:4) Parallel-counter is shown in figure 8.13 [32]. This parallel-counter consists of ten 1-bit operands. The upper two levels consist of a carry-save adder while the third level consists of a carry-propagate adder.

![Figure 8.13. Structural diagram and dot notation of (10:4) Parallel-counter.](image)

Each row in the input data has a one binary number. These set of numbers reduces the 10-input binary value to 4-bit binary output. The dot notation shows that the 10-inputs are aligned into three inputs marked in the dashed box. The divided three inputs are given into the single full adder. Each full adder reduces the number of operand by one. Instead of propagating the carry, the carry is moved left side down by one place to the full adder which placed in the next level.

If the number of operands is $n$, we need to use $(\frac{n}{3})$ full adders for summation at each level and the carry should be moved diagonally, which makes the propagation delay independent of the input word-length. This process should be repeated indefinitely until it reaches to two-bits. Then the resulted 2-bit values are passed into the ripple-carry adder or any other fast adders. Note that the critical path for this structure is two full adders and one carry-propagate adder (i.e., 2 Half adders and 1 Full adder).

We can minimize the overall delay only at the final level of carry-propagate adder there by using some fast adders such as carry-select adder, carry-look-ahead
adder, etc. It should be noted that the sum and the carry can be added, if it has the same weighted bits. The final result of the parallel-counter has the length of approximately $\log_2(n)$-bits. In this thesis, we used parallel-counter for counting the number of 1’s for 256-operands. The time taken to count $(n : \log_2(n+1))$ Counter is

$$(k \cdot T_{CSA}) + T_{CPA}$$

(8.16)

where

$T_{CSA} = \text{Propagation delay of the CSA which is equal to full adder delay ($T_{FA}$)}$

$T_{CPA} = \text{Propagation delay of the CPA}$

$K = \text{number of levels or tree height}$

$n = \text{Number of operands}$

### 8.2.5 (256:9) Parallel-counter

The (256:9) Parallel-counter is the circuit that counts the number of one’s among 256 inputs and produces a 9-bit binary value. The circuit consists of 12 levels of carry-save adder and an 8-bit vector-merging adder. The CSA decreases its number of operands by the factor of $2/3$ [31]. Each level of CSA reduces the number of full adders by $n/3$ times. This implies that the number of full adders at the first level must be $256/3 = 85$ full adders at the max. The resulting sequence decreases the number of full adders by 85, 56, 38, 24, 16, 10, 7, 5, 3 and 1 at each level of CSA. This process continues until the last level consists of two-operands. Initially, we added this two-operand binary value by using a vector-merging adder called ripple-carry adder. Due to the large occurrence of glitches produced by the difference in delays, this CPA will then be replaced with the carry-look-ahead adder to decrease the delay.

### 8.2.6 Simulation results

As discussed, the parallel-counter was designed using a 65 nm CMOS technology in cadence. The propagation delay of the parallel-counter is to multiply the tree height with the delay time of the carry-save adder and the obtained result will be then added with the delay time of the vector-merging adder. The measured values are shown below from the simulation

Tree height = 12 levels

$T_{CSA} = T_{FA} = 25$ ps

<table>
<thead>
<tr>
<th>(256:9) Parallel-counter</th>
<th>Total delay (ps)</th>
<th>Power consumption (mW)</th>
</tr>
</thead>
<tbody>
<tr>
<td>with RCA</td>
<td>581.5</td>
<td>22.14</td>
</tr>
<tr>
<td>with CLA</td>
<td>367.8</td>
<td>23.46</td>
</tr>
</tbody>
</table>

*Table 8.2. Delay and power consumption for (256:9) Parallel-counter.*
8.3 Conclusions

In this chapter, we have analysed the frequency-to-digital converter and the various sub-blocks of adder and their design procedures are explained. All sub-blocks of the adder are integrated and tested to analyse the performance with respect to delay and power consumption. The whole ADC integration and simulation results are followed in the next chapter.
Chapter 9

Experiments and Simulation results

9.1 Experimental arrangement

This chapter deals with the analysis and simulation experiments of the implemented ADC with aiming to improve its dynamic performance. The VCO-based ADC design has been implemented in behavioural- and transistor-levels. As mentioned in earlier chapters, CMOS 65 nm technology node has been employed for the circuit-level simulations. Different set of experiment simulations have been performed and their corresponding results have been tabulated at the end of the chapter. This VCO-based ADC is an all-digital system utilizing possible digital components along with simple suitable circuits.

The ADC design implementation consists of a multi-phase VCO, a one-bit counter for each phase and an adder to add each resulting bits of the one-bit counter. Therefore, the implemented design has an array of one-bit counter structure driven by a large adder tree-structure, where this combined structure increases the simulation time. And also, the ring oscillator delay elements are connected in a closed-chain which seriously increased the simulation time. After integrating all these sub-blocks, the complete circuit-level simulation took an order of few weeks or even a month for receiving a reasonable output data. In this VCO-based ADC design, the VCO alone is considered as an analog device and the processing devices are all considered as the digital components. In general, while processing signal in a noisy environment, the digital circuit is considered to have an upper hand as compared to an analog circuit, i.e., the digital signal is commonly known for its greater noise immunity over an analog signal. Hence, in the complete system design the VCO alone is chosen in circuit-level and then, different experiments have been carried out in a desirable time. A more descriptive content of the experiments are given in the following sections.
9.2 Simulations and results

The VCO-based ADC design has been initially modelled in the high-level to study the behaviour and the characteristic of a time-domain-based ADC. The dynamic performance evaluation has been measured, since it is a key test which assures the quality of the converted output signal over the applied range of frequencies. In order to evaluate the ADC dynamic performance, a sinusoidal wave of 40 MHz frequency and the voltage swing of 1 V are applied as a stimulus. The design parameters for the behaviour-level simulations have been chosen such that the model results to an ideal 8-bit ADC. After circuit-level simulations, the practical limitations have been understood and much desirable parameter values have been chosen for the behavioural simulations. The circuit-level VCO has been examined for different experiments (explanatory results in Chapter 6) and found to achieve a gain of 187 MHz with the tuning frequency range of 90 MHz to 277 MHz at 0 V to 1 V respectively. The ADC speed has been chosen as twice the VCO maximum oscillating frequency and it was chosen around 572 MHz.

Then, these achieved parameter values have been chosen for the high-level model and the VCO-based ADC design has been simulated again, so that the performance of the circuit-level and high-level simulations can be closely compared. Due to the design structure, the complete circuit-level simulations were taking a longer duration. Therefore, the ADC dynamic measurements have been carried out in the mixed-levels with transistor and behaviour designs. In the implemented ADC design, the VCO is the most non-linear device as compared with the other devices, taking this into understanding, in the circuit-level simulation testing, the VCO is alone designed in circuit-levels and the processing devices are modelled in the high-level for measuring the dynamic performance.

It was identified that the viewed output waveform at 1 V input voltage swing has experienced a clipping behaviour. In other words the ADC suffers from distortion and thereby the experiment started by analysing the reason for this clipping behaviour. The reasons for the distortion in output waveform could be an incorrect DC biasing or the applied signal amplitude may be too large or the conversion may not be linear for the entire input signal voltage.

At first, the experiments started by changing the input signals amplitude. The simulations were performed by changing the input signals peak-to-peak voltage, so that the simulation experiments could estimate the converters dynamic behaviour and also to verify the elimination of clipping behaviour. After different experiments, a much suitable range has been opted by viewing the unclipped waveform and also by analysis the dynamic measurement values. Figure 9.1 illustrates the half range input and output waveforms of the implemented VCO-based ADC design.

The clipping behaviour reasons were not clearly identified, however the results from simulation experiments determined that an applied input signal was correctly reproduced without clipping due to the opted input amplitude range. The results of the experiments performed by changing the peak-to-peak voltage have been captured and their corresponding output spectra are shown in figure 9.2. Later with the calculated dynamic performance results, a clear pictorial representation
9.2 Simulations and results

Figure 9.1. Input and output waveforms of the VCO-based ADC.

has been given as shown in figure 9.3.

Figure 9.2. Various output spectra of VCO-based ADC with respect to the change in peak-to-peak input signal voltage.

The peak-to-peak voltage tweaking experiments for analysing the dynamic performance has also found with a change in the DC level. Henceforth, the DC level was kept constant and needed experiments were again simulated at the same in-
Figure 9.3. Dynamic performance of VCO-based ADC is graphically represented with respect to the change in peak-to-peak input signal voltage.

put frequency. The constant DC level with the different peak-to-peak voltages of an applied input signal have been experimented in order to verify the ADC for providing an improved dynamic values. Figure 9.4, shows the output spectra with fixed DC level at different peak-to-peak voltages and corresponding dynamic performance have been graphically shown in figure 9.5. The system again found to deliver improved dynamic values at half-range input voltage. The dynamic results obtained, lead to choose an appropriate DC level and peak-to-peak voltage. But that was only a vague understating with these experiments and simulation results.

And then, the experiment added to verify the VCO linearity for the entire input amplitude since it could also be a reason for this distortion. In this VCO-based ADC design, the VCO tuning range will have a direct impact on the linearity of the ADC itself, since the ratio of the VCO tuning range to the sampling frequency will majorly determine the resolution of the ADC. Under the practical conditions, the VCO transfer function is a non-linear curve in circuit-level simulations. Considering this, in order to examine the VCO’s linearity, the VCO’s input signal was parametrically swept with DC input voltage in much minute voltage difference. Figure 9.6 shows the best linear tuning curve of the implemented VCO.

After viewing the practical curve, the VCO tuning range was found linear from 100 mV to 600 mV and not with the entire input voltage range. The practical linear curve had answered the reason for the performance behaviour in the peak-to-peak and the DC level experiments. From the measured VCO linear tuning range, the input amplitude range and the DC level have been exactly chosen. These values are the best input design parameters for providing the finest performance of the implemented time-domain-based ADC design.
9.2 Simulations and results

**Figure 9.4.** Various output spectra of VCO-based ADC with respect to the change in DC levels of input signal voltage.

**Figure 9.5.** Dynamic performance of VCO-based ADC is graphically represented with respect to the change in DC levels of input signal voltage.

Then the experiments and simulations are performed to identify the ADC bandwidth. Usually, the bandwidth of an ADC is related to the sampling frequency, but not in the case of an oversampling ADC. After different experiments for the input frequency range, the design parameters were accurately chosen and the ADC was found to deliver an ENOB of around 4.5-bit with the bandwidth of 1 MHz to
120 MHz. This frequency range was considered as the converters bandwidth which will provide a perfect reconstruction of the applied signal. For different frequency experiments, their corresponding output spectra are shown in figure 9.7 and their corresponding dynamic values have been pictorially represented in figure 9.8.

Interestingly, there could be two more factors, which can be discussed on ob-
9.3 Conclusions

The ADC dynamic performance has been experimented and simulated in various aspects in order to evaluate the implemented VCO-based ADC design performance. The VCO maximum linear tuning-range has been identified and an appropriate simulation has been performed to achieve the best dynamic performance results. Improving the ADC dynamic performance was a major concern in all the simulations and experiments. From this achieved result, it is clearly

Figure 9.8. Dynamic performance of VCO-based ADC is graphically represented with respect to the change in input signal frequency.

serving the dynamic performance pictorial representation. While experimenting, the dynamic performance simulation analysis has identified the range of acceptable input frequencies. It is observed from the pictorial representation that the achieved SNR values do not drop drastically, in contradictory, all other dynamic metrics value increases. Therefore, on performing digital post correction, it could definitely improve the dynamic performance of this implemented VCO-based ADC design.

From the bandwidth simulation experiments, after 120 MHz input frequency all dynamic metrics values were found to be reduced or degraded. But this is not shown in the graphical representation, but the values have been reported in table 9.1. The sampling window holds for a same count as the input frequency increases the maximum oscillating frequency and this could be a reason for reduce in the metric values. Therefore, the implemented VCO-based ADC design was found to deliver a peak performance of an ENOB around 4.9-bit at 572 MHz sampling frequency over 120 MHz input signal frequency. Entire experimented simulation results have been tabulated in table 9.1.

9.3 Conclusions

The ADC dynamic performance has been experimented and simulated in various aspects in order to evaluate the implemented VCO-based ADC design performance. The VCO maximum linear tuning-range has been identified and an appropriate simulation has been performed to achieve the best dynamic performance results. Improving the ADC dynamic performance was a major concern in all the simulations and experiments. From this achieved result, it is clearly
understood that increasing the VCO tuning range will increase the ADC resolution. Digital post correction can also be performed if this tuning range can be further stretched. After different experiment, the VCO-based ADC was comfortably found to achieve above 4.5-bit of effective resolution over a bandwidth of 1 MHz to 120 MHz. The inherent noise-shaping property can also be viewed from the simulated and experiments.
Table 9.1. Achieved results of the VCO-based ADC design.

<table>
<thead>
<tr>
<th>s. no.</th>
<th>Sweep parameter</th>
<th>Verilog-A</th>
<th>Schematic</th>
<th>Peak-peak voltage (v)</th>
<th>DC voltage (v)</th>
<th>Input frequency (MHz)</th>
<th>SNR (dB)</th>
<th>SNDR (dB)</th>
<th>SFDR (dB)</th>
<th>ENOB (Bits)</th>
</tr>
</thead>
<tbody>
<tr>
<td>1.</td>
<td>DC voltage</td>
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<td>0.8</td>
<td>0.4</td>
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<td>42.56</td>
<td>37.62</td>
<td>50.03</td>
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<tr>
<td></td>
<td></td>
<td>✓</td>
<td></td>
<td>0.8</td>
<td>0.4</td>
<td>40</td>
<td>40.26</td>
<td>19.18</td>
<td>20.48</td>
<td>2.89</td>
</tr>
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<td></td>
<td></td>
<td>✓</td>
<td></td>
<td>0.7</td>
<td>0.35</td>
<td>40</td>
<td>40.68</td>
<td>24.77</td>
<td>27.58</td>
<td>3.82</td>
</tr>
<tr>
<td></td>
<td></td>
<td>✓</td>
<td></td>
<td>0.5</td>
<td>0.35</td>
<td>40</td>
<td>37.52</td>
<td>29.20</td>
<td>32.75</td>
<td>4.59</td>
</tr>
<tr>
<td>2.</td>
<td>Peak-peak voltage</td>
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<td></td>
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<td>0.35</td>
<td>40</td>
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<td>37.25</td>
<td>50.07</td>
<td>5.89</td>
</tr>
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<td></td>
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<td>0.35</td>
<td>40</td>
<td>37.52</td>
<td>29.20</td>
<td>32.75</td>
<td>4.59</td>
</tr>
<tr>
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<td></td>
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<td></td>
<td>0.6</td>
<td>0.35</td>
<td>40</td>
<td>39.77</td>
<td>27.09</td>
<td>29.97</td>
<td>4.20</td>
</tr>
<tr>
<td></td>
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<td></td>
<td>0.7</td>
<td>0.35</td>
<td>40</td>
<td>40.68</td>
<td>24.77</td>
<td>27.58</td>
<td>3.82</td>
</tr>
<tr>
<td>3.</td>
<td>Input frequency</td>
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<td>0.35</td>
<td>40</td>
<td>39.07</td>
<td>37.25</td>
<td>50.07</td>
<td>5.89</td>
</tr>
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<td>0.35</td>
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<td>29.20</td>
<td>32.75</td>
<td>4.59</td>
</tr>
<tr>
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<td></td>
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<td>37.45</td>
<td>31.61</td>
<td>34.61</td>
<td>4.95</td>
</tr>
<tr>
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<td></td>
<td>✓</td>
<td></td>
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<td>0.35</td>
<td>200</td>
<td>25.08</td>
<td>22.27</td>
<td>35.49</td>
<td>3.4</td>
</tr>
</tbody>
</table>
Chapter 10

Conclusions and discussion

In this thesis work we have presented a conventional time-based ADC architecture with the target for delivering high resolution, but usually such architecture benefits for high-speed applications. In the variety of time-resolution-based topologies, the main focus was to understand the conception working of a time-based ADC and then to experiment the implemented design for acquiring an effective high resolution.

After a detailed study on the time-resolution-based ADCs, a conventional VCO-based-ADC with multi-phase single-bit quantization architecture has been chosen due to the simplicity in design perspective and implementation aspects. The working principle of this time-based ADC has been clearly studied and then understood by implementing the design using cadence design environment. In the initial phase, an 8-bit VCO-based-ADC architecture has been behaviourally modelled for its functional verifications, where it consists of voltage-to-time and time-to-digital conversions. The voltage-to-time conversion is performed with the aid of a VCO model and time-to-digital conversion is performed using a one-bit counters combined with an adder model. The ADC dynamic performance has been analysed by using Matlab since it was easier or well suited for discrete-time analysis.

In the next phase, different architectures of each conversion blocks have been studied for implementing the VCO-based ADC design in transistor-level using a 65 nm CMOS process. Finally, the complete design corresponds to a ring-oscillator structure for the VCO, two D Flip-Flop and a XOR logic gate for the counter and parallel-counter logic for the adder circuit. The multi-phase voltage-controlled ring oscillator is implemented by 254 delay elements with each delay element comprise of PMOS cross-coupled structure and it is custom-designed, resulting at the maximum frequency tuning range of 77 MHz to 286 MHz. Later, the practically achieved maximum tuning range of the ring oscillator has been assigned for the behavioural realized VCO’s tuning range. Then, the behavioural model resulted in an ENOB around 5.8-bits for 40 MHz input signal frequency.

After certain experiments and analysis, the transistor-level VCO-based all-digital ADC design has found to deliver an expected performance of 37 dB SNR.
at 40 MHz signal frequency with 4.6 ENOB (29 dB SNDR) by without involving in any digital calibration techniques. At 120 MHz signal frequency, the design delivered a reasonable performance of 4.9-bits ENOB (31 dB SNDR) and a 34 dB of SFDR. Over a bandwidth of 1 MHz to 120 MHz the design was found to deliver an ENOB of more than 4.5-bits.

This VCO-based ADC design uses more digital components than any other traditional or classical ADCs for performing data conversion. In addition, this design also gets sophisticated in deep submicron CMOS technology node. A comparable performance in the resolution of the VCO-based all-digital ADC has been resulted from this work and provided that the design has a possibility for serving as an alternate approach for an analog-to-digital conversion.

10.1 Future work

Further extensions of this work can be performed and it could lead to a better performance in the VCO-based ADC design. From the experiments and simulation chapter, it was clearly understood that there is a direct relationship between the VCO's tuning linearity and the ADC’s output resolution. One simple attempt to improve the ADCs resolution is to select a VCO which provides a much wider frequency tuning range and along with linear transfer characteristics. Achieving such a VCO design could be an interesting attempt and can also be a challenging task.

Another attempt could be the ADC non-linear error correction and it can be achieved by using a post-digital error-correction technique. The digital calibration technique is based on by defining a possible approximation for the ADC’s transfer function. After choosing an approximation technique, a compensation code can be generated from the computed difference between the defined and the measured transfer functions. A careful measure has to be taken for observing the measured transfer function and also while defining the approximated transfer function. The VCO-based ADC’s static performance can also be performed through this correction attempt. There can also be other attempts, where these two are the possible future works for improving the implemented all-digital VCO-based ADC design performance.
Appendix A

Appendix

Using the Verilog-A modelling language, the behavioural-level of the VCO-based ADC design has been implemented using cadence design environment. Each subsystem of design has been individually coded as given below.

A.1 Verilog-A source code of VCO [35]

The following lines of Verilog-A code shows the behavioural model of the voltage-controlled oscillator. First, the desired output frequency (inst_freg) is computed by scaling the input sinusoidal signal. Then the phase is calculated by integration of the output frequency where the function idtmod is used for integration and modulus operation. The resulted output phase is used to generate the sinusoidal output of the VCO.

`include "constants.vams"
`include "disciplines.vams"
define PI 3.14159265358979323846264338327950288419716939937511

module digRfAdcVcoVcoahdl(vin, vout);
input vin;
output vout;
electrical vin, vout;
parameter real amp = 1;
parameter real center_freg = 1K;
parameter real vco_gain = 1K;
parameter integer steps_per_period = 32; // 02/20/2004, Fangyi
real phase; // 02/20/2004, Fangyi
real inst_freg; // instantaneous frequency

analog begin
inst_freg = center_freg + vco_gain * V(vin);
phase = idtmod(inst_freg,0,1);
V(vout) <+ amp * sin (2 * PI * phase);
A.2 Verilog-A source code of D flip-flop [35]

The following lines of Verilog-A code shows the behavioural model of the positive edge triggered D flip-flop.

```
`include "constants.vams"
`include "disciplines.vams"

module digRfAdcVcoDff(vin_d, vclk, vout_q, vout_qbar);
input vclk, vin_d;
output vout_q, vout_qbar;
electrical vout_q, vout_qbar, vclk, vin_d;
parameter real vlogic_high = 5;
parameter real vlogic_low = 0;
parameter real vtrans = 2.5;
parameter real tdel = 3u from [0:inf);
parameter real trise = 1u from (0:inf);
parameter real tfall = 1u from (0:inf);
real vtrans_clk;
integer x;

analog begin
  vtrans_clk=vlogic_high/2;
  @ (cross( V(vclk) - vtrans_clk, +1 ))
  x = (V(vin_d) > vtrans);
  V(vout_q) <+ transition( vlogic_high*x + vlogic_low!*x, tdel, trise, tfall );
  V(vout_qbar) <+ transition( vlogic_high!*x + vlogic_low*x, tdel, trise, tfall );
end

endmodule
```

A.3 Verilog-A source code of XOR gate [35]

The following Verilog-A code shows the excerpted high-level behavioural model of the XOR gate.

```
`include "discipline.h"
`include "constants.h"

module xor_gate(vin1, vin2, vout);
input vin1, vin2;
output vout;
```
A.4 MATLAB code for measuring dynamic performance

The time-domain analysis could be better estimated using cadence environment, whereas the frequency-domain analysis could be better estimated using MATLAB tool. The MATLAB code for measuring the spectral impurities of the output signal is given as below.

clear all;

electrical vin1, vin2, vout;
parameter real vlogic_high = 5;
parameter real vlogic_low = 0;
parameter real vtrans = 1.4;
parameter real tdel = 2u from [0:inf);
parameter real trise = 1u from (0:inf);
parameter real tfall = 1u from (0:inf);
real vout_val;
integer logic1, logic2;
analog begin
  @( initial_step ) begin
    if (vlogic_high < vlogic_low) begin
      $display("Range specification error. vlogic_high = (%E) less than vlogic_low = (%E).", vlogic_high, vlogic_low);
      $finish;
    end
    if (vtrans > vlogic_high || vtrans < vlogic_low) begin $display("Inconsistent threshold specification w/logic family.");
      $finish;
    end
    logic1 = V(vin1) > vtrans;
    logic2 = V(vin2) > vtrans;
    @ (cross(V(vin1) - vtrans, 1)) logic1 = 1;
    @ (cross(V(vin1) - vtrans, -1)) logic1 = 0;
    @ (cross(V(vin2) - vtrans, 1)) logic2 = 1;
    @ (cross(V(vin2) - vtrans, -1)) logic2 = 0;
    //
    // define the logic function.
    //
    vout_val = (logic1 ∧ logic2) ? vlogic_high : vlogic_low;
    V(vout) <+ transition( vout_val, tdel, trise, tfall);
  end
endmodule
close all;

% Chosen Input Parameters
fSignal = 119.96e6; % Input Frequency
fSample = 572e6; % Sampling Frequency
NOS = 4196; % Number of Samples collected from the simulation
Required_NOS = 4096;

% Reading the File
% Frequency 120MHz
adcOut = dlmread('/edu/manth906/digRf/digRfAdcVco/m/Fin119.96Msamples4196NEWamplitude25.txt');

%COLLECTING THE DATA
Time = adcout(:,1:1);
Output_Voltage_Levels = adcout(:,2:2);
Input_Voltage = adcout(:,17:17);

% Removing first few unwanted Samples
ADC_output_fcoh = Output_Voltage_Levels((NOS-2^12):NOS-1);
Plot_time = Time((NOS-(2^12)):NOS-1);
ADC_output_fcoh_ac = ADC_output_fcoh;

N_spect = length(ADC_output_fcoh_ac)/2;
X_spect = 1:fSample/(N_spect*2):(fSample/2);
adcOut_spect = spect20(ADC_output_fcoh_ac);
figure(4),semilogx(X_spect, adcout_spect ),xlabel('Frequency (Hz)'),ylabel('Magnitude (dB)'),title('Output Spectrum of VCO Based ADC');

resStruct = daisyAnalyzeFFT(ADC_output_fcoh_ac);
SNR_at_Output = resStruct.snr
SNDR_at_Output = resStruct.sndr
SFDR_at_Output = resStruct.sfdr
ENOB_at_Output = resStruct.enob
Bibliography


[29] Benchmark companies, D-latch flip-flops, ELT148 Digital Devices II.


[34] Lan Wei, Implementation of Pipelined Bit-parallel Adders, Student Thesis, Linköping University, September 2003.