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Effect of Clock Duty Cycle Error on Two-channel Interleaved $\Delta\Sigma$ DACs

Ameya Bhide, *Student Member, IEEE,* Amin Ojani, *Student Member, IEEE,*
and Atila Alvandpour, *Senior Member, IEEE*

***Abstract*—Time-interleaved $\Delta\Sigma$ (TIDSM) DACs have the potential for a wideband operation. The performance of a two-channel interleaved $\Delta\Sigma$ DAC is very sensitive to the duty-cycle of the half-rate clock. This paper presents a closed-form expression for the SNDR loss of such DACs due to duty cycle error for modulators with a noise transfer function of $(1-z^{-1})^n$. Adding a low-order FIR filter after the modulator helps to mitigate this problem. A closed-form expression for the SNDR loss in the presence of this filter is also developed. These expressions are useful for choosing a suitable modulator and filter order for an interleaved $\Delta\Sigma$ DAC in the early stage of the design process.**

***Index Terms*—digital $\Delta\Sigma$-modulator, duty cycle, DSM, DAC, FIR filter, time-interleaving.**

I. Introduction

HIGH-speed $\Delta\Sigma$ digital-to-analog converters (DACs) are of interest in the design of flexible radio transmitters [1]. They offer the benefit of relaxing the analog complexity by moving a part of the signal processing to the digital domain and can reduce the order of the reconstruction filter required after the DAC. Recent radio standards like Ultra-wideband (UWB) and 60-GHz WiGig have bandwidths ranging from hundreds of megahertz to a few gigahertz. Employing $\Delta\Sigma$ DACs for such wideband operation requires very high sampling rates of many-gigahertz due to the oversampling involved, which is very challenging to achieve using conventional architectures as the integrator in the modulator becomes a bottleneck. Time-interleaved $\Delta\Sigma$ (TIDSM) DACs are hence required to relax the critical path of the integrator logic in the digital $\Delta\Sigma$ modulator, which improves the overall throughput and effective sampling rate [2]–[4].

Figure 1 shows the general structure of a two-channel TIDSM DAC that implements a noise transfer function (NTF) of $1-H(z)$. The digital modulator is now implemented as a 2 $\times$ 2 block digital filter containing the two polyphase components of $H(z)$ [5] and operates at a relaxed half-sampling-rate frequency of $f_s/2$. At high sampling rates, driving the DAC directly with the full-rate f_s clock becomes a challenge or this f_s clock can be sometimes unavailable. Additionally, a return-to-zero (RZ) DAC may be required for improved dynamic performance [6]. In these cases, the two generated polyphase outputs, y_0 and y_1 are then multiplexed by the same half-rate

Manuscript received Oct 13, 2014. This work was supported by the Swedish Foundation for Strategic Research (SSF).The authors are with the Department of Electrical Engineering, Linköping University, SE-58183, Linköping, Sweden. Email: {ameya,amin,atila}@isy.liu.se.

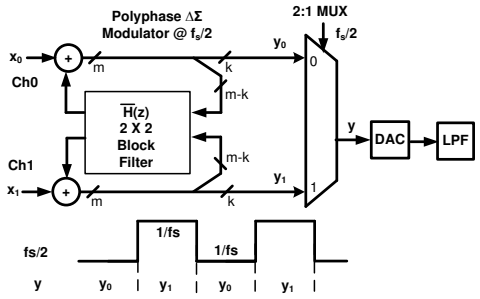


Fig. 1. Block diagram of a generic two-channel interleaved $\Delta\Sigma$ DAC implementing a noise transfer function $1-H(z)$.

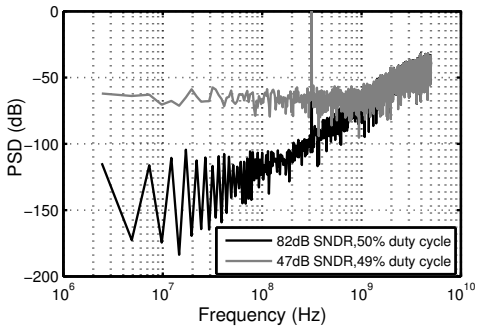


Fig. 2. Effect of 1% DCE on SNDR for a 4-bit DAC with f_s=10 GHz, OSR=16 (BW=312.5 MHz) and NTF of $(1-z^{-1})^3$.

$f_s/2$ clock to an effective f_s sampling rate and then fed to the DAC [2] [6]. The final full-rate multiplexing before the DAC is sensitive to both the edges of the $f_s/2$ clock as new data is presented to the DAC on both the edges. As long as the duty cycle of this clock is 50%, both the channels are reconstructed for a time $1/f_s$ as desired. However, if the duty cycle is not 50%, then a sampling time error is introduced into the DAC that results in a SNDR loss. Figure 2 illustrates the severity of the effect of this duty cycle error (DCE) in a 4-bit 10 GS/s two-channel wideband TIDSM DAC with a third-order NTF of $(1-z^{-1})^3$. At an oversampling ratio (OSR) of 16 (bandwidth=312.5 MHz), simulations show that even a 1% duty cycle error (i.e. duty cycle is 49% or 51%) in the half-rate 5 GHz clock results in a SNDR loss of 35 dB. Achieving an exact 50% clock duty-cycle at high speeds is very challenging. Although clock generators often employ duty cycle correction [7] or utilize a master clock that is first divided down by two to achieve a 50% duty cycle, there still exists a residual DCE [6]. Hence, it is of importance to analyze and estimate the effect of DCE on two-channel TIDSM DACs.

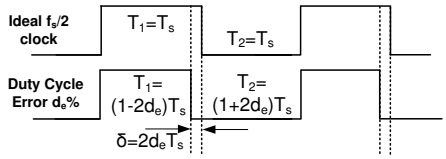


Fig. 3. Half-rate sampling clock of frequency $f_s/2$ and DCE = d_e%.

The effect of DCE on TIDSM DACs has received very less attention in the literature. Previous works [8], [9] have focused only on the analysis of sampling time errors in non-interleaved Nyquist and $\Delta\Sigma$ DACs resulting from stochastic clock jitter, which is not applicable in the case of a deterministic error like the DCE. In [10], the effect of time-average frequency (TAF) and flying-adder (FA) clocks on non-interleaved Nyquist DACs has been studied and a closed-form expression for the SDR is presented. A half-rate clock with a DCE behaves similarly as a FA clock and hence the analysis performed in [10] is used as a starting point to analyze the DCE effect on SNDR of TIDSM DACs.

In this work, a new closed-form expression for SNDR loss due to the DCE is derived for modulators of the type, NTF=$(1-z^{-1})^n$. It is further shown that the effect of DCE can be mitigated similarly as stochastic clock jitter by adding a low-order FIR filter between the modulator and the multiplexer that attenuates the high frequency noise [12]. A closed-form expression for estimating the SNDR loss in the presence of this filter is also developed. These expressions are useful as a suitable modulator and filter order that takes the DCE problem into account can be chosen in the very early phase of the design. The method presented in this work can be extended to any other NTF.

II. Mathematical Formulation of the SNDR Loss

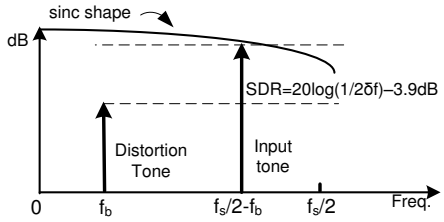
Figure 3 shows a clock of frequency $f_s/2$ having a DCE of d_e% i.e. a duty cycle variation from 50%. This means that the effective sampling time is of the form $T_1T_2T_1T_2...$ and so on. Let δ be the sampling time error in each sample given by $\delta = |2d_eT_s|$. Now, initially assume that this clock drives an interleaved Nyquist DAC (see Fig. 4(a)) which has a single input tone at a frequency of $f = f_s/2 - f_b$ that is greater than $f_s/4$. Then it has been shown in [10] and more recently [11] that such a clock of the form $T_1T_2T_1T_2...$ produces a distortion tone at a frequency of f_b i.e. the tone at $f_s/2 - f_b$ folds back to f_b and the signal-to-distortion ratio (SDR) of this DAC in dB is given by

$$\text{SDR} = 20\log\left(\frac{1}{2\delta f}\right) - 3.9 \tag{1}$$

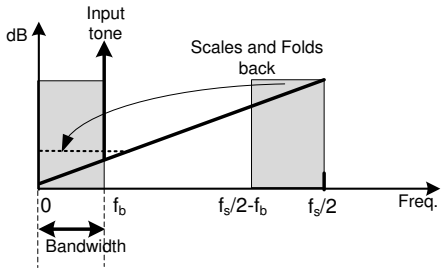
Equation (1) can be rewritten as

$$\text{SDR} = 20\log\left(\frac{f_s}{2\pi d_e f}\right) \tag{2}$$

Equation (2) calculates the SDR after the DAC that also accounts for the sinc shaping. Notice that if the input frequency tone, f is close to $f_s/2$, then it is scaled by the DAC sinc shaping while the distortion tone (close to 0) remains nearly unaffected by the sinc function. Since the error is introduced



(a) DCE Effect on a two-channel Nyquist DAC.



(b) DCE Effect on a two-channel TIDSM DAC.

Fig. 4. Folding effect of DCE on time-interleaved Nyquist and DSM DACs.

during the multiplexing, SDR can be also referred to the output of the multiplexer and before the DAC (refer Fig. 1).

$$\begin{aligned}\text{SDR}_{\text{mux}} &= 20\log\left(\frac{f_s}{2\pi d_e f}\right) + 20\log\left[\frac{\pi f/f_s}{\sin(\pi f/f_s)}\right] \\ &= 20\log\left[\frac{1}{2d_e\sin(\pi f/f_s)}\right]\end{aligned} \tag{3}$$

Now, consider the case of an interleaved $\Delta\Sigma$ DAC as shown in Fig. 4(b). Let the main input tone be located at f_b with 0 to f_b being the band of interest. Analogous to the case of the Nyquist DAC, the shaped noise at high frequencies will cause distortion tones at lower frequencies. More specifically, high frequency noise power in the frequencies from $f_s/2 - f_b$ to $f_s/2$ will be scaled by (3) and fold back into the frequency band from 0 to f_b, causing an SNDR loss. Also, note that for $f_b << f_s/2$, the SNDR in the desired band from 0 to f_b remains nearly unaffected by the sinc shaping of the DAC i.e. the SNDR after the multiplexer is approximately equal to the SNDR after the DAC.

Let the quantization noise power in the band of interest for an ideal TIDSM DAC be N_q and the signal (input tone) power be S. Let the total folded noise power into the band due to the DCE be N_f. The ideal SNDR is then given by S/N_q while $S/(N_q+N_f)$ is the reduced SNDR. A "noise figure" term for the TIDSM DAC that specifies the amount of relative SNDR loss in dB in the presence of DCE can then be defined as

$$F|_{dB} = 10\log\left(1 + \frac{N_f}{N_q}\right) \tag{4}$$

It can be noted that (4) is independent of the signal power i.e. number of DAC bits since N_q and N_f are functions of the NTF and OSR only. For a given NTF and an OSR, N_q and N_f can be computed to obtain a closed-form expression for F using (3) and (4).

III. Expression for SNDR Loss due to DCE

Assume that an n^{th}-order modulator with an NTF of the form $(1-z^{-1})^n$ is used and the bandwidth of interest is f_b,

similar to Fig. 4(b). Then,

$$|NTF(f)| = |1 - e^{-2j\frac{\pi f}{f_s}}|^n = \left[2\sin\left(\frac{\pi f}{f_s}\right)\right]^n \quad (5)$$

N_q is given by

$$N_q = \int_0^{f_b} |NTF(f)|^2 df \quad (6)$$

Due to the oversampling, assuming that $f_b << f_s/2$ gives $\sin\left(\frac{\pi f}{f_s}\right) \approx \frac{\pi f}{f_s}$. With OSR = $f_s/(2f_b)$, using (5) in (6) yields

$$N_q = \frac{\pi^{2n} f_s}{2(2n+1)OSR^{2n+1}} \quad (7)$$

Using (3), the folded noise power N_f can be written as

$$N_f = \int_{\frac{f_s}{2}-f_b}^{\frac{f_s}{2}} \left[2d_e \sin\left(\frac{\pi f}{f_s}\right)\right]^2 |NTF(f)|^{2n} df$$

$$N_f = 2^{2n+2} {d_e}^2 \int_{\frac{f_s}{2}-f_b}^{\frac{f_s}{2}} \sin^{2n+2}\left(\frac{\pi f}{f_s}\right) df \quad (8)$$

Changing the integral limits from 0 to f_b yields

$$N_f = 2^{2n+2} {d_e}^2 \int_0^{f_b} \sin^{2n+2}\left[\frac{\pi}{f_s}\left(\frac{f_s}{2} - f\right)\right] df$$

$$= 2^{2n+2} {d_e}^2 \int_0^{f_b} \cos^{2n+2}\left(\frac{\pi f}{f_s}\right) df \quad (9)$$

For $f_b << f_s/2$, $\cos(\frac{\pi f}{f_s}) \approx 1$. Eq. (9) simplifies to

$$N_f = \frac{2^{2n+1} {d_e}^2 f_s}{OSR} \quad (10)$$

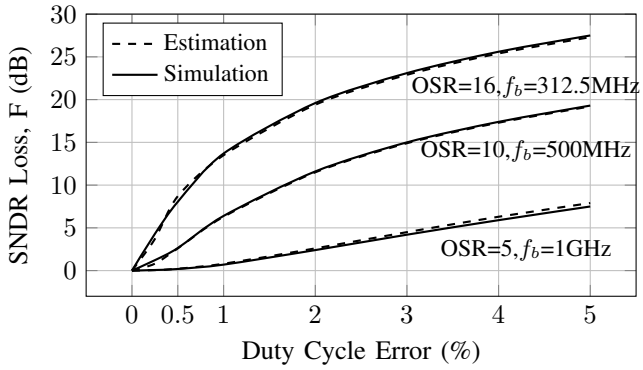
Now, using (7) and (10) in (4) yields

$$F|_{dB} = 10\log\left[1 + \frac{2^{2n+2}(2n+1){d_e}^2 OSR^{2n}}{\pi^{2n}}\right] \quad (11)$$

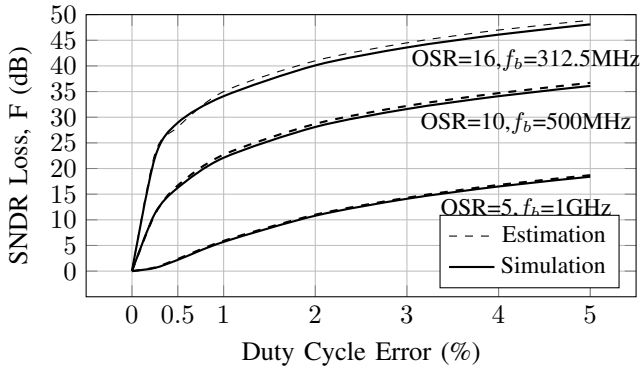
Thus, a closed-form expression for the SNDR loss, F due to a DCE of d_e% has been obtained. Equation (11) shows that in the presence of DCE, the dominant term that contributes to the SNDR loss is $(2\text{OSR}/\pi)^{2n}$.

IV. Validation of Expression for SNDR Loss

In order to validate (11), a 10 GS/s two-channel TIDSM DAC with 13-bit digital input and 4-bit DAC is chosen. The NTFs chosen for simulation are $(1-z^{-1})^2$ and $(1-z^{-1})^3$ i.e. second and third-order modulators respectively. Simulations are carried out for three values of OSR i.e. 16 (f_b=312.5 MHz), 10 (f_b=500 MHz) and 5 (f_b=1 GHz). These modulator orders and bandwidths are chosen as they are of potential interest in wideband applications for UWB and 60-GHz radio. The digital modulator is implemented as a discrete-time model in Matlab® while transient circuit simulations are performed for the multiplexer and the DAC in Cadence® Spectre®. Ideal multiplexer and DAC models are utilized and the DCE of the $f_s/2$ clock is parametrically varied from 0% to 5%. The DAC output is filtered with a Bessel low-pass filter having a bandwidth of f_b prior to measuring the SNDR. In all cases, the number of FFT points chosen is 2^{14} and a 0 dBFS single tone input of frequency f_b is used.



(a) NTF=$(1-z^{-1})^2$.



(b) NTF=$(1-z^{-1})^3$.

Fig. 5. Simulation versus Estimation of SNDR loss for a 10 GS/s TIDSM DAC for (a) second-order (n=2) and (b) third-order (n=3) modulators.

Figures 5(a) and 5(b) show the comparison between the simulated and estimated SNDR loss for the three OSR values and the two modulators respectively. The estimation using the linear quantizer model of the modulator (Eq. (11)) matches closely with the transient simulated SNDR loss with a less than 0.9 dB error. This demonstrates that the analysis in the preceding sections is valid and can be used to estimate the performance of the TIDSM DAC.

Equation (11) and the simulation results show that a higher OSR and n results in a higher SNDR loss. This makes higher OSR and higher order modulators more susceptible to the duty cycle problem. Higher order modulators are used because they yield more noise-shaping and hence a higher SNDR in the bandwidth of interest. Due to the high sensitivity of (11) to n, it can then so happen that the benefit of using a higher order modulator is nullified by the SNDR loss due to the DCE. In other words, it is possible that a lower order modulator shows a better performance than the higher order one above a certain value of DCE for a given value of OSR. In order to demonstrate this problem, consider that I_n is the improvement in the ideal SNDR obtained by using a $(n+1)^{\text{th}}$-order modulator over an n^{th}-order one. Then, from (7) we have

$$I_n = \frac{N_{q,n}}{N_{q,n+1}} = \frac{(2n+3)}{(2n+1)}\frac{OSR^2}{\pi^2} \quad (12)$$

Similarly, the ratio between the SNDR loss due to the DCE from an $(n+1)^{\text{th}}$-order modulator and an n^{th}-order one, L_n

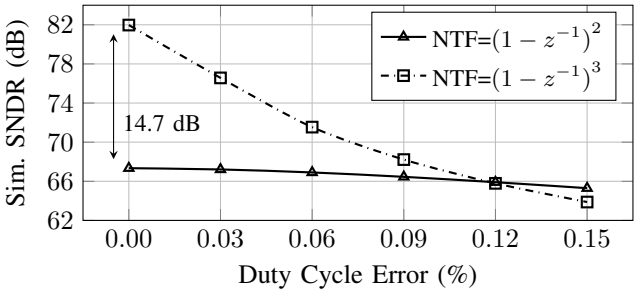


Fig. 6. Second-order modulator shows a better SNDR than third-order for OSR=16 and $d_e > 0.12\%$ as predicted by (15).

is calculated from (11) as

$$L_n = \frac{F_{n+1}}{F_n} = \frac{\pi^{2n+2} + 2^{2n+4} d_e^2 (2n+3) OSR^{2n+2}}{\pi^2[\pi^{2n} + 2^{2n+2} d_e^2 (2n+1) OSR^{2n}]} \quad (13)$$

Now equating I_n and L_n, a limit for d_e can be obtained above which an n^{th}-order modulator starts showing a better performance over an $(n+1)^{\text{th}}$-order one.

$$d_e = \sqrt{\frac{\pi^{2n}[(2n+3)OSR^2 - (2n+1)\pi^2]}{3(2n+3)(2n+1)2^{2n+2} OSR^{2n+2}}} \quad (14)$$

In order to obtain the value of d_e for a comparison between a second and a third-order modulator, substituting n=2 in (14) yields

$$d_e = \sqrt{\frac{7\pi^4 OSR^2 - 5\pi^2}{6720 \cdot OSR^6}} \quad (15)$$

For OSR=16, (15) results in a value of d_e=0.12%. This means that the duty cycle of the clock must be between the values 49.88% and 50.12% in order to obtain a benefit on the third-order modulator over a second-order. This requirement is extremely stringent and becomes even stricter as the OSR increases. On the other hand, for a more wideband operation with an OSR of 5, this limit of d_e becomes 1.08%. This is a more relaxed requirement on the clock. Thus, a higher order modulator is more suitable for operation with a low OSR.

In order to check the validity of (15), transient simulations of the obtained SNDR for the second and third-order modulators are also performed for small values of d_e between 0% and 0.15% when OSR=16. Fig. 6 shows the obtained simulation results. For no DCE, the third-order modulator has a simulated 14.7 dB higher SNDR (15.6 dB predicted by (12)). Exactly as predicted by (15), the performance of the third-order modulator drops below that of the second one for d_e as small as 0.12%.

V. Mitigating DCE Effect With Digital Filtering

The analysis in the preceding sections suggests that the amount of high-frequency noise that folds back into the bandwidth of interest must be reduced in order to mitigate the effect of the DCE. This means that the high-frequency shaped noise must be filtered out prior to the multiplexer. The magnitude of the shaped noise is the highest at $f_s/2$. Hence, introducing zero(es) at $f_s/2$ can limit the noise folded back into the desired band. FIR low-order low-pass filters having a transfer function of the type, $G(z) = (1+z^{-1})^m$

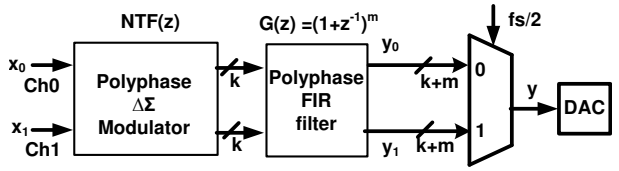


Fig. 7. Interleaved $\Delta\Sigma$ DAC with a FIR filter to reduce the effect of the DCE.

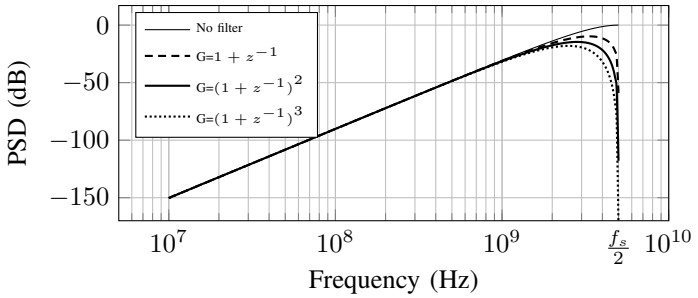


Fig. 8. Frequency response of a 10 GS/s TIDSM DAC noise-shaping with NTF(z)=$(1-z^{-1})^3$ in presence of the FIR filter.

(where m is the order) are of particular interest as they fulfill this requirement and have a very small attenuation in the desired band. Moreover, these filters can be implemented in a multiplier-less architecture making them suitable for high-speed operation. For third-order and above, other filter transfer functions e.g. [1 2 2 1] could be of interest as they have power-of-2 coefficients. However, [1 2 2 1] results in a much lesser attenuation close to $f_s/2$ compared to $(1+z^{-1})^3$. Hence, for the discussion in this section, only $G(z) = (1+z^{-1})^m$ is considered. Figure 7 shows the block diagram of a TIDSM DAC with such a filter which is also implemented with a polyphase architecture. The FIR filter must be of a low order because it increases the number of DAC bits. For every one order increase in the filter, the number of DAC bits increases by one. Hence, the FIR filtering comes at the expense of the DAC cell matching. Figure 8 shows the frequency response of the shaped noise in the presence of such a filter.

It is of interest to estimate the performance of the TIDSM DAC in the presence of the filter. Hence, a closed-form expression for the SNDR loss, F can be developed in this case as well. Such an expression for the TIDSM DAC is useful for the co-design of the modulator and the filter.

VI. Expression for SNDR Loss with FIR Filter

With $G(z) = (1+z^{-1})^m$,

$$|G(f)| = |1 + e^{-2j\frac{\pi f}{f_s}}|^m = \left[2\cos\left(\frac{\pi f}{f_s}\right)\right]^m \quad (16)$$

Then, the quantization noise power, N_q is given by

$$N_q = \int_0^{f_b} |NTF(f)|^{2n} |G(f)|^{2m} df \quad (17)$$

For $f_b << f_s/2$, $\cos(\frac{\pi f}{f_s}) \approx 1$ and $\sin(\frac{\pi f}{f_s}) \approx \frac{\pi f}{f_s}$, thus (17) simplifies to

$$N_q = \frac{\pi^{2n} 2^{2m} f_s}{2(2n+1) OSR^{2n+1}} \quad (18)$$

Using (3) and (16), the folded noise power N_f can be written as

$$N_f = \int_{\frac{f_s}{2}-f_b}^{\frac{f_s}{2}} \left[2d_e \sin\left(\frac{\pi f}{f_s}\right)\right]^2 |NTF(f)|^{2n}|G(f)|^{2m} df$$

$$N_f = 2^{2n+2m+2} {d_e}^2 \int_{\frac{f_s}{2}-f_b}^{\frac{f_s}{2}} \sin^{2n+2}\left(\frac{\pi f}{f_s}\right)\cos^{2m}\left(\frac{\pi f}{f_s}\right) df$$

Changing the integral limits from 0 to f_b yields

$$N_f = 2^{2n+2m+2} {d_e}^2 \int_0^{f_b} \sin^{2n+2}\left[\frac{\pi}{f_s}\left(\frac{f_s}{2}-f\right)\right] \cos^{2m}\left[\frac{\pi}{f_s}\left(\frac{f_s}{2}-f\right)\right] df \quad (19)$$

$$N_f = 2^{2n+2m+2} {d_e}^2 \int_0^{f_b} \cos^{2n+2}\left(\frac{\pi f}{f_s}\right)\sin^{2m}\left(\frac{\pi f}{f_s}\right) df$$

Further simplification results in

$$N_f = \frac{2^{2n+1}\pi^{2m} {d_e}^2 f_s}{(2m+1)OSR^{2m+1}} \quad (20)$$

Now, using (4), (18) and (20), the SNDR loss, F in the presence of the filter is simplified to

$$F = 10\log\left[1 + \frac{2^{2(n-m+1)} {d_e}^2 (2n+1)OSR^{2(n-m)}}{(2m+1)\pi^{2(n-m)}}\right] (21)$$

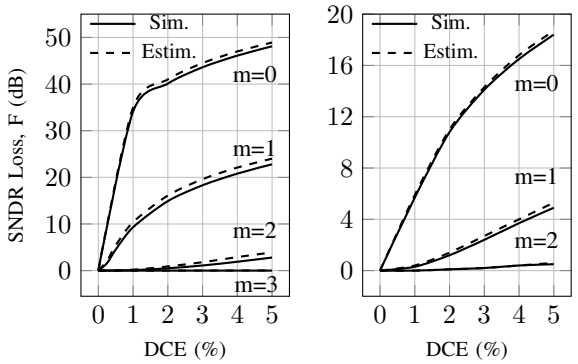
Firstly, it can be seen from (21) that m=0 represents the condition of no filter and simplifies to (11) as expected. Equation (21) intuitively also shows the improvement in the overall SNDR due to the filter. While (11) is a function of $(2OSR/\pi)^{2n}$, (21) is a function of $(2OSR/\pi)^{2(n-m)}$. Hence, increasing the filter order m improves the performance of the DAC. At $n = m$, the SNDR loss, F is no more a function of the OSR and achieves a near immunity to d_e.

A. Validation of SNDR Loss with FIR Filter

In order to validate the preceding analysis, transient simulations are now performed on the 10 GS/s TIDSM DAC with the filter included for n=3 with OSR=16 and OSR=5. The DCE is swept from 0 to 5% while the filter order is swept from 0 to 3. Figures 9(a) and 9(b) show that the simulated SNDR loss, F matches closely with the estimation from (21) with a less than 1.3 dB error.

For the case of OSR=16 (Fig. 9(a)), the first-order filter (m=1) shows a drastic improvement in performance e.g. a 24 dB improvement for d_e=1%. However, the SNDR loss is still high even with m=1. A second-order filter (m=2) shows a very good immunity to DCE with the loss being less than 4 dB for d_e as high as 5% and less than 0.5 dB for d_e=2%. Filter order of three results in near immunity to the DCE with a less than 0.05 dB loss due to DCE. For the case of OSR=5 (Fig. 9(b)), m=1 itself could be a sufficient option as it shows a <1.3 dB SNDR loss for d_e upto 2%.

As mentioned previously, the immunity to DCE with an m^{th}-order filter comes at the cost of m additional DAC bits. In other words, the overall DAC moves from being DCE-limited to matching-limited. Hence, mismatch shaping may be additionally required in the presence of the filter.



(a) OSR=16, f_b=312.5 MHz. (b) OSR=5, f_b=1 GHz.

Fig. 9. Simulation versus estimation of SNDR loss of a 10 GS/s TIDSM DAC for n=3 as a function of filter order, m and OSR from (21).

VII. Conclusions

This paper mathematically analyzes the effect of DCE on two-channel TIDSM DACs with NTF=$(1-z^{-1})^n$. The TIDSM DAC is found to be very sensitive to this error which limits the overall performance. A closed-form expression that estimates the performance loss due to the DCE is derived. Adding a low-order FIR filter can mitigate the effect of DCE. The expression is further extended to include the effect of the filter. The presented method can be extended to other NTFs. This analysis is useful as these expressions support a duty cycle "aware" design process for wideband TIDSM DACs.

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