A 11-GS/s 1.1-GHz Bandwidth Interleaved ΔΣ DAC for 60-GHz Radio in 65-nm CMOS

Ameya Bhide and Atila Alvandpour

Ameya Bhide and Atila Alvandpour, A 11-GS/s 1.1-GHz Bandwidth Interleaved ΔΣ DAC for 60-GHz Radio in 65-nm CMOS, 2015, IEEE Journal of Solid-State Circuits, (PP), 99, 1-13.
http://dx.doi.org/10.1109/JSSC.2015.2460375

An 11-GS/s 1.1-GHz Bandwidth Interleaved $\Delta\Sigma$ DAC for 60-GHz Radio in 65-nm CMOS

Ameya Bhide, *Student Member, IEEE*

and Atila Alvandpour, *Senior Member, IEEE*

Department of Electrical Engineering, Linköping University, SE-58183, Linköping, Sweden.

Email: {ameya,atila}@isy.liu.se.

ABSTRACT

This work presents an 11 GS/s 1.1 GHz bandwidth interleaved $\Delta\Sigma$ DAC in 65 nm CMOS for the 60-GHz radio baseband. The high sample rate is achieved by using a two-channel interleaved MASH 1-1 architecture with a 4-bit output resulting in a predominantly digital DAC with only fifteen analog current cells. Two-channel interleaving allows the use of a single clock for the logic and the multiplexing which requires each channel to operate at half sampling rate of 5.5 GHz. To enable this, a look-ahead technique is proposed that decouples the two channels within the integrator feedback path thereby improving the speed as compared to conventional loop-unrolling. Measurement results show that the $\Delta\Sigma$ DAC achieves a 53 dB SFDR, -49 dBc IM3 and 39 dB SNDR within a 1.1 GHz bandwidth while consuming 117 mW from 1 V digital/1.2 V analog supplies. Furthermore, the proposed $\Delta\Sigma$ DAC can satisfy the spectral mask of the IEEE 802.11ad WiGig standard with a second order reconstruction filter.

Keywords – $\Delta\Sigma$ DAC, time-interleaving, MASH, 60-GHz radio, high-speed, IEEE 802.11ad, WiGig.

I. INTRODUCTION

The increasing demand for high-data-rate short-range wireless communication has led to the evolution of the unlicensed 60-GHz radio band ($57.2-65.8$ GHz) which has a continuous bandwidth of 9 GHz. This has resulted in the development of recent standards, such as WiGig (IEEE 802.11ad) [1], ECMA-387 [2] and WirelessHD [3]. These standards have divided the 60-GHz band into four channels, each having a 1.76 GHz (I+Q paths) RF channel bandwidth (BW).

Digital-to-analog converters (DAC) form a part of the transmitter baseband and are required to have a wide bandwidth greater than 880 MHz (in both, I & Q paths to enable the 1.76 GHz channel BW) and a resolution greater than $6-8$ bits to support the different modulation schemes of these standards [4]–[8]. Most of the DACs reported in literature for 60-GHz radio have so far used a conventional approach with a $2\times$ digital interpolation of the baseband, followed by a Nyquist current-steering DAC and a fourth or fifth order passive LC-analog anti-aliasing filter, which then connects to an up-conversion mixer [4] [7]. This approach is shown in Fig. 1(a). The passive filters occupy a large on-chip area and have a low quality factor [8]. While some low-area high-order wideband active filters have also been recently reported [9] [10], they are challenging to design and impact the transmitter linearity.

With the advances in CMOS scaling, there is a trend of using digital processing to move the analog functionality of the RF transceivers to the digital domain for easy configurability and relaxing the analog circuit requirements. Some examples of these techniques in transmitters include oversampling/interpolation filtering to reduce the anti-aliasing filter order and the use of $\Delta\Sigma$ modulation to reduce the number of DAC unit cells [11]–[15]. However, these techniques have been applied only for relatively low channel-bandwidth standards (<160 MHz) e.g. WLAN, WiMAX, UMTS, WCDMA and UN-II bands where the carrier frequencies are

only a few gigahertz.

Applying similar techniques to 60-GHz radio is challenging due to its large BW which results in a very high speed requirement from the digital processing. Nevertheless, there is an emerging trend towards digital architectures for the 60-GHz band. A 7-bit oversampling interpolation digital FIR filter before the DAC operating at $9.6\,$GS/s is presented in [8]. This oversampling filter, along with the sinc response of a Nyquist DAC, can satisfy the spectral mask of the WiGig standard without an anti-aliasing filter and allow the DAC to directly connect to the mixer. This digital oversampling based architecture is shown in Fig. 1(b). However, this architecture now requires a Nyquist DAC with at least $6-8$ bits of resolution and operating at a high sample rate of $\sim 10\,$GS/s. The design of this DAC is challenging as this may require the use of analog techniques such as use of sub-DACs or dual-current cells with higher matching requirements, special DAC switching schemes e.g. quad-switching, clocking schemes with extensive phase calibration and threshold voltage calibration of the switch to correct timing errors [16]–[18].

A third potential architecture that still uses a digital oversampling filter but now instead uses a $\Delta\Sigma$ DAC instead of the Nyquist DAC is shown in Fig. 1(c). In this scenario, the $\Delta\Sigma$ DAC can further enable this trend towards digital architectures by using digital processing to reduce the number of DAC unit cells and hence the overall DAC complexity. However, $\Delta\Sigma$ DACs have the drawback of a large out-of-band shaped quantization noise which needs to be filtered out to meet the spectral mask of the WiGig standard. If the order of the filtering can be restricted to a first or a second order, then a good trade-off between the high filter order of the conventional transmitter (Fig. 1(a)) and the large complexity of a high-speed Nyquist DAC in the interpolation-based architecture (Fig. 1(b)) can be achieved. The $\Delta\Sigma$ DAC (Fig. 1(c)) can thus present an intermediate digital solution.

Based on the foregoing discussion, the $\Delta\Sigma$ DAC is required to work at $\sim 10\,$GS/s and

provide a BW>880 MHz. $\Delta\Sigma$ DACs have not been targeted for this high bandwidth and sample rate because of the speed limitation of the integrator (feedback path) in conventional digital $\Delta\Sigma$ modulators (DSM). Hence, time-interleaved $\Delta\Sigma$ modulators (TIDSM) that use a poly-phase decomposition (loop-unrolling) of the integrator are required to relax the critical path in the modulator [19]–[23]. Using this concept, MASH based TIDSMs that achieve 8 GS/s [20], [23] and a $\Delta\Sigma$ DAC with 200 MHz BW [20] have been previously reported. However, these loop-unrolled architectures are eventually limited by the critical path of the integrator and the final full-rate-multiplexing that makes a greater than 10 GS/s speed very challenging. Hence, this work presents a two-channel MASH look-ahead time-interleaved $\Delta\Sigma$ modulator (LA-TIDSM) that reduces the critical path of a conventional loop-unrolled MASH TIDSM by modifying the execution order of the computations, while the two-channel architecture allows a single clock design with a simplified final multiplexing.

A two-channel LA-TIDSM MASH $1-1$ DAC with an 8-bit digital input and a 4-bit DAC that achieves 11 GS/s and 1.1 GHz bandwidth is presented in this work. This DAC along with a second order low pass filter can support the spectral mask of the IEEE 802.11ad WiGig standard for the 60-GHz band. The remainder of this paper is organized as follows. Sections II and III describe the modulator choice and the LA-TIDSM architecture respectively. Sections IV and V describe the implementation of the LA-TIDSM DAC and the testing methodology using an on-chip testing memory. Finally, the measurement results and the conclusions are presented in Sections VI and VII respectively.

II. Modulator Architecture

In order to support modulation schemes from BPSK to 16-QAM, the $\Delta\Sigma$ DAC is targeted for a >40 dB SNDR in a bandwidth of 880 MHz [11]. The DSM should operate at a multiple of the reference sampling rate, which is 1.76 GHz in Single Carrier (SC) mode for the WiGig

standard. The order of the DSM also affects the out-of-band quantization noise and hence the filter order required to meet the spectral mask. In addition to these constraints, the number of channels in the TIDSM based DAC and the choice of the final full-rate-multiplexing (serializer) strategy also influences the choice of the DSM order and the achievable SNDR.

Fig. 2 shows a generic two-channel TIDSM architecture that is obtained by loop-unrolling a conventional DSM. The two-channel TIDSM shown in Fig. 2 implements a NTF(z)=1−H(z) and operates at a relaxed half-sampling rate of $f_s/2$. The DSM is implemented as a 2×2 block digital filter that contains the two poly-phase components of H(z) [19]. The two outputs are then multiplexed by the same half-rate-clock to the full sampling rate of f_s. While a larger number of channels can further relax the critical path in the DSM [21], the final full-rate-multiplexing now requires accurate multiphase clock generation which is challenging at high frequencies [16], [23]. Hence, two-channel TIDSM DACs are of particular interest as they use only a single half-rate-clock for the DSM and the multiplexing, thus keeping a low clocking complexity while still relaxing the DSM critical path. The multiplexing and the overall DAC performance of this two-channel architecture is sensitive to the duty cycle of the $f_s/2$ clock. A duty cycle error (DCE) in the $f_s/2$ clock i.e. a variation from 50% duty cycle directly impacts the SNDR of the TIDSM DAC since this results in a timing skew between the two channels. The SNDR loss results from the folding of the high-frequency shaped noise between $f_s/2 - f_{in}$ and $f_s/2$ back into the BW of interest that lies between 0 and f_{in}. It has been shown in [24] that the loss in SNDR, $L_{\Delta\Sigma}$ from this noise folding in a TIDSM DAC due to a DCE of $d_e\%$ is given by

$$L_{\Delta\Sigma}|_{dB} = 10\log\left[1 + \frac{2^{2n+2}(2n+1){d_e}^2\text{OSR}^{2n}}{\pi^{2n}}\right] \tag{1}$$

where NTF(z)=$(1-z^{-1})^n$, n represents the DSM order and OSR(=f_s/(2BW)) is the over-sampling ratio. Although duty cycle correction or a double frequency clock that is divided

down to achieve a 50% duty cycle can be employed to mitigate this problem, there still exists some residual DCE [16], [25]. This suggests that an increased SNDR is required as a margin to accommodate some amount of DCE. It can further be noted that the DCE does not affect the SFDR of the $\Delta\Sigma$ DAC. The interleaving spurs resulting from the band between 0 and f_{in} appear in the band between $f_s/2 - f_{in}$ and $f_s/2$. Hence, these tones are also filtered out by the anti-aliasing filter.

Table I shows the different possible alternatives for the TIDSM DAC in the presence of above mentioned constraints. The SNDR is estimated for a 0 dBFS sine wave at 880 MHz and a DCE error of 1% i.e. the clock duty cycle is between 49% and 51% (a 2 ps timing error at 10 GS/s). In order to estimate the filter order needed, the baseband signal is assumed to be first up-sampled and pulse shaped with a 0.25 roll-off root-raised-cosine (RRC) filter prior to the TIDSM [7]. The TIDSM uses an 8-bit input data from the filter and an NTF(z)=$(1 - z^{-1})^n$. It can firstly be seen from Table I that the fourth option with an OSR of 7 and a first order filter is the most desirable option but the 12.32 GS/s sample rate is very challenging. The third option with 10.56 GS/s, 4-bit DAC and a second order filter is the next best that can achieve the 40 dB SNDR. It can be further seen from Table I and Eq. (1) that a third order DSM does not yield a better SNDR in the presence of 1% DCE. Thus, the second order TIDSM with a 4-bit DAC and operating at >10.56 GS/s is chosen as the design target. The unit cell current matching (σ) for the 4-bit thermometer coded DAC was chosen such that the SNDR loss due to mismatch is less than that produced by a 1% DCE. Monte-Carlo simulations showed that $\sigma < 1.1\%$ satisfies this requirement. Fig. 3 shows the WiGig spectral mask that can be met this chosen DAC option and a second order filter.

III. Proposed Look-Ahead Time-Interleaved Modulator

The traditional MASH DSM architecture that consists of a cascade of first-order error-feedback (EFB) DSMs (Fig. 4) is a very attractive candidate for high-speed implementation due to two main reasons [11], [12]. Firstly, the critical path is the shortest, corresponding to one adder delay, and restricted within each of the individual modulators. Any critical path spanning across the different cascade stages can be pipelined as this is a forward path [21]. Secondly, a cascade of first-order modulators is inherently stable. A conventional first-order EFB modulator with the integrator critical path is shown in Fig. 5 wherein the q LSBs of the input signal, x enter the integrator. The carry generated from the integrator is then added to the remaining p MSBs of x. The integrator bit-width is determined by the number of DAC bits required. Fig. 6 shows the first-order loop-unrolled two-channel TI EFB DSM operating at half the speed but the critical path is now a two adder delay (Adders A and B). The two adders, A and B can be optimized to achieve a very high speed, nevertheless, they ultimately limit the modulator speed [20]. An effective 10 GHz speed cannot be met with this two-channel architecture in a standard $1\,\mathrm{V}$ $65\,\mathrm{nm}$ CMOS technology if purely static CMOS logic with its robust noise margins and $>$1-bit per pipeline stage is to be used.

The main reason for the speed limitation of this first order EFB TIDSM is the fact that adder B has to wait for the computation from adder A i.e the two adders (or channels) are coupled (shown in Fig. 7(a)). If the two channels/adders could be decoupled, then the two additions can happen in parallel within the integrator, thus speeding it up (Fig. 7(b)). To achieve this decoupling, a pre-computation that corresponds to the intermediate computed value of Fig. 7(a) is performed prior to the loop. If this pre-computation (or look-ahead) turns out to be incorrect, then a post-decode block corrects this after the integrator. In summary, this involves moving a part of the computation out from the integrator feedback loop to

before (look-ahead) and after the integrator (post-decode).

In order to arrive at the proposed LA solution, the first-order EFB two-channel TIDSM of Fig. 6 must be considered again. The DSM has an input width of $l = p+q$ bits, of which the q LSBs enter the feedback path i.e. the integrator. The two carry signals (C_0,C_1) generated from the integrator are then added to the p MSBs of the two channels respectively to obtain the noise-shaped output. Let $x_{0,LSB}$ and $x_{1,LSB}$ be the lower q bits of the two-channel entering the integrator. Then, the following equations can be written for the k^{th} sample of the two generated sum (S_0, S_1) and carry (C_0, C_1) signals.

$$S_0(k) = [S_1(k-1) + x_{0,LSB}(k)] \bmod 2^q \tag{2}$$

$$S_1(k) = [S_0(k) + x_{1,LSB}(k)] \bmod 2^q \tag{3}$$

$$C_0(k) = \left\lfloor \frac{S_1(k-1) + x_{0,LSB}(k)}{2^q} \right\rfloor \tag{4}$$

$$C_1(k) = \left\lfloor \frac{S_0(k) + x_{1,LSB}(k)}{2^q} \right\rfloor \tag{5}$$

where $\lfloor\ \rfloor$ denotes a floor operation and can take the value of 0 or 1 in this case. Using (2) in (3), we get

$$S_1(k) = [[(S_1(k-1) + x_{0,LSB}(k)] \bmod 2^q + x_{1,LSB}(k)] \bmod 2^q \tag{6}$$

Equation (6) represents the two coupled adders. This equation is commutative in nature if any carry generated is ignored and can be rewritten as

$$S_1(k) = [(x_{0,LSB}(k) + x_{1,LSB}(k)) \bmod 2^q + S_1(k-1)] \bmod 2^q \tag{7}$$

Equation (7) shows that the first addition part of the equation, i.e. $x_{0,LSB}(k) + x_{1,LSB}(k)$ can be pre-computed in advance (look-ahead) before entering the feedback loop since the two inputs are readily available i.e. S_1 can be computed independent of S_0. Rewriting (7) as,

$$S_1(k) = [x_{L,LSB}(k) + S_1(k-1)] \bmod 2^q \tag{8}$$

where $x_{L,LSB}(k) = [(x_{0,LSB}(k) + x_{1,LSB}(k)) \bmod 2^q]$ and represents only the sum part from this addition i.e. lower q bits (and not the carry generated from the addition). From (2) and (8), it can be seen that the computation of S_0 and S_1 is possible in parallel, thus making it possible to decouple the two adders, A and B. The parallel computation of S_0 and S_1 results in the improvement of the operating speed by reducing the critical path to that of only one adder as compared to (6). Fig. 8 demonstrates the proposed LA-TIDSM that implements (2) and (8) in parallel by moving the pre-computation of the intermediate partial sum, $x_{L,LSB}$ to before the loop.

However, this modified order of executing the additions compared to the loop-unrolled TIDSM (Fig. 6) for computing S_1 results in an incorrect carry being generated from the loop for the second channel (CH1) in some cases. If the carry generated from $S_1(k-1) + x_{L,LSB}$ (Eq. (8)) in the LA-TIDSM is called CL_1, then $CL_1 \neq C_1$, where C_1 (Eq. (5)) is the correct expected carry for CH1 of Fig. 6. Note that carry of CH0 is not affected by this change in order of the additions, i.e. $CL_0 = C_0$. Hence, for the modulators of Fig. 6 and Fig. 8 to be functionally equivalent, the expected carry C_1 must be correctly decoded before passing it on to the final addition with the p MSB bits.

In order to decode the correct value of C_1, the carry CF_0 generated by the pre-addition of $x_{0,LSB}$ and $x_{1,LSB}$ is also propagated forward (Fig. 8). The information to calculate C_1 is found to be embedded within CF_0, CL_0 and CL_1. The truth table for predicting C_1 from CF_0, CL_0 and CL_1 is shown in Table II. Simplifying the truth table results in the following expression,

$$C_1 = CF_0CL_1 + \overline{CL_0}(CF_0 + CL_1) \tag{9}$$

A numerical example explaining the LA-TIDSM is also presented in Appendix A. The proof for arriving at this truth table for C_1 that results in the functional equivalency between the

TIDSM and the proposed LA-TIDSM is provided in Appendix B.

The delay of the pre-computation in (8) is one adder delay similar to that of the integrator while the delay required to implement the post-decoding of C_1 in (9) is less than one adder delay. This technique can be extended to any number of channels. While the critical path of a conventional M-channel TIDSM is M adders, for an LA-TIDSM it always remains one adder delay, independent of the number of channels. In a M-channel LA-TIDSM, M-1 look-ahead additions are performed prior to the integrator i.e. $x_{0,LSB} + x_{1,LSB} + x_{2,LSB} ... + x_{M-2,LSB} + x_{M-1,LSB}$ and M-1 carry signals resulting from each addition are propagated forward. The expression for the correct carry C_i of the i^{th} channel $\forall\ i \neq 0$ can be generalized for an M-channel LA-TIDSM as

$$C_i = CF_{i-1}CL_i + \overline{CL_{i-1}}(CF_{i-1} + CL_i) \tag{10}$$

where $1 \leq i \leq M-1$. It can be recollected that C_0 is always correctly generated and requires no post-correction.

Alternative implementations of the LA-TIDSM are also possible. Referring to (6) where $C_1(k) = \lfloor (S_0(k) + x_{1,LSB}(k))/2^q \rfloor$, there exists another way of computing C_1 instead of the post-decode block. It is observed that C_1 is not required within the loop and hence can be calculated by replicating the operation $(S_0 + x_{1,LSB})$ outside the loop. However, this technique is inefficient as it requires an extra adder and does not help to improve the critical path within the loop.

The TIDSM structure of Fig. 2 and its enhancement, the LA-TIDSM in Fig 8 is obtained by a TI/poly-phase decomposition of the delay element, z^{-1} in the integrator transfer function, $H(z) = z^{-1}/(1-z^{-1})$. An alternative TI implementation of the MASH architecture has been recently proposed in [23] by using a poly-phase decomposition of the full integrator transfer function, $H(z)$ instead. This implementation also has a one adder critical path within the

loop, but results in an inefficient carry generation logic for C_0 and C_1. For a two-channel implementation of a first order modulator, the LA-TIDSM uses only 3 adders while [23] requires 8 adders. As the number of channels increases, the hardware savings are larger e.g. for 3-channels, the LA-TIDSM uses only 5 adders while [23] requires 21 adders.

IV. High-Speed LA-TIDSM DAC Design

A. Modulator Design

An 8-bit input two-channel LA-TIDSM with 4-bit output is implemented in a MASH 1-1 configuration consisting of a cascade of two first-order EFB DSMs. Each of the two EFB DSMs is pipelined into 2-bit sections as shown in Fig. 9. Only purely static CMOS custom designed logic is used. The FFs used are conventional Static Transmission Gate Flip-flops (TGFF) while the 2-bit additions are carried out using 1-b carry-select full adders (FA). A NOR gate for synchronously resetting the integrator is also used at the end of the addition. Since the NOR gate is inverting, Adder 2 generates $\overline{\text{sum}}$ and $\overline{\text{carry}}$. On the other hand, Adder 1 generates $\overline{\text{sum}}$ and carry. However, this requirement of different output polarities from the two adders has no impact on the total delay.

Table III shows the post-layout simulated delay contributions from the various components in the critical path formed by the feedback. The simulations are carried out at $1\,\text{V}$, 75° C for a typical corner and 110° C for a slow corner in a standard $65\,\text{nm}$ CMOS process using general purpose (GP) transistors and maximum RC extracted layout. Adder 1 is inherently slower than Adder 2 because it produces the complementary inputs/outputs and has a two gate delay. Adder 2 on the other hand, receives complementary carry inputs, doesn't need to produce complementary outputs and has only a one gate delay. The output FF for S_1 is replicated so that one copy of the output goes to the next MASH stage while one copy goes back into the feedback loop. It is seen that the total delay of $181\,\text{ps}$ at the typical corner

implies a maximum half-clock frequency of 5.52 GHz and an effective rate of 11.05 GS/s. Comparing this to the 2-bit TIDSM pipeline of [20], this represents a 37 ps improvement in the delay or a 17% speed up in the critical path.

B. Final Multiplexer and DAC Current Cell Design

Fig. 10 shows the 2:1 final full-rate multiplexing (MUX) scheme and the switch driver. The 4-bit output of the LA-TIDSM is converted to a 15-bit thermometer code prior to the final multiplexing. The CH1 thermometer encoding is moved to the clock falling edge through a half-cycle path shifting of the CH1 output from the LA-TIDSM. There is a half-cycle path at the input of the MUX which has a 70 ps delay and hence easily meets the timing. Since the switch driver is required to generate complementary outputs, this pseudo-differential multiplexing with the cross-coupled inverters, I_1 and I_2 helps to nominally equalize the delays of the complementary outputs. The switch driver is made high-crossing through the use of two cross-coupled NMOS, M_{n1} and M_{n2} [26]. The cross-over point is set at 0.7 V as setting it any higher yields no further improvement in the dynamic performance of the whole DAC. The switch driver is designed for 15 ps rise and fall times when connected to the current-steering DAC. The MUX utilizes two 1 V power supplies, one for the clock distribution and one for the switch driver. Each of these rails use an on-chip decoupling of 100 pF.

Fig. 11 shows the DAC current cell used. The current source M_1 utilizes a low-V_t low-power (LP) NMOS and is designed for 0.6% current mismatch σ [27] with an overdrive voltage of 360 mV. The matching is over-designed compared to the requirement of 1.1% from Section II because the DAC also supports a modulator bypass mode that allows the DAC to be driven directly from the memory by a 4-bit data of any other NTF for testing purposes. The switches M_2 and M_3 use the fast low-V_t GP devices and operate in the linear region. The cascodes, M_4 and M_5 on top of the switches are sized for an output impedance

that gives a greater than 50 dB SFDR performance. The cascodes also use 1.2 V low-V_t LP NMOS which grants some additional headroom compared to the 1 V GP devices. Cascoding on top of the switches is used to avoid the coupling of the switch driver signals with the DAC output. For measurement purposes, the DAC has a differential $100\,\Omega$ on-chip source termination and is interfaced to a spectrum analyzer with an off-chip 1.1 GHz bandwidth 2:1 center-tapped transformer. This setup ensures proper impedance matching for the DAC.

Deep n-well structures have been extensively used in order to reduce the substrate noise coupling from the digital blocks. The MUX and the switch driver NMOS devices are also placed in small distributed deep n-wells while the 4-bit DAC consisting of only NMOS is placed in a separate large deep n-well. The 15 current cells are laid out in a one single column with the odd and even numbered cells placed on either side of the center respectively to mitigate the gradient errors. The clock distribution to the 15 MUX switch driver cells is carefully matched with an H-tree and the NMOS of the distribution buffers are also placed in small distributed deep n-wells.

V. Chip Implementation and Testing Methodology

A prototype IC is fabricated in a standard 65 nm CMOS technology and mounted on a JLCC-68 package. It integrates a 8-bit two-channel LA-TIDSM with a 4-bit DAC and a 1-Kbit memory to enable full speed testing of the DAC. Fig. 12 shows the chip photograph while Fig. 13 shows the overall testing methodology. The memory is designed using static TGFFs and laid out in a 32b$\times$32b aspect ratio with each location being 8-bit wide. The memory is written into serially at a low speed and then read at full speed internally during the DAC operation. This is achieved by first fetching four memory locations incrementally using a lower frequency $f_s/4$ clock. This 32-bit data is split into two 16-bit streams representing odd and even data. These two streams are then multiplexed using the $f_s/2$ clock to obtain two

8-bit data that are fed to the LA-TIDSM. The memory allows a 128-point deep signal to be tested and hence the minimum frequency bin spacing in the input signal is $f_s/128$. For all the SFDR and IM3 measurements, a $\pm$0.5 LSB dithered input signal is used so that the non-linearity components are not masked while no dithering is used during SNDR measurement. The entire chip including the pads occupies an area of $1.5\,\text{mm}\times 0.9\,\text{mm}$. The high-speed $f_s/2$ clock is sent into the chip as a sinusoidal differential signal and amplified to rail-to-rail within the chip. Static CMOS pseudo-differential clock distribution is used. Fig. 14 shows the overall clock distribution strategy for the IC using the pseudo-differential clock inverter (CI) as a building block. The short clock path to the MUX comprising only 7 inverter stages with a H-tree (mentioned earlier in Section IV-B) is also shown in the same figure. The duty cycle is set by the cross-coupled inverters in the clock distribution and hence no external duty cycle calibration of the input clock is performed.

VI. Measurement Results

The LA-TIDSM DAC achieves an effective sample rate of $11\,\text{GS/s}$. Since the $3\,\text{dB}$ bandwidth of the transformer is $1.1\,\text{GHz}$, all the measurements are restricted to this bandwidth. Fig. 15 shows the measured wideband spectrum and the noise shaping at $11\,\text{GS/s}$ with a $1.1\,\text{GHz}$ input tone. Fig. 16 shows that the measured SNDR is $39\,\text{dB}$ in a $1.1\,\text{GHz}$ bandwidth. Fig. 17 shows a measured IM3 of $-49\,\text{dBc}$ with two $-6\,\text{dBFS}$ tones located at $945\,\text{MHz}$ and $1117\,\text{MHz}$ respectively. Due to the limited depth of the testing memory, the closest distance between two coherently sampled sinusoidal tones possible is $170\,\text{MHz}$. To measure the harmonic distortion, a $428\,\text{MHz}$ tone is the highest frequency whose HD2 and HD3 lie close to the $0-1.1\,\text{GHz}$ band. The measured HD2/HD3 is $56\,\text{dB}/53\,\text{dB}$ respectively and shown in Fig. 18.

Fig. 19 shows a sweep of the input frequency versus the measured SFDR (0$-$1.1 GHz

band), SNDR ($0-$input frequency) and IM3 (center frequency) at 11 GS/s. The figure shows that a greater than 53 dB SFDR and smaller than -49 dBc IM3 performance is achieved in the $0-1.1$ GHz band. The measured SNDR is 42 dB (ENOB 6.8 bits) for the WiGig 880 MHz BW and 39 dB (ENOB 6.2 bits) in a 1.1 GHz BW. The total measured power consumption is 117 mW from 1 V digital (90 mW) and 1.2 V (27 mW) analog supplies. The power and area breakdown of the $\Delta\Sigma$ DAC is shown in Table IV.

In order to evaluate only the final MUX and estimate the DCE in the $\Delta\Sigma$ DAC, the 4-b DAC is configured as a wideband Nyquist DAC that is directly driven from the memory by using the modulator bypass path in the chip. A 4-b unshaped single tone signal at 2.83 GHz (f_{in}) is used. This results in a measured interleaving spur of -36.9 dBc at 2.67 GHz ($f_s/2 - f_{in}$) as shown in Fig. 20. The timing error, Δt is then calculated using ([18])

$$\text{SFDR} = 20\log_{10}\left(\frac{1}{\pi f_{in}\Delta t}\right) \tag{11}$$

This yields $\Delta t = 1.6$ ps or an estimated DCE of 0.88%. Using (1), the DCE is found to contribute to a 1.2 dB relative SNDR loss for the IEEE 802.11ad 880 MHz BW and a 0.6 dB loss for the 1.1 GHz BW.

In order to measure the IEEE 802.11ad spectral mask, single-carrier 16-QAM encoded random data with a frequency bin spacing of ~ 80 MHz between 0 to 880 MHz is first generated and pulse-shaped in Matlab with an 18^{th}-order RRC filter having a 0.25 roll-off factor. This data is loaded into the memory for the mask measurement. The filtering is achieved from a combination of the 1.1 GHz interfacing transformer, bonding wire inductance, JLCC socket capacitance and the PCB track. It is seen that this overall combination provides a 1.5^{th}-order low-pass response between $0.95-1.9$ GHz and a 2.3^{rd}-order low-pass filter response between $1.9-3$ GHz. Fig. 21 shows the measured spectral mask under these conditions at 10.56 GS/s operation. It can be observed that the mask of the IEEE 802.11ad (WiGig) standard is met

and the out-of-band quantization noise from the second-order $\Delta\Sigma$ modulator is found not to be a limiting factor.

Table V shows the comparison of this LA-TIDSM DAC with previously reported $\Delta\Sigma$ DACs having a sample rate >2.5 GHz. It is seen that this work represents an improvement of over five times in the measured bandwidth and is the first $\Delta\Sigma$ DAC to achieve a sample rate greater than 10 GS/s and BW greater than 1 GHz. High-speed DSMs have also been used in hybrid DACs (a combination of Nyquist and $\Delta\Sigma$ DACs) [12], [23] and frequency synthesizers [21]. Table VI shows a comparison with these previously reported high-speed digital $\Delta\Sigma$ modulators having greater than 5 GHz speed. The table shows that the high speed $\Delta\Sigma$ modulator space is dominated by the MASH architecture and this LA-TI DSM achieves the highest speed.

Since the aim of this LA-TIDSM DAC is to provide a third alternative to the traditional Nyquist DAC based architecture (Fig.1(a)) and the oversampled high-speed Nyquist DAC architecture (Fig. 1(b)), it is of interest to compare the performance of this DAC with other previously reported DACs with these characteristics and a similar resolution. Table VI shows this comparison. For high-speed DACs reported in [18] and [28], performance in the $0-1.1$ GHz bandwidth has been extracted so a comparison with similar bandwidths can be made. It can be seen that the overall SFDR in this work shows a similar performance as these Nyquist DACs. The overall figure-of-merit (FOM) [29] is found to be comparable to the other Nyquist DACs. Since 75% of the power in $\Delta\Sigma$ DAC comes from the digital part, this DAC can benefit from further CMOS scaling which can further improve its FOM. An area comparison of this $\Delta\Sigma$ DAC with [4] and [30] is easier because these DACs are also designed in 65 nm CMOS. The $\Delta\Sigma$ DAC in this work has 1.6 times more area than the Nyquist DAC presented in [4]. In [30], although a very compact DAC is presented, a high performance analog transistor with 1.5 times better matching parameter, A_{vt} is used. If normal

low-Vt low-power transistors are used, then the $\Delta\Sigma$ DAC would have 2 times larger area than the Nyquist DAC of [30]. This indicates that the two-channel TI-$\Delta\Sigma$ DAC has a larger area consumption as compared to Nyquist DACs due to the increased digital processing. If the area is a constraint, then a TIDSM with larger number of channels can help to reduce the area [21].

The DAC clock spurs can be a concern in transceivers utilizing frequency-division duplexing (FDD) where transmit and receive operations occur simultaneously in bands that are close to each other, such as LTE or W-CDMA standards. The DAC clock can leak through the antenna duplexer into the receiver band degrading its performance [31]. IEEE 802.11ad compliant 60-GHz radio transceivers, on the other hand, use time-division duplexing (TDD) where transmit and receive operations are in the same band with separate antennas and no duplexer [4], [5]. Thus, the receiver performance is less affected by the DAC clock spurs.

VII. Conclusion

This work has presented an $11\,$GS/s $1.1\,$GHz bandwidth time-interleaved MASH 1-1 $\Delta\Sigma$ DAC in $65\,$nm CMOS that is suitable for the $60\,$GHz radio baseband. Consisting of only fifteen analog current cells (4-bit DAC), the highly digital $\Delta\Sigma$ DAC achieves a dynamic performance of $53\,$dB SFDR, $-49\,$dBc IM3 and $39\,$dB SNDR in a $1.1\,$GHz bandwidth consuming $117\,$mW of power. The high sample rate and bandwidth is enabled by a two-channel architecture allowing a single half-rate-clock for the logic and the multiplexing. This requires the logic to operate at half of the sampling rate, which is achieved through a look-ahead technique that reduces the critical path of the modulator to one adder only. The $\Delta\Sigma$ DAC has the potential for use in digital architectures for wideband transmitters.

APPENDIX

A. Numerical Example of the LA-TIDSM

An example of the look-ahead approach is presented here using decimal numbers in order to explain the post-decode block. Assume that the integrator can hold values between 0 and 9. Let the value stored in the integrator, $S_1(k-1) = 3$. Let the two channel inputs $x_{0,LSB}(k)$ and $x_{1,LSB}(k)$ be 6 and 8 respectively. Then, using (2)−(5), the following result is obtained for the conventional TIDSM of Fig. 6: $S_0(k) = 9$, $C_0(k) = 0$, $S_1(k) = 7$ and $C_1(k) = 1$.

Now considering the LA-TIDSM of Fig. 8, we get $x_{L,LSB}(k) = 4$ and $CF_0(k) = 1$. Moving into the integrator, the following result is obtained: $S_0(k) = 9$, $CL_0(k) = 0$, $S_1(k) = 7$ and $CL_1(k) = 0$. It is seen that the value of $S_0(k)$ and $S_1(k)$ are correctly calculated. Also, $CL_0 = C_0$ while $C_1 \neq CL_1$. Hence, the correct value of C_1 has to be predicted looking at CF_0, CL_0 and CL_1 i.e. the truth table in Table II. For $CF_0 = 1$, $CL_0 = 0$ and $CL_1 = 0$, we get $C_1 = 1$ from the table which is the correct expected value in a conventional TIDSM.

B. Proof of Equivalency between TIDSM and LA-TIDSM

The critical part of LA-TIDSM is arriving at the truth table for correctly decoding C_1 (Table II) that results in a functional equivalency with the TIDSM. In this section, only the q LSB's of x_0 and x_1 are used and hence the LSB suffix for these variables is dropped. Consider the sequencing of operations in a TIDSM (Fig. 6). Let the integrator output in the previous clock $S_1(k-1)$ be called S_1 for the remainder of this section. Then, the value of the carry C_1 is calculated in the TIDSM by combining (2), (3) and (5) and re-writing them as

$$C_1 = 1 \text{ if } F > 2^q - 1 \text{ else } C_1 = 0. \tag{12}$$

$$\text{where } F = [(S_1 + x_0) \bmod 2^q] + x_1 \tag{13}$$

Now, looking at the LA-TIDSM in Fig. 8, C_1 needs to be correctly predicted from CF_0, CL_0 and CL_1 i.e. F must be estimated for the eight different cases. The following two identities are used in the proof for any two q-bit unsigned numbers, a and b.

$$a+b \leq 2^q-1 \implies (a+b) \bmod 2^q \leq 2^q-1 \ \& \ a+b = (a+b) \bmod 2^q \tag{14}$$

$$a+b > 2^q-1 \implies a+b = [(a+b) \bmod 2^q] + 2^q \tag{15}$$

Only two of the eight cases from Table II are proved here but a similar procedure is extended for other cases as well.

Case 4 ($\text{CF}_0 = 1$, $\text{CL}_0 = 0$, $\text{CL}_1 = 0$):

$$CF_0 = 1 \implies x_0 + x_1 > 2^q - 1 \tag{16}$$

$$CL_0 = 0 \implies S_1 + x_0 \leq 2^q - 1 \tag{17}$$

$$CL_1 = 0 \implies S_1 + [(x_0 + x_1) \bmod 2^q] \leq 2^q - 1 \tag{18}$$

From (16), if $x_0 + x_1 > 2^q - 1$, then $S_1 + x_0 + x_1 > 2^q - 1$. Now using (17), we have

$$[(S_1 + x_0) \bmod 2^q] + x_1 > 2^q - 1$$

$$\implies F > 2^q - 1 \implies C_1 = 1 \tag{19}$$

Case 5 ($\text{CF}_0 = 1$, $\text{CL}_0 = 0$, $\text{CL}_1 = 1$):

$$CF_0 = 1 \implies x_0 + x_1 > 2^q - 1 \tag{20}$$

$$CL_1 = 0 \implies S_1 + x_0 \leq 2^q - 1 \tag{21}$$

$$CL_1 = 1 \implies S_1 + [(x_0 + x_1) \bmod 2^q] > 2^q - 1 \tag{22}$$

Using (20) in (22), we have

$$S_1 + x_0 + x_1 - 2^q > 2^q - 1$$

$$\implies S_1 + x_0 + x_1 > 2^{(q+1)} - 1 \tag{23}$$

Now, using (21) in (23), we get $x_1 > 2^q$, which cannot be true. Hence, this condition cannot occur implying $C_1 = X$.

Extending this proof similarly to the remainder of the six cases results in the truth table of Table II.

ACKNOWLEDGEMENT

This work was supported by the Swedish Foundation for Strategic Research (SSF), Swedish Research Council (VR) and Swedish Innovation Agency (VINNOVA).

REFERENCES

[1] "IEEE 802.11ad - Amendment 3: Enhancements for Very High Throughput in the 60 Ghz Band," *Standard*, March 2012. [Online]. Available: http://ieeexplore.ieee.org/servlet/opac?punumber=6171797

[2] "High rate 60 GHz PHY, MAC and PALs : ECMA-387," *Standard*, Dec 2010. [Online]. Available: http://www.ecma-international.org/

[3] "WirelessHD Specification v1.1 overview," *Standard*, May 2010. [Online]. Available: http://www.wirelesshd.org/

[4] N. Saito, T. Tsukizawa, N. Shirakata, T. Morita, K. Tanaka, J. Sato, Y. Morishita, M. Kanemaru, R. Kitamura, T. Shima, T. Nakatani, K. Miyanaga, T. Urushihara, H. Yoshikawa, T. Sakamoto, H. Motozuka, Y. Shirakawa, N. Yosoku, A. Yamamoto, R. Shiozaki, and K. Takinami, "A fully integrated 60-GHz CMOS transceiver chipset based on WiGig/IEEE 802.11ad with built-in self calibration for mobile usage," *IEEE J. Solid-State Circuits*, vol. 48, no. 12, pp. 3146–3159, Dec. 2013.

[5] K. Okada, K. Kondou, M. Miyahara, M. Shinagawa, H. Asada, R. Minami, T. Yamaguchi, A. Musa, Y. Tsukui, Y. Asakura, S. Tamonoki, H. Yamagishi, Y. Hino, T. Sato, H. Sakaguchi, N. Shimasaki, T. Ito, Y. Takeuchi, N. Li, Q. Bu, R. Murakami, K. Bunsen, K. Matsushita, M. Noda, and A. Matsuzawa, "A full 4-channel 6.3Gb/s 60GHz direct-conversion transceiver with low-power analog and digital baseband circuitry," in *IEEE ISSCC Dig. Tech. Papers*, Feb 2012, pp. 218–220.

[6] M. Miyahara, H. Sakaguchi, N. Shimasaki, and A. Matsuzawa, "An 84 mW 0.36 mm^2 analog baseband circuits for 60 GHz wireless transceiver in 40 nm CMOS," in *Proc. IEEE Radio Frequency Integrated Circuits Symposium (RFIC)*, June 2012, pp. 495–498.

[7] M. Tokumaru, H. Ikoma, Y. Yamada, K. Okamoto, A. Yamamoto, and Y. Shirakawa, "A 14.6th-order 3.456GHz transmit baseband filter in 110nm CMOS for millimeter-wave communication systems," in *Proc. IEEE Custom Integrated Circuits Conference*, Sept. 2009, pp. 175 –178.

[8] J. Muller, B. Stefanelli, A. Frappe, L. Ye, A. Cathelin, A. Niknejad, and A. Kaiser, "A 7-bit 18^{th} order 9.6 GS/s FIR up-sampling filter for high data rate 60-GHz wireless transmitters," *IEEE J. Solid-State Circuits*, vol. 47, no. 7, pp. 1743 –1756, July 2012.

[9] F. Houfaf, M. Egot, A. Kaiser, A. Cathelin, and B. Nauta, "A 65nm CMOS 1-to-10GHz tunable continuous-time low-pass filter for high-data-rate communications," in *IEEE ISSCC Dig. Tech. Papers*, Feb 2012, pp. 362–364.

[10] P. Wambacq, V. Giannini, K. Scheir, W. Van Thillo, and Y. Rolain, "A fifth-order 880MHz/1.76GHz active lowpass filter for 60GHz communications in 40nm digital CMOS," in *Proc. IEEE European Solid State Circuits Conference (ESSCIRC)*, Sept 2010, pp. 350–353.

[11] A. Jerng and C. Sodini, "A wideband $\Delta\Sigma$ digital-RF modulator for high data rate transmitters," *IEEE J. Solid-State Circuits*, vol. 42, no. 8, pp. 1710–1722, Aug 2007.

[12] A. Pozsgay, T. Zounes, R. Hossain, M. Boulemnakher, V. Knopik, and S. Grange, "A fully digital 65nm CMOS transmitter for the 2.4-to-2.7GHz WiFi/WiMAX bands using 5.4GHz $\Delta\Sigma$ RFDAC," in *IEEE ISSCC Dig. Tech. Papers*, Feb. 2008, pp. 360 –619.

[13] P. Seddighrad, A. Ravi, M. Sajadieh, H. Lakdawala, and K. Soumyanath, "A 3.6GHz, 16mW $\Delta\Sigma$ DAC for a 802.11n / 802.16e transmitter with 30db digital power control in 90nm CMOS," in *Proc. IEEE European Solid State Circuits Conference (ESSCIRC)*, Sept 2008, pp. 202–205.

[14] A. Frappe, A. Flament, B. Stefanelli, A. Kaiser, and A. Cathelin, "An all-digital RF signal generator using high-speed $\Delta\Sigma$ modulators," *IEEE J. Solid-State Circuits*, vol. 44, no. 10, pp. 2722 –2732, Oct. 2009.

[15] B. Mohr, N. Zimmermann, B. Thiel, J. Mueller, Y. Wang, Y. Zhang, F. Lemke, R. Leys, S. Schenk, U. Bruening, R. Negra, and S. Heinen, "An RFDAC based reconfigurable multistandard transmitter in 65nm CMOS," in *Proc. IEEE Radio Frequency Integrated Circuits Symposium (RFIC)*, June 2012, pp. 109–112.

[16] J. Savoj, A. Abbasfar, A. Amirkhany, M. Jeeradit, and B. Garlepp, "A 12-GS/s phase-calibrated CMOS digital-to-analog converter for backplane communications," *IEEE J. Solid-State Circuits*, vol. 43, no. 5, pp. 1207 –1216, May 2008.

[17] G. Engel, S. Kuo, and S. Rose, "A 14b 3/6GHz current-steering RF DAC in 0.18 um CMOS with 66dB ACLR at 2.9GHz," in *IEEE ISSCC Dig. Tech. Papers*, 2012, pp. 458–460.

[18] E. Olieman, A.-J. Annema, and B. Nauta, "An interleaved full nyquist high-speed DAC technique," *IEEE J. Solid-State Circuits*, vol. 50, no. 3, pp. 704–713, March 2015.

[19] R. Khoini-Poorfard, L. Lim, and D. Johns, "Time-interleaved oversampling A/D converters: theory and practice," *IEEE Trans. Circuits Syst. II: Analog and Digital Signal Processing*, vol. 44, no. 8, pp. 634–645, Aug 1997.

[20] A. Bhide, O. Najari, B. Mesgarzadeh, and A. Alvandpour, "An 8-GS/s 200-MHz bandwidth 68-mw $\Delta\Sigma$ DAC in 65-nm CMOS," *IEEE Trans. Circuits Syst. II: Express Briefs*, vol. 60, no. 7, pp. 387–391, July 2013.

[21] P. Madoglio, A. Ravi, L. Cuellar, S. Pellerano, P. Seddighrad, I. Lomeli, and Y. Palaskas, "A 2.5-GHz, 6.9-mW, 45-nm-LP CMOS $\Delta\Sigma$ modulator based on standard cell design with time-interleaving," *IEEE J. Solid-State Circuits*, vol. 45, no. 7, pp. 1410 –1420, July 2010.

[22] J. Pham and A. C. Carusone, "A time-interleaved $\Delta\Sigma$ DAC architecture clocked at the Nyquist rate," *IEEE Trans. Circuits Syst. II: Express Briefs*, vol. 55, no. 9, pp. 858–862, 2008.

[23] S. Su, T.-I. Tsai, P. Sharma, and M.-W. Chen, "A 12 bit 1 GS/s dual-rate hybrid DAC with an 8 GS/s unrolled pipeline delta-sigma modulator achieving $>$75 dB SFDR over the nyquist band," *IEEE J. Solid-State Circuits*, vol. 50, no. 4, pp. 896–907, April 2015.

[24] A. Bhide, A. Ojani, and A. Alvandpour, "Effect of clock duty cycle on two-channel interleaved $\Delta\Sigma$ DACs," *IEEE Trans. Circuits Syst. II: Express Briefs*, vol. 62, no. 7, pp. 646–650, July 2015.

[25] S. Joshi, J. Liao, Y. Fan, S. Hyvonen, M. Nagarajan, J. Rizk, H.-J. Lee, and I. Young, "A 12-Gb/s transceiver in 32-nm bulk CMOS," in *Proc. IEEE Symposium on VLSI Circuits*, June 2009, pp. 52–53.

[26] P. Palmers and M. Steyaert, "A 10-Bit 1.6-GS/s 27-mw current-steering D/A converter with 550-MHz 54-dB SFDR bandwidth in 130-nm CMOS," *IEEE Trans. Circuits and Syst I: Reg. Papers*, vol. 57, no. 11, pp. 2870 –2879, Nov. 2010.

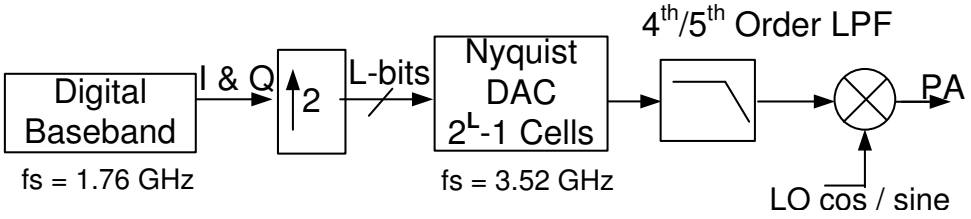
[27] M. Pelgrom, A. C. Duinmaijer, and A. Welbers, "Matching properties of MOS transistors," *IEEE J. Solid-State Circuits*, vol. 24, no. 5, pp. 1433–1439, Oct 1989.

[28] G. Radulov, P. Quinn, and A. van Roermund, "A 28-nm CMOS 7-GS/s 6-bit DAC with DFT clock and memory reaching SFDR $>$ 50 dB up to 1 GHz," *IEEE Trans. Very Large Scale Integration Systems*, vol. PP, no. 99, pp. 1–1, 2014.

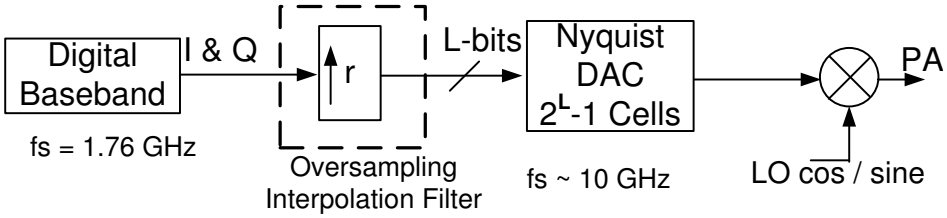
[29] D. Giotta, P. Pessl, M. Clara, W. Klatzer, and R. Gaggl, "Low-power 14-bit current steering DAC for ADSL2+/CO applications in 0.13 μm CMOS," in *Proc. IEEE European Solid State Circuits Conference (ESSCIRC)*, Sept 2004, pp. 163–166.

[30] S. Tual, P. Singh, A. Bal, and C. Garnier, "A 3GS/s 9b 1.2V single supply pure binary DAC with $>$50dB SFDR up to 1.5GHz in 65nm CMOS," in *Proc. IEEE Symposium on VLSI Circuits*, June 2011, pp. 64–65.

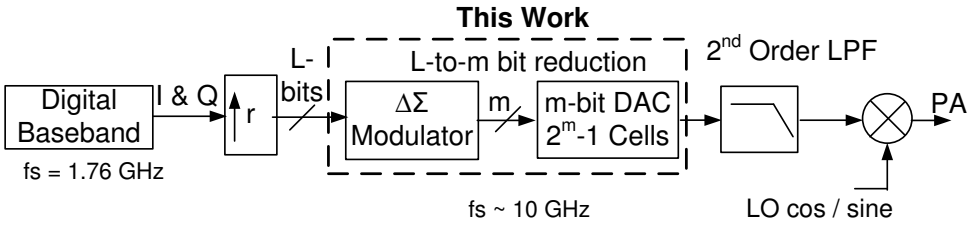
[31] S. M. Lee, S. Taleie, G. Saripalli, and D. Seo, "Clock-phase-noise-induced TX leakage estimation of a baseband wireless transmitter DAC," *IEEE Trans. Circuits Syst. II: Express Briefs*, vol. 59, no. 5, pp. 277–281, 2012.



(a) Nyquist DAC based conventional architecture used in [4], [5] and [6].



(b) Oversampling filter used in [8] that requires a high-speed Nyquist DAC.



(c) $\Delta\Sigma$ DAC based architecture proposed in this work.

Fig. 1: Comparison of different DAC based architectures for 60-GHz radio baseband.

TABLE I: Different modulator options for the 880 MHz bandwidth.

Option No.	**Mod. Order**	**Samp. Freq (GHz)/OSR**	**DAC Bits**	**Ideal SNDR(dB) @ 880 MHz**	**Loss from 1% DCE (dB)**	**Eff. SNDR (dB)**	**LP Filter. Order**
1	2	8.8/5	4	42.3	0.8	41.5	2
2	2	10.56/6	3	40.0	1.5	38.5	2
3	2	10.56/6	4	45.4	1.5	43.9	2
4	2	12.32/7	4	49.1	2.5	46.6	1
5	2	12.32/7	3	43.6	2.5	41.1	2
6	3	8.8/5	4	47.1	5.9	41.2	2
7	3	10.56/6	4	51.1	9.9	41.2	2

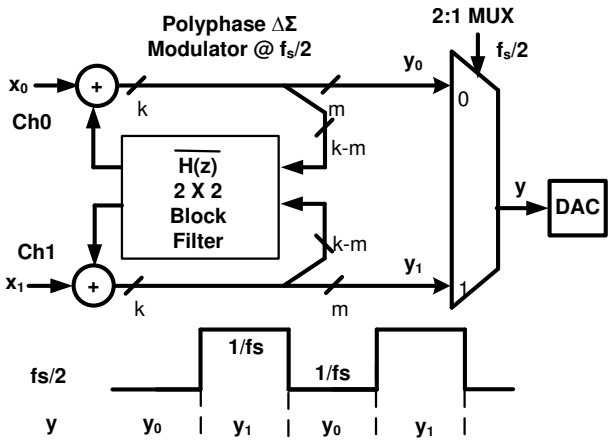


Fig. 2: A general time-interleaved $\Delta\Sigma$ modulator implementing with H(z)=1−NTF(z).

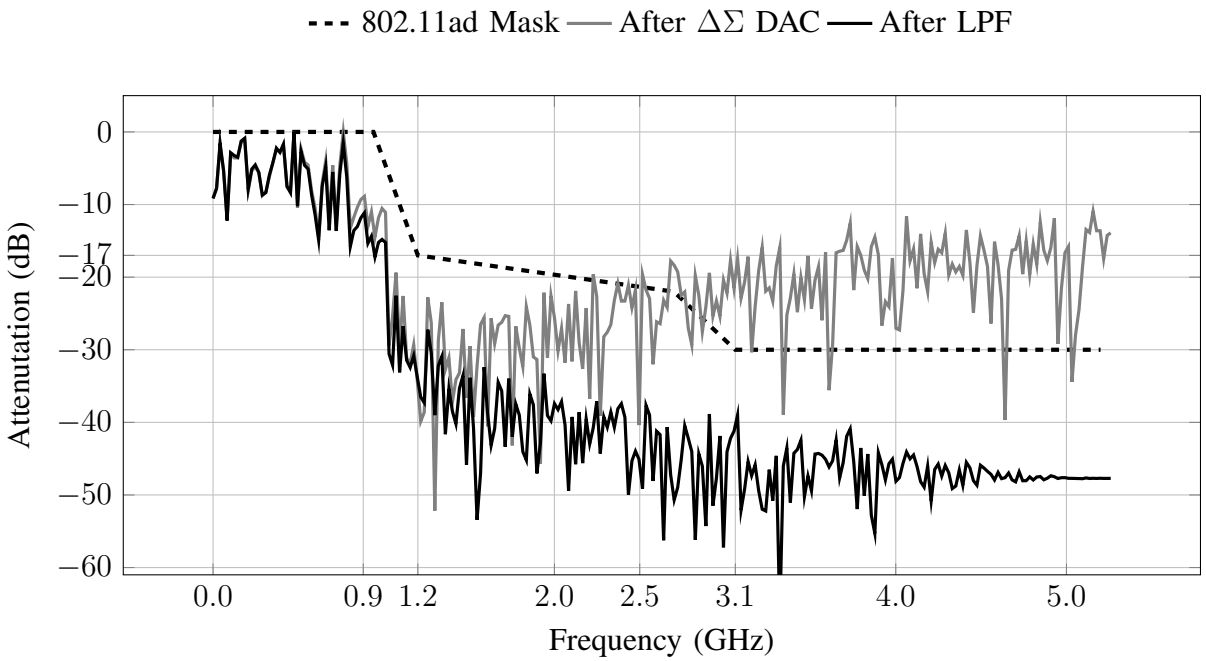


Fig. 3: Filtering with a second order LPF for a second order $\Delta\Sigma$ 4-bit DAC at 10.56 GS/s with single-carrier 16-QAM random data.

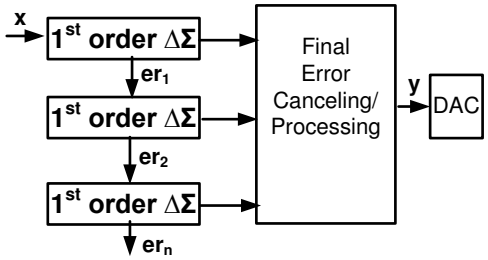


Fig. 4: An n^{th} order MASH architecture constructed from first-order EFB DSMs.

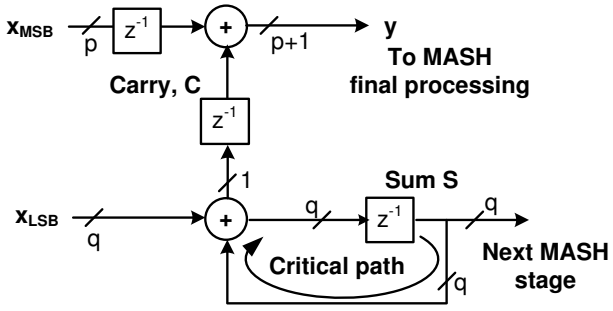


Fig. 5: A conventional first-order EFB DSM.

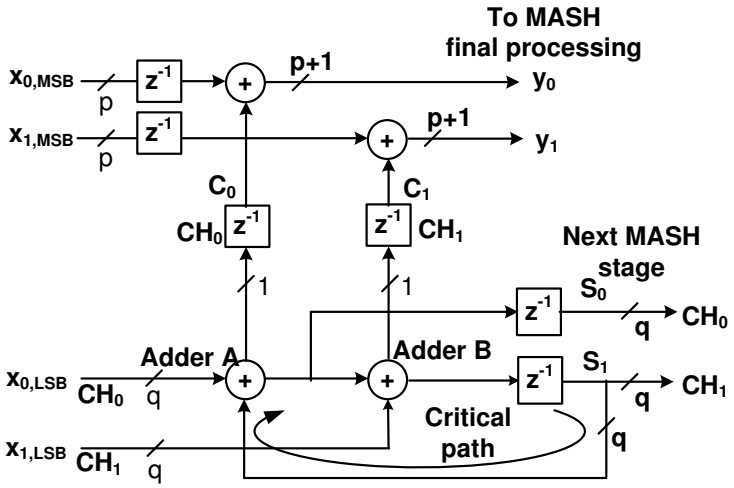
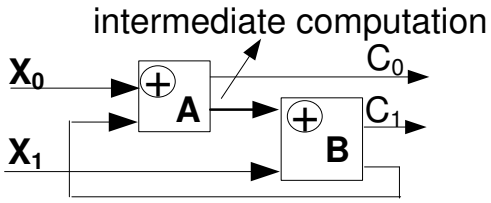
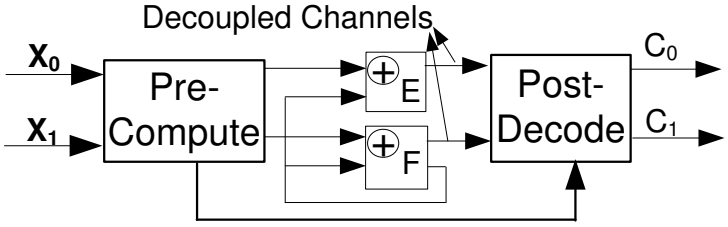


Fig. 6: A 2-channel TI EFB DSM.



(a) Speed limitation from the coupled adders.



(b) Proposed Look-ahead technique to decouple the two adders.

Fig. 7: TIDSM versus the LA-TIDSM approach to improve the speed.

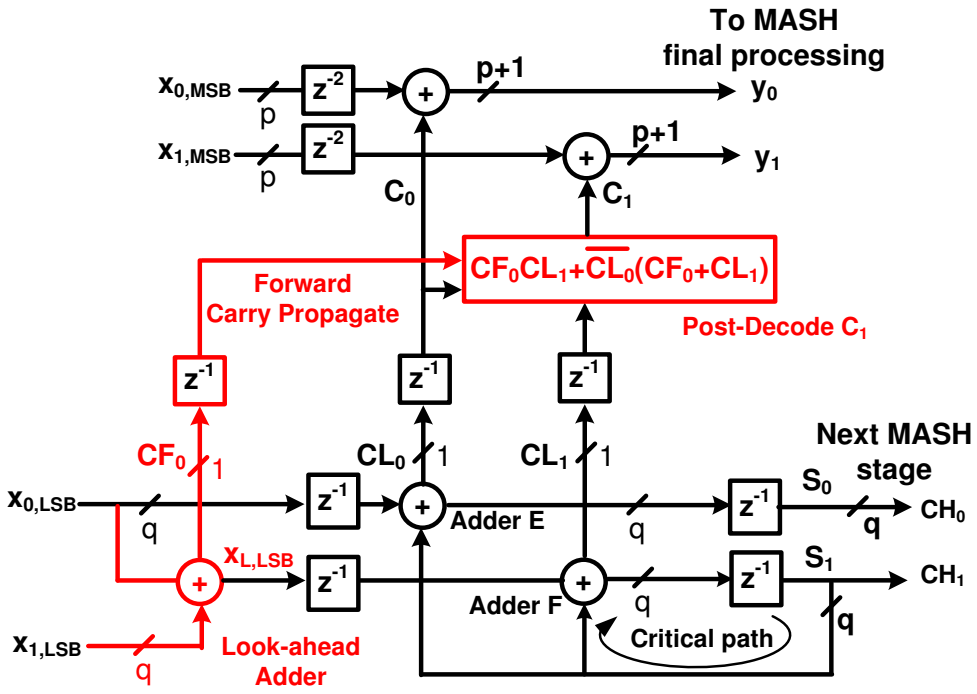


Fig. 8: Proposed two-channel LA-TIDSM EFB DSM with only one adder critical path.

TABLE II: Truth Table to compute the correct value of carry, C_1 from CF_0, CL_0 and CL_1.

Case No.	$\mathbf{CF_0}$	$\mathbf{CL_0}$	$\mathbf{CL_1}$	Expected $\mathbf{C_1}$
0	0	0	0	0
1	0	0	1	1
2	0	1	0	X
3	0	1	1	0
4	1	0	0	1
5	1	0	1	X
6	1	1	0	0
7	1	1	1	1

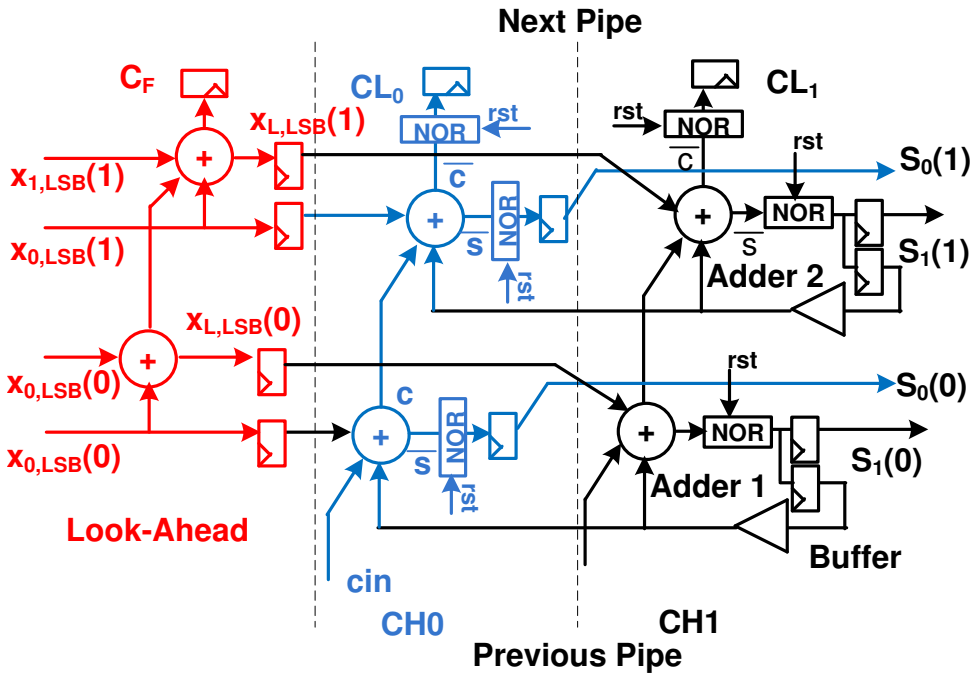


Fig. 9: A 2-bit pipeline slice of a first-order EFB LA-TIDSM. Red colour represents the LA part. Blue colour is for CH0 path and black for CH1 path.

TABLE III: Post-layout simulated delay of the 2-bit integrator pipeline (Fig. 9) at 1 V and different corners.

Block	**Load**	**Delay (ps) Typical, 75°C**	**Delay (ps) Slow, 110°C**
FF Output Delay	2 Inverters	32	37
Buffer	2 XOR, 1 NAND, 1 NOR	16	21
Adder 1 (input→cout)	2 XOR	63	75
Adder 2 (cin→cout)	1 NOR	22	28
Reset NOR gate	2 FF	25	31
FF Setup Time	–	23	26
Total Delay		181	218

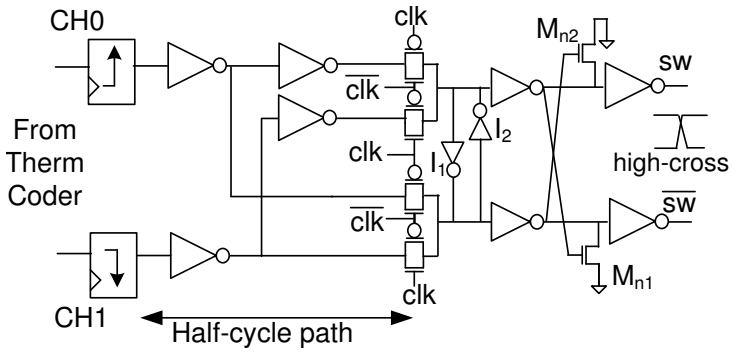


Fig. 10: Final 2:1 Multiplexer with high-crossing switch driver.

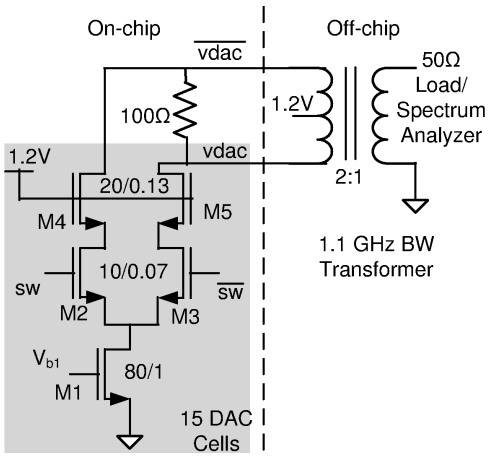


Fig. 11: DAC current cell interfaced with a center-tapped 2:1 transformer.

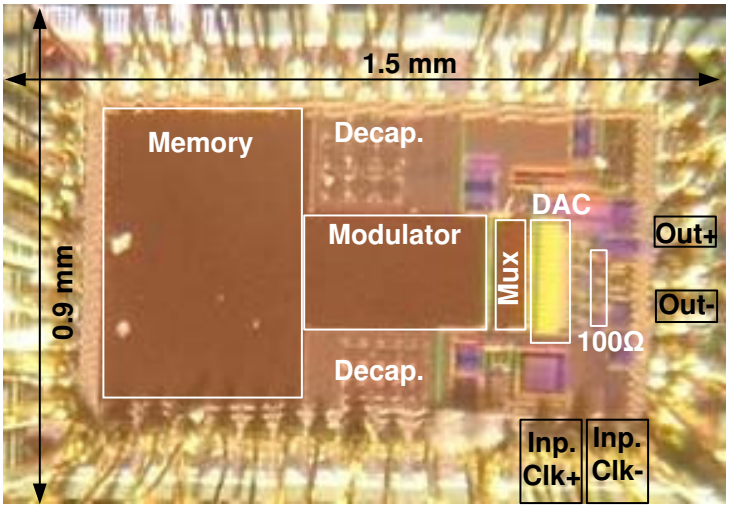


Fig. 12: Chip Photograph.

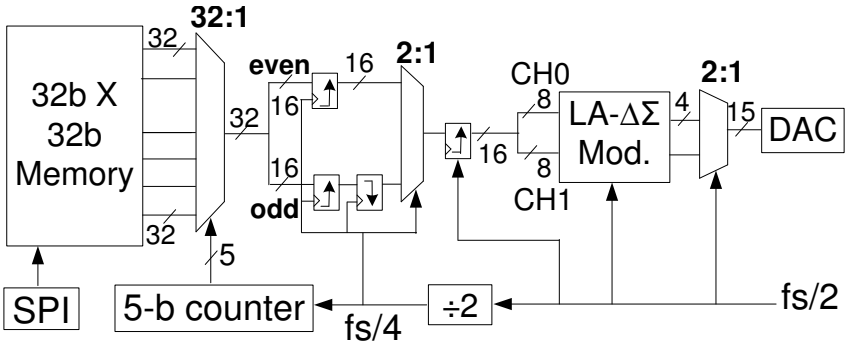


Fig. 13: Memory Architecture for full speed LA-TIDSM DAC testing.

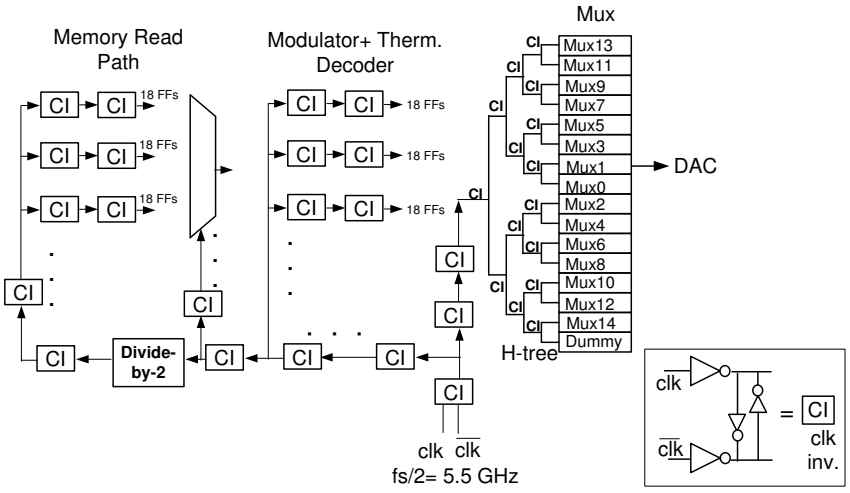


Fig. 14: Overall clock distribution strategy.

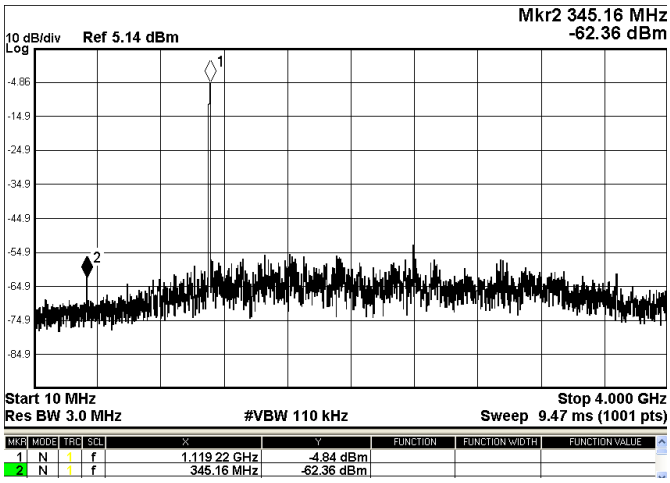


Fig. 15: Measured wideband spectrum with a 1.1 GHz input at 11 GS/s.

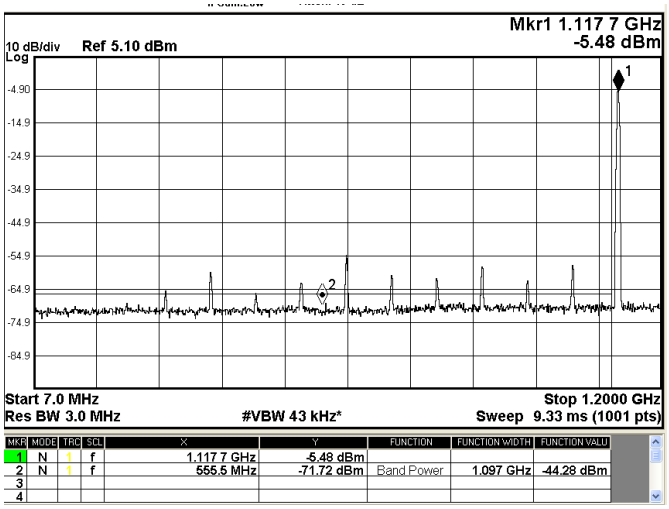


Fig. 16: Measured 39 dB SNDR with a 1.1 GHz single tone at 11 GS/s with no dithering.

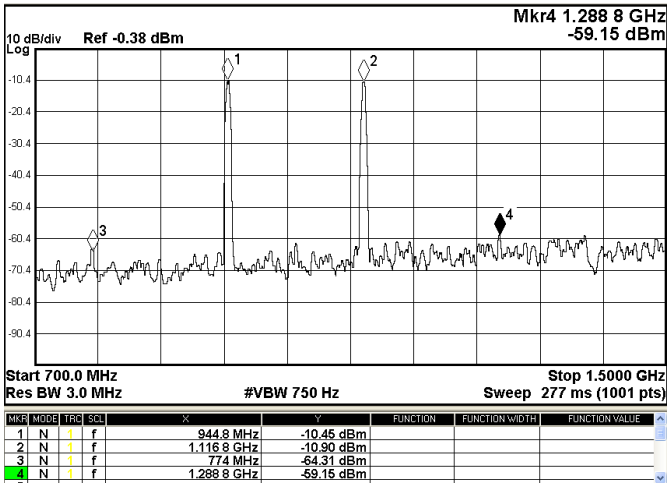


Fig. 17: Measured IM3 of −49 dBc with two tones at 945 MHz and 1.1 GHz respectively.

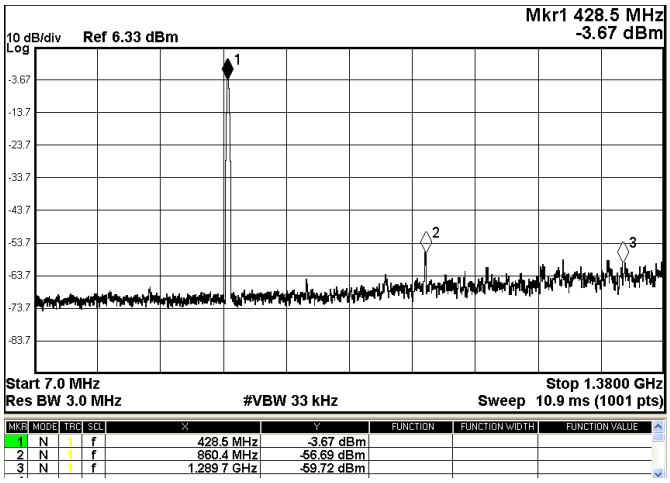


Fig. 18: Measured 53 dB HD2 and 56 dB HD3 with a 428 MHz input sine tone.

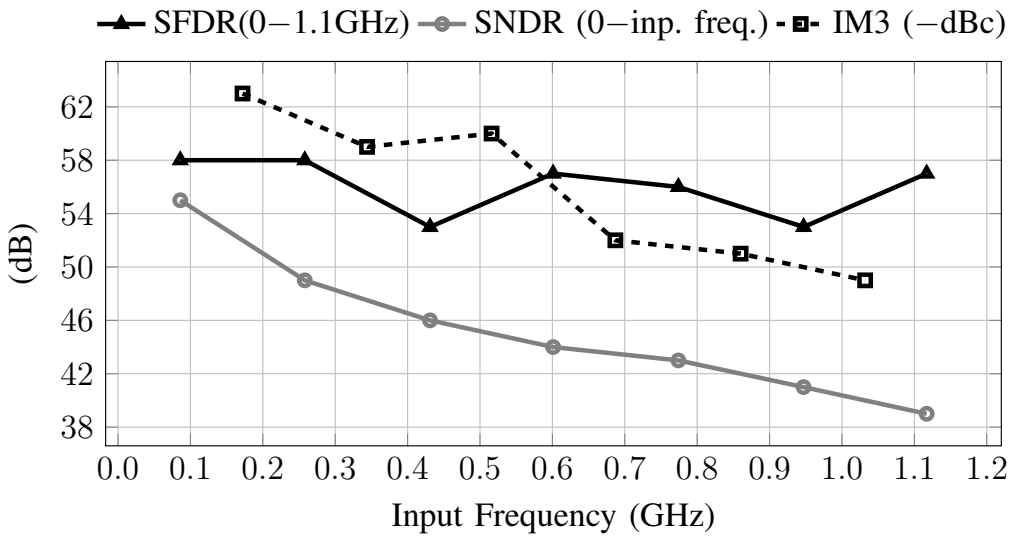


Fig. 19: Measured SFDR (in 0−1.1 GHz band), SNDR (0−inp. freq.) and IM3 (center freq.) versus frequency at 11 GS/s.

TABLE IV: Power and Area Breakdown of the DAC by function.

Power		**Area**	
Function	**Power (mW)**	**Block**	**Area**
DAC (1.2 V)	27	DAC	300×60 μm^2
MUX (1 V)	18	MUX	280×85 μm^2
$\Delta\Sigma$ Logic (1 V)	30	$\Delta\Sigma$ Mod.	260×375 μm^2
$\Delta\Sigma$ Clock Distr. (1 V)	42	-	-
Total	**117**	**Total**	**0.14 mm^2**

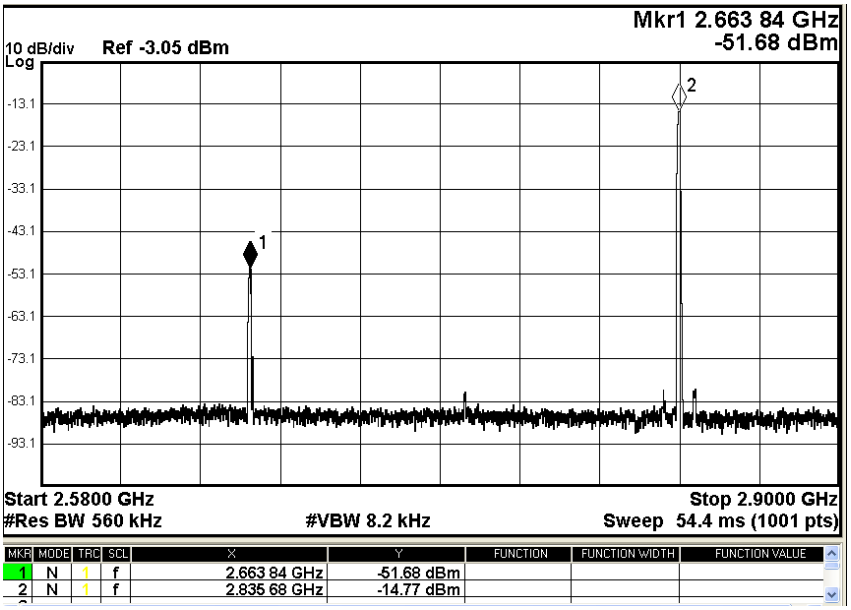


Fig. 20: Measured interleaving spur of $-36.9\,\text{dBc}$ at $2.67\,\text{GHz}$ with a $2.83\,\text{GHz}$ tone to estimate the DCE.

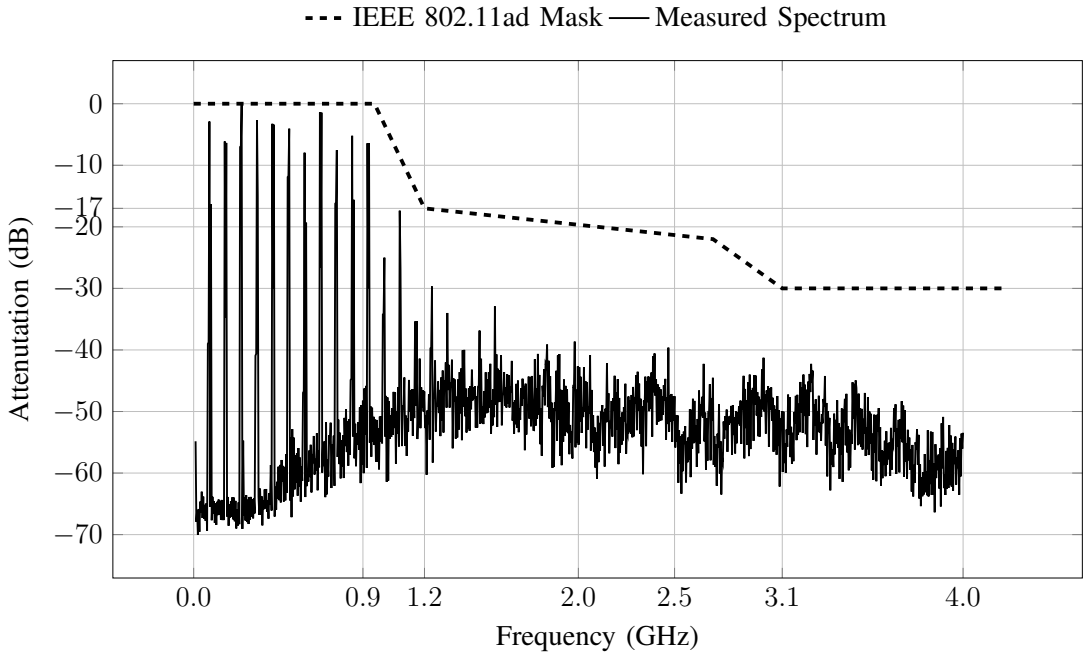


Fig. 21: Measured Spectral Mask with 16-QAM single-carrier random data at $10.56\,\text{GS/s}$.

TABLE V: Comparison with complete $\Delta\Sigma$ DACs having >2.5 GS/s sampling rate.

Paper	Seddighrad [13] ESSCIRC'08	Frappe [14] JSSC'09	Jerng [11] JSSC'07	Bhide [20] TCAS-II'13	This Work
Mod. Type	EFB	EFB	MASH	TI MASH	LA-TI MASH
Tech.	90nm	90nm	0.13μm	65nm	65nm
Inp./Out Bits	10/3	13/1	12/3	12/3	8/4
Order	2	3	2	2	2
Speed (GS/s)	3.6	4	2.6	8	11
BW (MHz)	10	50	100	200	1100
SNDR (dB)	70	53	30	26	39
IM3 ($-$dBc)	70	-	51	57	49
Area (mm^2)	-	$<$0.15	$<$0.11*	0.13	0.14
Power (mW)	16	54*	40*	68	117
$V_{pp\text{-}diff}$ 50Ω	0.3*	1.3	0.35	0.3	0.5

* Estimated.

TABLE VI: Comparison with other Digital $\Delta\Sigma$ Modulators with $>$ 5 GHz speed.

Ref.	**Tech. (nm)**	**Freq. (GHz)**	**Type**	**P (mW)**	**Area (mm^2)**
Pozsgay [12] ISSCC'08	65	5.4	5b, 3rd ord MASH	$>$48	–
Bhide [20] TCAS-II'13	65	8	12b, 2nd ord 2-ch TI-MASH	62	0.075
Su [23] JSSC'15	65	8	12b, 3rd ord 8-ch TI-MASH	$<$165	–
This Work	65	11	8b, 2nd ord 2-ch LA TI-MASH	70	0.098

TABLE VII: Comparison of this work with wideband Nyquist DACs.

	OSR=5	Low OSR(=1,2) Nyq. DACs			High-speed Nyq. DACs (OSR=3−8)		
Paper	This Work	[7] Tokumaru CICC'09	[4] Saito JSSC'13	[30] Tual VLSI'11	[16] Savoj JSSC'08	[28]† Radulov TVLSI'14	[18]† Olieman JSSC'15
DAC	$\Delta\Sigma$	Nyq.	Nyq.	Nyq.	Nyq.	Nyq.	Nyq.
Usage	60-GHz Radio	60-GHz Radio	60-GHz Radio	Comm. SoC	Wireline Backplane	Comm. SoC	–
Tech. (nm)	65	110	65	65	90	28	28
Inp. Bits	8	8	7	9	8	6	9
Speed (GS/s)	11	3.4	3.5	3	12	7	11
BW (MHz)	1100	890	880	1500	750	1000	1100
SFDR (dBc)	53	31	48	55	51	50	56
IM3 (−dBc)	49	–	–	60	–	50	57
Swing (V)	0.5	0.6*	0.6*	0.4	1.6	0.25	0.425
Power (mW)	117	100	71	60	113	145	<110
Area (mm^2)	0.14	0.125	0.085	0.04	<0.2	0.035	0.04
FOM** (10^{12} V Hz/W)	2.1	0.19	1.87	5.62	3.77	0.55	>2.68

*- Estimated.** **FOM**= $\frac{V_{swing}}{P} \times \text{BW} \times 10^{\frac{\text{SFDR}}{20}}$. [29]

† Extracted performance in 0−1.1 GHz band.

LIST OF FIGURES

LIST OF TABLES