Linköping Studies in Science and Technology Dissertations No. 1702

Thermal Issues in Testing of Advanced Systems on Chip

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Many cutting-edge computer and electronic products are powered by advanced Systems-on-Chip (SoC). Advanced SoCs encompass superb performance together with large number of functions. This is achieved by efficient integration of huge number of transistors. Such very large scale integration is enabled by a core-based design paradigm as well as deep-submicron and 3D-stacked-IC technologies. These technologies are susceptible to reliability and testing complications caused by thermal issues. Three crucial thermal issues related to temperature variations, temperature gradients, and temperature cycling are addressed in this thesis.

Existing test scheduling techniques rely on temperature simulations to generate schedules that meet thermal constraints. The difference between the simulated temperatures and the actual temperatures is an error. This error, for past technologies, is negligible. However, advanced SoCs experience large errors due to large process variations. Such large errors have costly consequences, such as overheating, and must be taken care of.

Advanced SoCs manufactured as 3D stacked ICs experience large temperature gradients. Temperature gradients accelerate certain early-life defect mechanisms. These mechanisms can be artificially accelerated by enforcing the gradients so that the corresponding defects are detected on time. Moreover, temperature gradients exacerbate some delay-related defects. In order to detect such defects, testing must be performed when appropriate temperature-gradients are enforced.

The last thermal issue addressed by this thesis is related to temperature cycling. Temperature cycling test procedures are used to detect cycling-related early-life failures. Such failures affect advanced SoCs, particularly through-silicon-via structures in 3D stacked ICs. Existing temperature cycling testing techniques are too costly for 3D stacked ICs and therefore new inexpensive techniques must be developed.

This thesis presents several test-scheduling based techniques to address the thermal issues discussed above. All the proposed techniques have been implemented and evaluated with extensive experiments based on ITC'02 benchmarks as well as a number of 3D stacked ICs. Experiments show that the proposed techniques work effectively and reduce the test costs. We have also developed a fast temperature simulation technique based on a closed-form solution for the temperature equations. Experiments demonstrate that the proposed simulation technique reduces the test schedule generation time by more than half.

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