Analysis and design of low noise transconductance amplifier for selective receiver front-end

Quoc Tai Duong, Fahad Qazi and Jerzy Dabrowski

Linköping University Post Print

N.B.: When citing this work, cite the original article.

The original publication is available at www.springerlink.com:

Quoc Tai Duong, Fahad Qazi and Jerzy Dabrowski, Analysis and design of low noise transconductance amplifier for selective receiver front-end, 2015, Analog Integrated Circuits and Signal Processing, (85), 2, 361-372.

<http://dx.doi.org/10.1007/s10470-015-0629-5>

Copyright: Springer Verlag (Germany)

<http://www.springerlink.com/?MUD=MP>

Postprint available at: Linköping University Electronic Press

<http://urn.kb.se/resolve?urn=urn:nbn:se:liu:diva-122187>

Analysis and Design of Low Noise Transconductance Amplifier for Selective Receiver Front-End

Quoc-Tai Duong, *Student Member IEEE*, Fahad Qazi, *Member IEEE*,
and Jerzy J. Dąbrowski, *Senior Member IEEE*

Abstract—Analysis and design of a low-noise transconductance amplifier (LNTA) aimed at selective current-mode (SAW-less) wideband receiver front-end is presented. The proposed LNTA uses double cross-coupling technique to reduce noise figure (NF), complementary derivative superposition (DS), and resistive feedback to achieve high linearity and enhance input matching. The analysis of both NF and IIP3 using Volterra series is described in detail and verified by *SpectreRF*® circuit simulation showing $NF < 2$ dB and $IIP3 = 18$ dBm at 3 GHz. The amplifier performance is demonstrated in a two-stage highly selective receiver front-end implemented in 65 nm CMOS technology. In measurements the front-end achieves blocker rejection competitive to SAW filters with noise figure 3.2–5.2 dB, out of band $IIP3 > +17$ dBm and blocker $P_{1dB} > +5$ dBm over frequency range of 0.5–3 GHz.

Index Terms— Low-noise transconductance amplifier (LNTA), highly linear LNA, wideband LNA, SAW-less receiver, wideband selective RF front-end.

I. INTRODUCTION

FOR a multi-standard radio receiver the wideband RF front-end circuit is essential. It is well known that a low-noise amplifier (LNA) as the first front-end stage largely decides the receiver performance in terms of noise figure (NF) and linearity. With relaxed requirements on RF filters the demands placed on the front-end linearity are usually increased according to intermodulation or cross-modulation effects evoked by strong interferers. While the nonlinear contribution of the following receiver stages is raised by the LNA gain, the overall NF is reduced. As a consequence a reasonable balance between linearity and noise performance of the LNA, mixer, and to some extent the baseband stages must be attained. One possible solution to this problem is a current-mode front-end where LNA is a transconductance amplifier (LNTA) followed by a passive mixer [1–7]. Since current rather than a voltage is applied, the mixer design is simplified and also the effect of $1/f$ noise is diminished. Most of those designs implement the concept of so called SAW-less front-end making use of N-path filtering [8]. In fact, it is the high output impedance of LNTA that jointly with low impedance of the N-path circuitry enables significant blocker attenuation at offset frequencies. In this case the demands for the input range (up to 0 dBm, i.e. 632

mV_{pp}), and respectively for the linearity and compression of the LNTA, are exacerbated since the attenuation is achieved at the output rather than at the input of the amplifier. Additionally, such an LNTA is challenged by the requirement of wideband (WB) operation typical of the contemporary multi-band radios.

The LNTA nonlinearity originates from two major sources: nonlinear transconductance which converts linear input voltage to nonlinear output drain current, and nonlinear output conductance, the effect of which is evident under large output voltage swing. The latter can be avoided using a low impedance output load that is usually achieved using a passive mixer followed by a transimpedance amplifier (TIA) [1–6].

Several techniques exist to improve linearity of LNAs [9]. The optimization of gate bias voltages can fairly improve linearity of LNA [10] but it leads to reduced range of the input amplitudes and increased sensitivity to process variation. The WB negative feedback by resistive source degeneration also improves linearity but limits the voltage headroom of the devices and adds extra noise. Superposition of an auxiliary transistor to cancel nonlinearity of the main device, called derivative superposition (DS), extends fairly the linear gain range [11, 12]. Its variant referred to as the complementary DS also improves the second order nonlinearity of the amplifier [13]. More recently, this technique has been also presented in [15, 17, 7]. Unlike DS, in the post-distortion technique (PD) the auxiliary device operates in saturation and is controlled by the output voltage. The PD advantage is in superior PVT robustness as demonstrated e.g. in [18].

Other critical concerns in LNA/LNTA design i.e., the input matching and noise figure (NF) usually cannot be compromised. A popular wideband matching technique exploits the common gate (CG) circuit with its input impedance approximated by the inverse of the front device transconductance ($1/g_m$). Since in this case g_m is virtually bound to 20 mS, achieving larger effective values of the amplifier transconductance requires an extra amplification stage. To guarantee NF of the CG amplifier below 3 dB extra mechanisms are necessary, such as negative /positive feedback [23, 24], output noise cancellation using an auxiliary amplifier [20] (also called feed forward cancellation), or capacitive cross coupling when a balanced circuit is used [19]. Another WB matching technique providing a low NF is based on the reactive feedback which requires on-chip RF transformers [21].

A combination of a low noise figure with high linearity for wideband LNTA applications in CMOS was presented in [1–

Manuscript received May 04, 2015. This work was supported by Swedish Foundation for Strategic Research.

Q-T. Duong and J. Dąbrowski are with the Dept. of Electrical Engineering, Linköping University, Sweden, SE-581 83, Sweden, F. Qazi is with Catena AB, Stockholm, Sweden, (e-mail: tai.qazi@isy.liu.se).

6, 13, 14, 25]. In particular, the noise cancelling receiver demonstrated in [4] extends the noise cancelling to the N-path filter / mixer resulting in the superior NF, but it consumes more power than the circuits using conventional noise cancellation [1-3, 5, 6].

In this paper we present analysis and design of LNTA suitable for current-mode wideband front-end with RF N-path filtering in 0.5 to 3 GHz frequency range. The LNTA design combines two linearization techniques, namely the derivative superposition and resistive feedback, with NF reduction by double capacitive cross-coupling which results in superior noise performance. The resistive feedback also helps to attain good input matching without sacrificing gain of the common gate input stage. By using elevated supply voltage the LNTA can tolerate blockers up to 0 dBm without compression. The mathematical analyses of NF and IIP3 are described in detail and the achieved estimates are verified by *SpectreRF*® simulation. The LNTA is implemented and measured in a two-stage highly selective receiver front-end, integrated using 65 nm CMOS technology [7].

The paper is arranged as follows. In Section II we derive the LNTA circuit architecture combining various mechanisms to achieve the intended performance. In Section III we analyze the noise figure and verify the attained estimate by simulation. The Volterra series based analysis of IIP3 and verification is presented in Section IV. In Section V the LNTA implementation as a part of the receiver front-end with RF N-path filtering is presented. Conclusion is provided in the last section.

II. LNTA DESIGN

Based on our preliminary work [17], here, we describe the LNTA design in detail, including a complete noise and linearity analysis.

For high linearity we refer to the complementary DS technique, which due to the reusing of current, gives also significant power savings. The complementary common gate (CG) architecture has been preferred over its counterpart, common source (CS) (Fig. 1), for the ease in achieving wideband input matching and low noise figure.

By using appropriate bias voltages the nonlinear third order g_m terms can be cancelled providing a high value of IIP3 [13, 14, 15, 16]. In this case the pMOS is an auxiliary transistor with g_m much smaller than that of nMOS. Large off-chip inductors L_1 , L_2 rather than resistors are used to guarantee maximum bias voltage V_{ds} and thereby to reduce the g_{ds} nonlinearity that is increasingly pronounced in deep submicron CMOS.

The input impedance and noise factor for the DS-CG circuit can be estimated from

$$Z_{in} = \frac{1}{g_{mn} + g_{mp}} \quad (1)$$

$$F \cong 1 + \frac{\gamma}{\alpha(g_{mn} + g_{mp})R_{so}} \quad (2)$$

Figure 1. LNTA complementary DS architectures, a) common source b) common gate.

where R_{so} is the source resistance, γ is the excess channel thermal noise coefficient, and $\alpha = g_m/g_{do}$, with g_m as the device transconductance and g_{do} as zero-biased channel conductance. Clearly, for perfect matching we have $F \approx 1 + \gamma/\alpha$. In deep submicron CMOS $\gamma/\alpha > 2/3$, and to reduce its effect on F we use a differential (balanced) variant of this circuit where the capacitive cross-coupling technique is adopted [19, 22]. In this case, F can be estimated from

$$F \cong 1 + \frac{\gamma}{2\alpha} \quad (3)$$

according to partial noise cancellation achieved in this circuit. We observe that for $\gamma/\alpha \approx 1$, the expected noise figure is $NF = 10\log(1.5) \approx 1.75$ dB.

Further noise factor improvement as we proposed in [17] can be achieved by using double capacitive cross-coupling circuit shown in Fig. 2 (to be discussed in detail in Sec. III).

By sizing up the transistors the LNTA transconductance can be increased to some extent, but the input impedance is decreased accordingly and the reflection coefficient S11 is largely deteriorated. One solution to mitigate this tradeoff is based on the source degeneration technique. Acting as a local negative feedback it additionally improves circuit linearity. With a resistance R_{sn} as shown in Fig. 3 the LNTA input impedance can be restored as demonstrated by (4) for the n-MOS part of the circuit. Knowing that $g_m/C_{gs} = 2\pi f_T$ where $f_T \approx 100$ GHz, for simplicity we can assume $\omega C_{gs}/g_m = f/f_T \approx 0$. Then for the nMOS part of the circuit we find

$$Z_{in}^{(n)} \cong \frac{1 + Z_L Y_{dsn} + R_{sn}(g_{mn} + Y_{dsn})}{g_{mn} + Y_{dsn}/2} \quad (4)$$

where Y_{dsn} is the drain-source admittance and Z_L is the loading impedance while the inductor reactance goes to infinity. A similar formula can be derived for the pMOS part ($Z_{in}^{(p)}$) and assuming the drain-source admittances are small enough we find the LNTA input impedance as $Z_{in}^{(p)} \parallel Z_{in}^{(n)}$. The LNTA transconductance is inversely proportional to Z_{in} that is

$$G_m = \frac{1}{Z_{in}^{(p)}(\omega)} + \frac{1}{Z_{in}^{(n)}(\omega)} \quad (5)$$

Figure 2. Differential LNTA implementing DS and capacitive cross-coupling technique (simplified schematic).

Figure 3. S11 and linearity improvement by resistive source degeneration.

Hence, there is a tradeoff between the input matching and LNTA gain. For perfect matching no increase in G_m is achieved. In practice, however, the requirement is $S_{11} < -10$ dB. To meet this condition the corresponding boundaries of Z_{in} can be found: $Z_{in} \in (0.67, 2)R_{so}$, where R_{so} is the matching resistance. In an extreme case, when $Z_{in} = 2R_{so}$ and $R_s = 0$ we have $G_m \approx 2/2R_{so}$. Next, the transistors are sized up and by using R_s we obtain $Z_{in} = 0.67R_{so}$ with the corresponding $G_m \approx 3/R_{so}$. This means $3\times$ increase in G_m (9.5 dB) is feasible while $S_{11} = -10$ dB. Clearly, larger values of R_s should be avoided here to preserve a sufficient V_{ds} voltage headroom. Also the noise factor is traded for S_{11} as the R_s resistors add noise. Moreover, when the loading impedance Z_L is selective (as for N-path filters), its impedance goes down at offset frequencies and the input impedance (4) is reduced accordingly providing thereby attenuation of blockers at the amplifier input.

The proposed final LNTA circuit, designed in 65 nm CMOS is shown in Fig.4. It combines the discussed above techniques to achieve high linearity and a low noise figure over a wide frequency range. Four off-chip inductors providing reactance of a few hundred Ohms each are large enough to guarantee $S_{11} < -10$ dB also at lower frequencies. Similarly, the coupling capacitances $C_s > 10$ pF should be chosen ($X_s < 2\Omega$)

to avoid reduction of LNTA transconductance gain. Four of them (connected to transistor gates) must be integrated at the expense of the silicon area overhead. After choosing the bias voltages (to be discussed in Sec. IV) and the output DC equal to $V_{DD}/2$ the sizes of the MOS transistors M_p , M_n were chosen to achieve the best third-order g_m cancellation with $29\mu\text{m}/65\text{nm}$ and $48\mu\text{m}/65\text{nm}$, respectively. The source degeneration resistors providing correction of S11 are $R_{sp} = 17\Omega$ and $R_{sn} = 111\Omega$.

Figure 4. Circuit schematic of proposed wideband LNTA.

III. LNTA NOISE ANALYSIS

The circuit model for noise analysis is shown in Fig.5. In each half of the circuit there are five noise sources to be considered: v_{ns} (source noise), v_{nM1} (of M_1), v_{nM3} (of M_3), v_{nRsp} (of R_{sp}) and v_{nRsn} (of R_{sn}), using the following equations

$$\begin{aligned} v_{ns}^2 &= 4kTR_{so}, \\ v_{nM1}^2 &= \frac{4kT\gamma_1}{\alpha_1 g_{m1}}, \quad v_{nM3}^2 = \frac{4kT\gamma_3}{\alpha_3 g_{m3}}, \\ v_{nRsn}^2 &= 4kTR_{sn}, \quad v_{nRsp}^2 = 4kTR_{sp}, \end{aligned} \quad (6)$$

where k is Boltzmann's constant, T is the absolute temperature in Kelvin. The differential noise current at the output $i_{n,out} = i_y - i_x$ can be calculated using superposition principle. In particular for v_{ns} the currents $i_1, \dots, i_4$ as shown in Fig.5 can be found as

$$i_{1,3} = (v_y - v_x)g_{m1,3t}, \quad i_{2,4} = (v_x - v_y)g_{m2,4t} \quad (7)$$

with

$$g_{m1,2t} = \frac{1}{R_{sn} \left(1 + \frac{sC_{gsn}}{g_{m1,2}} \right) + \frac{1}{g_{m1,2}}}$$

$$g_{m3,4t} = \frac{1}{R_{sp} \left(1 + \frac{2sC_{sgp}}{g_{m3,4}} \right) + \frac{1}{g_{m3,4}}} \quad (8)$$

Using Kirchhoff's Voltage Law (KVL) for the loop from v_x to v_y through v_{ns} and Kirchhoff's Current Law (KCL) at nodes v_x , v_y we have

$$\begin{aligned} v_x - v_y &= v_{ns} + R_{so} \left[i_1 \left(1 + \frac{2sC_{gsn}}{g_{m1}} \right) + i_3 \left(1 + \frac{2sC_{sgp}}{g_{m3}} \right) \right] \\ &- R_{so} \left[i_2 \left(1 + \frac{2sC_{gsn}}{g_{m2}} \right) + i_4 \left(1 + \frac{2sC_{sgp}}{g_{m4}} \right) \right] \end{aligned} \quad (9)$$

Figure 5. LNTA circuit for noise analysis.

Substituting (7) into (9), the voltage of $v_x - v_y$ can be found as

$$v_x - v_y = \frac{v_{ns}}{1 + R_{so} \sum_{k=1}^4 g_{mktz}} \quad (10)$$

with

$$\begin{aligned} g_{m1,2tz} &= g_{m1,2} \left(1 + \frac{2sC_{gsn}}{g_{m1,2}} \right), \\ g_{m3,4tz} &= g_{m3,4} \left(1 + \frac{2sC_{sgp}}{g_{m3,4}} \right) \end{aligned} \quad (11)$$

The output differential noise current $i_{ns_out} = i_y - i_x$ due to noise source of v_{ns} can be calculated as

$$i_{ns_out} = \frac{-v_{ns} \sum_{k=1}^4 g_{mkt}}{1 + R_{so} \sum_{k=1}^4 g_{mktz}} \quad (12)$$

With similar procedure, we can calculate the output differential noise currents i_{nM1_out} , i_{nM3_out} , i_{nRsp_out} , i_{nRsn_out} due to v_{nM1} , v_{nM3} , v_{nRsp} and v_{nRsn} respectively

$$i_{nM3_out} = \frac{-R_{so} v_{nM3} [g_{m3tz} (1 + R_{sp} sC_{sgp}) - 2sC_{sgp} \sum_{k=1}^4 g_{mkt}]}{1 + R_{so} \sum_{k=1}^4 g_{mktz}} + v_{nM3} g_{m3t} (1 + R_{sp} sC_{sgp}) \quad (13)$$

$$i_{nM1_out} = \frac{-R_{so} v_{nM1} [g_{m1tz} (1 + R_{sn} sC_{gsn}) - 2sC_{gsn} \sum_{k=1}^4 g_{mkt}]}{1 + R_{so} \sum_{k=1}^4 g_{mktz}} + v_{nM1} g_{m1t} (1 + R_{sn} sC_{gsn}) \quad (14)$$

$$i_{nRsn_out} = \frac{R_{so} v_{nRsn} g_{m1t} \left(1 + \frac{2sC_{gsn}}{g_{m1}} \right) \sum_{k=1}^4 g_{mkt}}{1 + R_{so} \sum_{k=1}^4 g_{mktz}} - v_{nRsn} g_{m1t} \quad (15)$$

$$i_{nRsp_out} = \frac{R_{so} v_{nRsp} g_{m3t} \left(1 + \frac{2sC_{sgp}}{g_{m3}} \right) \sum_{k=1}^4 g_{mkt}}{1 + R_{so} \sum_{k=1}^4 g_{mktz}} - v_{nRsp} g_{m3t} \quad (16)$$

TABLE I.
NF VERSUS (γ/α) COMPARISON OF (3) AND (21)

(γ/α)	2/3	1	1.5	2	2.5	3
$NF_{cross-coupling}$ (dB)	1.25	1.76	2.43	3.01	3.52	3.98
$NF_{proposed}$ (dB)	0.88	1.07	1.34	1.59	1.83	2.06
ΔNF (dB)	0.37	0.69	1.09	1.42	1.69	1.92

Figure 6. NF comparison of analytical model (12-18) and SpectreRF® circuit simulation for proposed LNTA (transistor level).

The same noise contribution will be achieved from the other half of the circuit. The noise factor (F) and noise figure (NF) will be calculated based on (12-16) as

$$F = \frac{2i_{ns_out}^2 + 2i_{nM1_out}^2 + 2i_{nM3_out}^2 + 2i_{nRsn_out}^2 + 2i_{nRsp_out}^2}{2i_{ns_out}^2} \quad (17)$$

$$NF = 10 \log_{10}(F) \quad (18)$$

In order to compare NF of the proposed circuit to the one with conventional cross-coupling, the equivalent circuit can be simplified by ignoring the gate-source capacitances. The noise factor in this case will be

$$F = 1 + \frac{\gamma_1 g_{m1}^2}{\alpha_1 g_{m1} R_{so} \left(\sum_{k=1}^4 g_{mkt} \right)^2} + \frac{\gamma_3 g_{m3}^2}{\alpha_3 g_{m3} R_{so} \left(\sum_{k=1}^4 g_{mkt} \right)^2} \quad (19)$$

$$+ \frac{g_{m1t}^2}{\left(\sum_{k=1}^4 g_{mkt} \right)^2} \frac{R_{sn}}{R_{so}} + \frac{g_{m3t}^2}{\left(\sum_{k=1}^4 g_{mkt} \right)^2} \frac{R_{sp}}{R_{so}}$$

The input impedance of the differential circuit ideally should be $Z_{in} = 2R_{so}$. Then for matching we need

$$Z_{in} = 2R_{so} = \frac{2}{\sum_{k=1}^4 g_{mkt}} \quad (20)$$

For brevity we can assume that the differential circuit is perfectly balanced having the same γ , α values for all transistors. Then (19) can be simplified to

$$F = 1 + \frac{\gamma \left(\frac{g_{m1}^2}{g_{m1}} + \frac{g_{m3}^2}{g_{m3}} \right)}{4\alpha R_{so} (g_{m1t} + g_{m3t})^2} + \frac{(R_{sn} g_{m1}^2 + R_{sp} g_{m3}^2)}{4R_{so} (g_{m1t} + g_{m3t})^2} \quad (21)$$

It should be noted that the double cross-coupling results in $1/4$ coefficient for the (γ/α) contribution as compared to $1/2$ for the traditional cross-coupling. Moreover, the noise factor contribution by the source degeneration resistors (the 3rd term in (21)) appears less than the one by transistors for $(\gamma/\alpha) > 1$. A comparison between NF of the proposed circuit and the conventional one (3) for $g_{m1} = g_{m2} = 30$ mS, $g_{m3} = g_{m4} = 13.6$ mS, $R_{so} = 50 \Omega$, $R_{sn} = 111 \Omega$, $R_{sp} = 17 \Omega$, is shown in Table I. With technology scaling the ratio (γ/α) is increasingly large so the NF improvement is more pronounced. For example with $(\gamma/\alpha) = 1.5$ the proposed LNTA can improve NF from 2.43 dB down to 1.34 dB.

The NF comparison of the presented analytical model and SpectreRF® circuit simulation including the gate-source

Figure 7. a) Schematic of conventional inverter, b) Simulation of third-order transconductances of PMOS g_{3p} , NMOS g_{3n} and output g_3 .

capacitances according to (12-16) is shown in Fig. 6. In this verification we use specifications captured from the designed chip: $g_{m1} = g_{m2} = 30$ mS, $g_{m3} = g_{m4} = 13.6$ mS, $R_{so} = 50 \Omega$, $R_{sp} = 17.2 \Omega$, $R_{sn} = 110.8 \Omega$, $C_{gsn} = 30$ fF, $C_{gsp} = 20$ fF. As seen the respective differences remain within 0.08 dB that can be considered negligible.

IV. LINEARITY ANALYSIS USING VOLTERRA SERIES

The simulation environment using a conventional inverter, here, also considered as common-source complementary DS circuit, with output bias voltage was proposed in [13] as shown in Fig. 7a. This circuit can achieve high linearity due to subtraction of the nonlinear current components of the transistors M_p and M_n . Both the second and third order terms can be partly cancelled if the circuit is appropriately biased. However, the useful input range is very narrow as shown for g_3 in Fig. 7b where $g_3 = \partial^3 i_o / \partial (V_{in})^3$. In effect the possible blockers are not well tolerated by this circuit, still resulting in significant distortion.

A possible way to overcome this problem is using different bias voltages for M_p and M_n in combination with the resistive source degeneration applied to the both transistors as presented in Fig. 8a [17]. In Fig. 8b, the input voltage range can be significantly increased comparing the previous case in Fig. 7b. The combined g_3 is less than its components g_{n3} and g_{p3} in the operating range as seen in the zoom view. Moreover, it should be noted that R_{sp} is much less than R_{sn} in order to maintain the output bias voltage at $V_{dd}/2$ while M_n is larger than M_p . Should we increase the size of M_p and the resistance of R_{sp} , the effective g_3 would be less, but its range would shrink degrading the linearity for large blockers.

The following analysis aims at describing IIP3 and third-order gain H_3 of LNTA using the Volterra series approach. Figure 9 shows the small-signal model for linearity analysis where the differential circuits are assumed to be identical for simplicity. The drain current of M_p and M_n can be modelled up to 3rd-order as

$$i_{dp} = g_{1p} v_{sgp} + g_{2p} v_{sgp}^2 + g_{3p} v_{sgp}^3 \quad (22)$$

$$i_{dn} = g_{1n} v_{gsn} + g_{2n} v_{gsn}^2 + g_{3n} v_{gsn}^3 \quad (23)$$

where g_{ip} and g_{in} are the i^{th} -order coefficients of M_p and M_n , accordingly, obtained by taking the derivative of the drain DC current I_{SD}/I_{DS} with respect to the gate-source voltage V_{SG}/V_{GS} at the DC bias point

Figure 8. a) Schematic of resistive-feedback technique, b) Simulation of third-order transconductances of PMOS g_{3p} , NMOS g_{3n} and output g_3 .

$$g_{1p} = \frac{\partial I_{SDP}}{\partial V_{SGP}}, \quad g_{1n} = \frac{\partial I_{DSN}}{\partial V_{GSN}} \quad (24)$$

$$g_{2p} = \frac{1}{2!} \frac{\partial^2 I_{SDP}}{\partial V_{SGP}^2}, g_{2n} = \frac{1}{2!} \frac{\partial^2 I_{DSN}}{\partial V_{GSN}^2} \quad (25)$$

$$g_{3p} = \frac{1}{3!} \frac{\partial^3 I_{SDP}}{\partial V_{SGP}^3}, g_{3n} = \frac{1}{3!} \frac{\partial^3 I_{DSN}}{\partial V_{GSN}^3} \quad (26)$$

Applying the Volterra series to the output voltage

$$v_{outm} = G_1 \circ v_{in} + G_2 \circ v_{in}^2 + G_3 \circ v_{in}^3 \quad (27)$$

$$v_{in} = A_1 \circ v_{so} + A_2 \circ v_{so}^2 + A_3 \circ v_{so}^3 \quad (28)$$

$$v_{out} = H_1 \circ v_{so} + H_2 \circ v_{so}^2 + H_3 \circ v_{so}^3 \quad (29)$$

Figure 9. Equivalent circuit of a proposed wideband LNTA.

where $v_{in} = v_{inp} - v_{inn}$ and $v_{out} = v_{outp} - v_{outn}$. If circuits are completely symmetric v_{out} can be calculated as

$$v_{outp} = -G_1 \circ v_{in} + G_2 \circ v_{in}^2 - G_3 \circ v_{in}^3 \quad (30)$$

$$v_{out} = -2G_1 \circ v_{in} - 2G_3 \circ v_{in}^3 \quad (31)$$

From (27) and (A.15) from Appendix A, we have

$$G_1 = \frac{-\hat{Z}_L \left\{ \left(g_{1p} + \frac{1}{r_{dp}} \right) n_p + \left(g_{1n} + \frac{1}{r_{dn}} \right) n_n \right\}}{\eta_L} \quad (32)$$

$$G_2 = \frac{\hat{Z}_L \left\{ \frac{g_{2p} G_{1p}^2}{(1+k_p)^3 m_p^2} - \frac{g_{2n} G_{1n}^2}{(1+k_n)^3 m_n^2} \right\}}{\eta_L} \quad (33)$$

$$G_3 = \frac{\frac{\hat{Z}_L G_{1p}}{(1+k_p)^3 m_p^2} \left\{ 2g_{2p} \frac{R_{sp}}{r_{dp}} G_2 + \frac{G_{1p}^2}{(1+k_p) m_p} \left[g_{3p} - \frac{2R_{sp} g_{2p}^2}{(1+k_p) m_p} \right] \right\} - \frac{\hat{Z}_L G_{1n}}{(1+k_n)^3 m_n^2} \left\{ 2g_{2n} \frac{R_{sn}}{r_{dn}} G_2 + \frac{G_{1n}^2}{(1+k_n) m_n} \left[g_{3n} - \frac{2R_{sn} g_{2n}^2}{(1+k_n) m_n} \right] \right\}}{\eta_L} \quad (34)$$

where

$$\eta_L = 1 - \hat{Z}_L \left\{ \left(g_{1p} + \frac{1}{r_{dp}} \right) R_{sp} + \left(g_{1n} + \frac{1}{r_{dn}} \right) R_{sn} \right\} \quad (35a)$$

$$G_{1p} = -n_p + \frac{R_{sp}}{r_{dp}} G_1, G_{1n} = n_n - \frac{R_{sn}}{r_{dn}} G_1 \quad (35b)$$

Substituting (A.17-22), (A.3), (A.9-13), (22-23) into (A.16) and comparing with (28), we can find A_1 , A_2 and A_3

$$A_1 = \frac{1}{1 + 2R_{so} \left\{ \frac{1}{2} \left(\frac{1}{sL_p} + \frac{1}{sL_n} - \frac{1}{r_{dp}} - \frac{1}{r_{dn}} \right) + G_1 \left(\frac{1}{r_{dp}} + \frac{1}{r_{dn}} \right) + G_{1p} \left[\frac{-2sC_{sgp} - \frac{1}{r_{dp}} + \frac{m_p}{R_{sp}}}{(1+k_p) m_p} - \frac{1}{R_{sp}} \right] + G_{1n} \left[\frac{2sC_{gsn} + \frac{1}{r_{dn}} - \frac{m_n}{R_{sn}}}{(1+k_n) m_n} + \frac{1}{R_{sn}} \right] \right\}} \quad (36)$$

$$A_2 = 2R_{so} A_1^3 \left\{ \frac{R_{sp} g_{2p}}{(1+k_p)^3 m_p^3} \left(\frac{1}{r_{dp}} - \frac{m_p}{R_{sp}} \right) \left(-n_p + \frac{R_{sp}}{r_{dp}} G_1 \right)^2 - \frac{R_{sn} g_{2n}}{(1+k_n)^3 m_n^3} \left(\frac{1}{r_{dn}} - \frac{m_n}{R_{sn}} \right) \left(n_n - \frac{R_{sn}}{r_{dn}} G_1 \right)^2 \right\} \quad (37)$$

$$\begin{aligned}
A_3 = & 2R_{so}A_1^2 \frac{sC_{gsp}}{(1+k_p)m_p} \left\{ \left[\frac{R_{sp}}{r_{dp}} G_3 A_1^2 - \frac{2A_2 R_{sp} g_{2p}}{(1+k_p)^2 m_p^2} G_{1p}^2 \right] + \frac{R_{sp} A_1^2}{(1+k_p)^3 m_p^3} \left[\left(\frac{2g_{2p}^2 R_{sp}}{(1+k_p)m_p} - g_{3p} \right) G_{1p}^3 \right] \right\} \\
& - 2R_{so}A_1^2 \frac{\left(sC_{gsp} + \frac{1}{r_{dp}} - \frac{m_p}{R_{sp}} \right)}{(1+k_p)m_p} \left\{ \left[-\frac{R_{sp}}{r_{dp}} G_3 A_1^2 - \frac{2A_2 R_{sp} g_{2p}}{(1+k_p)^2 m_p^2} G_{1p}^2 \right] - \frac{R_{sp} A_1^2}{(1+k_p)^3 m_p^3} \left[\left(\frac{2g_{2p}^2 R_{sp}}{(1+k_p)m_p} - g_{3p} \right) G_{1p}^3 \right] \right\} \\
& - 2R_{so}A_1^2 \frac{sC_{gsn}}{(1+k_n)m_n} \left\{ \left[-\frac{R_{sn}}{r_{dn}} G_3 A_1^2 - \frac{2A_2 R_{sn} g_{2n}}{(1+k_n)^2 m_n^2} G_{1n}^2 \right] + \frac{R_{sn} A_1^2}{(1+k_n)^3 m_n^3} \left[\left(\frac{2g_{2n}^2 R_{sn}}{(1+k_n)m_n} - g_{3n} \right) G_{1n}^3 \right] \right\} \\
& + 2R_{so}A_1^2 \frac{\left(sC_{gsn} + \frac{1}{r_{dn}} - \frac{m_n}{R_{sn}} \right)}{(1+k_n)m_n} \left\{ \left[\frac{R_{sn}}{r_{dn}} G_3 A_1^2 - \frac{2A_2 R_{sn} g_{2n}}{(1+k_n)^2 m_n^2} G_{1n}^2 \right] - \frac{R_{sn} A_1^2}{(1+k_n)^3 m_n^3} \left[\left(\frac{2g_{2n}^2 R_{sn}}{(1+k_n)m_n} - g_{3n} \right) G_{1n}^3 \right] \right\}
\end{aligned} \tag{38}$$

Figure 10. The third-order voltage gain H_3 (41) versus the bias voltage V_{gsn} .

If two single-ended circuits are identical, we substitute (28, 29) into (31) and have

$$H_1(\omega_1) = -2G_1(\omega_1)A_1(\omega_1) \tag{39}$$

$$H_2(\omega_1, \omega_2) = -2G_1(\omega_1 \pm \omega_2)A_2(\omega_1, \omega_2) \tag{40}$$

$$\begin{aligned}
H_3(\omega_1, \omega_2, \omega_3) = & -2[G_1(\omega_1 \pm \omega_2 \pm \omega_3)A_3(\omega_1, \omega_2, \omega_3) \\
& + G_3(\omega_1, \omega_2, \omega_3)A_1^3(\omega_1 \pm \omega_2 \pm \omega_3)]
\end{aligned} \tag{41}$$

From [18, 25], IIP3 can be estimated as

$$IIP_{3,dBm} = 20 \log_{10} \left(\sqrt{\frac{4}{3} \frac{H_1(\omega_1)}{H_3(\omega_1, \omega_2, \omega_3)}} \right) + 10 \tag{42}$$

DS technique has been used to cancel the third-order transconductance distortion g_3 well [9] but the operating range of input voltage V_{gs} is not wider than 200 mV. In this design, we propose a technique that can cancel the third-order voltage gain (41) in larger operating range up to 650 mV shown in Fig. 10. From that figure, the bias voltages can be chosen as $V_{gsn} = 570$ mV and $V_{sgp} = V_{gsn} + 190$ mV = 760 mV. Therefore IIP3 of LNTA is not sensitive to the bias voltages and can tolerate large blockers up to 0 dBm.

The IIP3 obtained by the Volterra series model (42) and by SpectreRF™ simulations are depicted in Fig. 11 for two RF frequencies with the following parameters $g_{1n} = 30$ mS, $g_{1p} =$

13.6 mS, $g_{2n} = 57$ (mA/V²), $g_{2p} = 8.2$ (mA/V²), $g_{3n} = -70.3$ (mA/V³), $g_{3p} = -9.6$ (mA/V³), $r_{dn} = 339 \Omega$, $r_{dp} = 843 \Omega$ at $V_{DD} = 2.5$ V with $R_{so} = 50 \Omega$, $L_p = 30$ nH, $L_n = 70$ nH, $R_{sp} = 17.2 \Omega$, $R_{sn} = 110.8 \Omega$, $C_{gsn} = 30$ fF, $C_{gsp} = 20$ fF.

Figure 11. IIP3 comparison of analytical expression (42) and SpectreRF® simulation for LNTA, using two-tone 40 MHz spacing (transistor level).

Figure 12. Monte-Carlo simulation of LNTA IIP3 obtained with 50 iterations at $f_{RF} = 3$ GHz, 40 MHz spacing, $C_L = 1$ pF.

As shown, IIP3 is rising with the loading capacitance due to the reduced output voltage swing. For the same reason larger IIP3 values are attained at the higher operating frequency. It

In post-layout simulation with pad and bonding wire parasitics the IIP3 estimate at $f_{RF} = 3$ GHz with 40 MHz spacing is reduced by 4 dB, i.e. from 22 dBm at transistor level to 18 dBm for 2.5 V supply. The Monte-Carlo post-layout simulation under process variation with fixed bias is shown in Fig. 12. The mean value is 17.9 dBm while the standard variation is only 0.24 dB. To see the separate contributions to IIP3 by the different mechanisms used we found IIP3 to be reduced by 3 dB, down to 15 dBm, for supply voltage changed to the standard value, 1.2 V. The circuit will lose 6 dB more when the derivative superposition technique is excluded resulting in IIP3 = 9 dBm. Finally, by removing the resistive degeneration, IIP3 = 5 dBm is attained.

V. IMPLEMENTATION OF A SELECTIVE RECEIVER FRONT-END

With N-path filter as a load the LNTA noise figure is raised by approximately 1 dB that can be attributed to noise folding as devised in [7]. In effect, the two-stage front-end NF varies between 3.2 dB and 5.2 dB for frequencies between 500 MHz and 3 GHz, respectively. The NF at 2 GHz under 0 dBm blocker with 100 MHz offset is 12 dB that is below the 3GPP limit. Similarly, the in-band IIP3 is only less than 0 dBm due to large loading impedance (large voltage swing). On the contrary, the out-of-band IIP3 is as large as +20 dBm in the lower frequency range and +17 dB at 3GHz. Additionally, superior blocker rejection of 44 dB is attained for frequencies up to 2 GHz and 38 dB at 3 GHz owing to the two-stage filtering [7]. Measured S11 for different LO frequencies is shown in Fig. 16. Within the whole frequency range 0.5–3 GHz, S11 is below -10 dB in the bandwidth of interest.

TABLE II
PERFORMANCE COMPARISON

Author/ year	Architecture	CMOS process	NF (dB)	Av(dB)/Gm	IIP3 (dBm)	S11 (dB)	Power (mW)	BW (GHz)
H.M. Geddada [15] TMTT-14	LNTA	45 nm	3 min	-1.7 ^(a)	10.8 ^(a)	< -9	30.2	0.1 – 2
M. Mehrpoo [26] RFIC -13	LTNA	65 nm	5.9	100mS	20	< -10	11.3	0.8 – 2.2
L. Zhang [27] TCASII-15	LTNA	65 nm	6.2 min	242mS ^(*)	6.5	< -9	72	0.6 – 10.5 ^(*)
This work ^(**)	LNTA	65 nm	1.3 – 1.9	14^(b)	18	< -11	16.5	0.5 – 3
D. Murphy [4] JSCC-12	Front-end	40 nm	1.9/ (5.5–8) ^(c)	58	+13/15 ^(c)	< -8.8	50 – 100	0.8 – 2.9
A. Mirzaei [28] JSCC -11	Front-end	65 nm	5.3	55	-6.3	< -10	34.2	2.14
M. Darvishi [29] JSCC -13	Front-end	65 nm	2.8	25	+26	N/A	18-57	0.1 – 1.2
This work	Front-end	65 nm	3.2 – 5.3	45-25	20	< -9	46-113	0.5 – 3

^{a)} with (load) $Z_{RF} = 30 \Omega$, ^{b)} at 2GHz, $C_{load} = 0.2$ pF (80 Ω), ^(*) Simulation results, ^(**) Post-layout simulation with pad, bonding wire parasitics of 1nH and 2 Ω , ^(c) Noise Cancellation ON/Noise cancellation OFF.

V. CONCLUSIONS

In this paper we have presented LNTA design suitable for current-mode wideband front-end in CMOS technology. The amplifier architecture has been derived from the common gate circuit making use of complementary DS technique, which enables highly linear amplification. The tradeoff between the input matching and the transconductance of transistors (g_m) has been mitigated by resistive source degeneration. As a negative feedback it also supported the amplifier linearity. On the other hand, a suitable impedance mismatch at the input was useful to achieve a larger amplifier gain (G_m).

Superior noise performance has been attained by the double capacitive cross-coupling technique in a differential setup as proposed in this work. In effect, the LNTA compares favorably with the state-of-the-art designs both in terms of NF and linearity.

We have presented a complete NF analysis and Volterra series based IIP3 analysis of the amplifier. The obtained estimates were shown compliant with the circuit simulation results. The LNTA was implemented in 65 nm CMOS as a part of a tunable RF front-end using two-stage N-path filtering technique that provided blocker rejection competitive to SAW filters. Owing to the LNTA design the front-end linearity and noise performance have been placed well in line with the state-of-the-art.

APPENDIX A

DERIVATION OF THE VOLTERRA OPERATORS FOR THE PROPOSED LNTA: G1, G2 AND G3

For the circuit shown in Fig. 9 the respective currents and voltages can be expressed as

$$v_{sgp} = \frac{-n_p v_{in} - R_{sp}(i_{dp} - \frac{v_{outn}}{r_{dp}})}{m_p} \quad (A.1)$$

$$v_{gsn} = \frac{n_n v_{in} - R_{sn}(i_{dn} + \frac{v_{outn}}{r_{dn}})}{m_n} \quad (A.2)$$

$$v_{sp} = v_{sgp} + \frac{v_{in}}{2}, \quad v_{sn} = \frac{v_{in}}{2} - v_{gsn} \quad (A.3)$$

$$v_{outn} = k_{loadn}(i_{dp} - i_{dn} + \frac{v_{sp}}{r_{dp}} + \frac{v_{sn}}{r_{dn}}) \quad (A.4)$$

where

$$m_p = 1 + R_{sp}(C_{gsp}s + \frac{1}{r_{dp}}), \quad m_n = 1 + R_{sn}(C_{gsn}s + \frac{1}{r_{dn}}) \quad (A.5)$$

$$n_p = 1 + \frac{R_{sp}}{2r_{dp}}, \quad n_n = 1 + \frac{R_{sn}}{2r_{dn}} \quad (A.6)$$

$$k_p = \frac{g_{lp}R_{sp}}{m_p}, \quad k_n = \frac{g_{ln}R_{sn}}{m_n} \quad (A.7)$$

$$\hat{Z}_L = \frac{Z_L}{1 + Z_L(\frac{1}{r_{dp}} + \frac{1}{r_{dn}})} \quad (A.8)$$

Substituting (22, 23) into (A1, A2) with maximum 3rd order of v_{in} , we have

$$v_{sgp}^3 = \frac{B_p^3}{m_p^3(1+k_p)^3}, \quad v_{gsn}^3 = \frac{B_n^3}{m_n^3(1+k_n)^3} \quad (A.9)$$

$$v_{sgp}^2 = \frac{B_p^2}{m_p^2(1+k_p)^2} \left(1 - \frac{2R_{sp}g_{2p}B_p}{m_p^2(1+k_p)^2} \right) \quad (A.10)$$

$$v_{gsn}^2 = \frac{B_n^2}{m_n^2(1+k_n)^2} \left(1 - \frac{2R_{sn}g_{2n}B_n}{m_n^2(1+k_n)^2} \right) \quad (A.11)$$

$$v_{sgp} = \frac{1}{m_p(1+k_p)} \left\{ B_p - \frac{R_{sp}g_{2p}B_p^2}{m_p^2(1+k_p)^2} \left(1 - \frac{2R_{sp}g_{2p}B_p}{m_p^2(1+k_p)^2} \right) - \frac{R_{sp}g_{3p}B_p^3}{m_p^3(1+k_p)^3} \right\} \quad (A.12)$$

$$v_{gsn} = \frac{1}{m_n(1+k_n)} \left\{ B_n - \frac{R_{sn}g_{2n}B_n^2}{m_n^2(1+k_n)^2} \left(1 - \frac{2R_{sn}g_{2n}B_n}{m_n^2(1+k_n)^2} \right) - \frac{R_{sn}g_{3n}B_n^3}{m_n^3(1+k_n)^3} \right\} \quad (A.13)$$

where

$$B_p = -n_p v_{in} + \frac{R_{sp}}{r_{dp}} v_{out}, \quad B_n = n_n v_{in} - \frac{R_{sn}}{r_{dn}} v_{out} \quad (A.14)$$

Substituting (22, 23), (A3, A9-13) into (A4), we have

$$v_{outn} = \frac{\hat{Z}_L B_p (g_{1p} + \frac{1}{r_{dp}})}{(1+k_p)m_p} + \frac{\hat{Z}_L B_p^2}{m_p^2(1+k_p)^3} \left\{ g_{2p} \left(1 - \frac{2R_{sp}g_{2p}B_p}{m_p^2(1+k_p)^2} \right) + \frac{g_{3p}B_p}{m_p(1+k_p)} \right\} \quad (A.15)$$

$$- \frac{\hat{Z}_L B_n (g_{1n} + \frac{1}{r_{dn}})}{(1+k_n)m_n} - \frac{\hat{Z}_L B_n^2}{m_n^2(1+k_n)^3} \left\{ g_{2n} \left(1 - \frac{2R_{sn}g_{2n}B_n}{m_n^2(1+k_n)^2} \right) + \frac{g_{3n}B_n}{m_n(1+k_n)} \right\}$$

APPENDIX B

DERIVATION OF THE VOLTERRA OPERATORS FOR THE PROPOSED LNTA: A1, A2, A3, H1, H2 AND H3

For the circuit of Fig. 9 the current and voltage equations follow

$$v_{in} = v_{so} - 2R_{so}i_{so} \quad (A.16)$$

$$i_{so} = -sC_{gsp}v_{sgp1} + sC_{gsn}v_{gsn1} + v_{inp} \left(\frac{1}{sL_p} + \frac{1}{sL_n} \right) + i_{dp2} - i_{dn2} \\ + sC_{gsp}v_{sgp2} - sC_{gsn}v_{gsn2} + \frac{v_{sp2} - v_{outp}}{r_{dp}} - \frac{v_{outp} - v_{sn2}}{r_{dn}} \quad (A.17)$$

where

$$v_{sgp1} = v_{sgp}(v_{in}, v_{out}), \quad v_{sgp2} = v_{sgp}(-v_{in}, -v_{out}) \quad (A.18)$$

$$v_{gsn1} = v_{gsn}(v_{in}, v_{out}), \quad v_{gsn2} = v_{gsn}(-v_{in}, -v_{out}) \quad (A.19)$$

$$v_{sp2} = v_{sp}(-v_{in}, -v_{out}), \quad v_{sn2} = v_{sn}(-v_{in}, -v_{out}) \quad (A.20)$$

$$i_{dp2} = i_{dp}(-v_{in}, -v_{out}), \quad i_{dn2} = i_{dn}(-v_{in}, -v_{out}) \quad (A.21)$$

For differential mode, the single voltages should be

$$v_{inp} = -v_{inn} = \frac{v_{in}}{2}, \quad v_{outp} = -v_{outn} = \frac{v_{out}}{2} \quad (A.22)$$

REFERENCES

- [1] Z. Ru, et al. "Digitally enhanced software-defined radio receiver robust to out-of-band interference," *J. of Solid-State Circuits*, vol. 44, no. 12, December 2009.
- [2] C.Y. Yu, et al., "A SAW-Less GSM/GPRS/EDGE Receiver Embedded in 65-nm SoC," *IEEE J. Solid-State Circuits*, vol. 46, iss. 12, pp. 3047-4060, Dec. 2011.
- [3] A. Mirzaei, et al., "A 65 nm CMOS quad-band SAW-less receiver SoC for GSM/GPRS/EDGE," *IEEE J. Solid-State Circuits*, vol. 46, iss. 4, pp. 950-946, April 2011.
- [4] D. Murphy, H. Darabi, et al. "A blocker-tolerant, noise-cancelling receiver suitable for wideband wireless applications," *IEEE J. Solid-State Cir.*, vol. 47, no. 12, pp. 2943-2963, Dec. 2012.
- [5] J. Kim and J. Silva-Martinez, "Low-Power, Low-Cost CMOS Direct-Conversion Receiver Front-End for Multistandard Applications," *IEEE J. of Solid-State Circuits*, vol. 48, no. 9, pp. 2090-2103, 2013.
- [6] I. Fabiano t al., "SAW-Less Analog Front-End Receivers for TDD and FDD," *IEEE J. of Solid-State Circuits*, vol. 48, no.12, pp. 3067-3079, 2013.
- [7] F. Qazi, et al., "Two-stage highly selective receiver front-end based on impedance transformation filtering," *IEEE, Trans. on Circuit and Systems II*, vol. 62, no. 5, pp. 421-425, 2015.
- [8] L.E. Franks, and I.W. Sandberg, "An Alternative Approach to the Realization of Network Transfer Functions: The N-Path Filter," *Bell System Technical Journal*, vol. 39, no. 5, pp. 1321-1350, 1960.
- [9] H. Zhang and E.Sanchez-Sinencio "Linearization Techniques for CMOS Low Noise Amplifiers: A Tutorial," *Transactions on Circuit and Systems*, vol. 58, no. 1, pp.22-36, January 2011.
- [10] V. Aparin et al., "Linearization of CMOS LNAs via optimum gate biasing," *Proc. IEEE Int. Conf. Circuits and Systems*, pp. 748-751, 2004.
- [11] T.W. Kim, B. Kim, and K Lee, "Highly linear receiver front-end adopting MOSFET transconductance linearization by multiple gated transistors," *J. of Solid-State Circuits*, vol.39, No.1, pp. 223-229, 2004.
- [12] V. Aparin et al., "Modified derivative supposition method for linearizing FET low-noise amplifiers," *IEEE Trans. Microwave Theory Tech.*, vol. 53, no. 2, pp. 571-581, 2005.
- [13] D. Im, et al., "A wideband CMOS low noise Amplifier Employing Noise and IM2 distortion cancellation for a digital TV tuner," *J. of Solid-State Circuits*, vol. 44, no. 3, pp. 686-698, Mar. 2009.
- [14] W-H. Chen, et al., "A highly linear broadband CMOS LNA employing noise and distortion cancellation," *J. of Solid-State Circuits*, vol. 43, no. 5, May 2008.
- [15] H.M. Geddada, et al., "Wide-Band Inductorless Low-Noise Transconductance Amplifiers With High Large-Signal Linearity," *IEEE Trans. on Microwave Theory and Techniques*, vol. 62, no. 7, pp. 1495-1505, 2014.
- [16] N. Ahsan, et al., "Highly linear wideband low power current mode LNA," *Intl. Conf. on Systems and Electronic Systems, ICSES*, 4 pp. 2008.
- [17] Q-T. Duong and J. Dąbrowski, "Low noise transconductance amplifier design for continuous-time delta sigma wideband front-end," in *Europ. Conf. on Cir. Theory and Design. (ECCTD)*, pp. 825 - 828, 2011.
- [18] H. Zhang, et al., "A low-power, linearized, ultra-wideband LNA design technique," *J. of Solid-State Circuits*, vol. 44, no. 2, pp.320-330, Feb 2009.
- [19] W.Zhuo, et al., "Using capacitive cross-coupling technique in RF low noise amplifier and down-conversion mixer design," *European Solid-State Circuits Conference, ESSCIRC*, pp.77-80, 2000.
- [20] F. Bruccoleri, et al., "Wide-band CMOS low-noise amplifier exploiting thermal noise canceling," *J. of Solid-State Circuits*, vol. 39, no. 2, pp. 275-282, Feb. 2004.
- [21] M. Reiha and J. Long "A 1.2V Reactive-Feedback 3.1-10.6 GHz Low-Noise Amplifier in 0.13um CMOS," *J. of Solid State Circuits*, vol. 42, no. 5, pp. 1023-1033, May 2007.
- [22] A. Amer, et al., "A 90-nm Wideband Merged CMOS LNA and Mixer Exploiting noise cancellation," *J. of Solid-State Circuits*, vol. 42, no 2, December 2007.

- [23] S. Woo et al., "A 3.6mW differential common-gate CMOS LNA with positive-negative feedback," *IEEE International Solid-State Circuits Conference - Digest of Technical Papers, ISSCC*, pp. 218-219, 2009.
- [24] J. Kim et al., "Wideband Common-Gate CMOS LNA Employing Dual-Negative Feedback With Simultaneous Noise, Gain, and Bandwidth Optimization," *IEEE Trans. on Microwave Theory and Techniques*, vol. 58, no. 9, pp. 2340 – 2351, 2010.
- [25] S-C. Blaakmeer, et al., "Wideband balun-LNA with simultaneous output balancing, noise-canceling and distortion-canceling," *J. of Solid-State Circuits*, vol. 43, no. 6, pp. 1341–1350, June 2008.
- [26] M. Mehrpoo and R. B. Staszewski, "A Highly Selective LNTA Capable of Large-Signal Handling for RF Receiver Front-Ends," in *Proc. IEEE RFIC Symp.*, Jun. 2013, pp. 185–188, 2013.
- [27] L. Zhang, et al., "Analysis and Design of a 0.6-10.5GHz LNTA for Wideband Receivers," *Trans. On Circuits and Systems II, Express Briefs*, vol. 62, no. 5, pp. 431–435, May 2015.
- [28] A. Mirzaei, et al., "A low-power process-scalable super-heterodyne receiver with integrated high-Q filters," *J. of Solid-State Circuits*, vol. 46, no 12, pp. 2920–2932, 2011.
- [29] M. Darvishi, et al., "Design of Active N-Path Filters," *J. of Solid-State Circuits*, vol. 48, no 12, pp. 2962–2976, 2013.

Quoc-Tai Duong (S'10) received the B.Eng. degree in electrical and electronics engineering from Ho Chi Minh city University, Vietnam, in 2007, and the M.S. degree from Kyung Hee University, South Korea, in 2010. Since 2011, he has been pursuing the Ph.D. degree at Linköping University, Sweden. He has worked on power management for RFID, RF receiver front-ends as well as high-speed DACs. His current research interests include data

converters, mixed-signal/RF circuits, and power management.

Fahad Qazi (S'09 – M'15) received his B.S. degree in electrical engineering from COMSATS Institute of Information Technology, Pakistan in 2006. He received his M.S. and Ph.D. degrees in electronics (System on Chip) from Linköping University, Sweden in 2009 and 2015, respectively. Currently, he is with Catena Wireless Electronics AB, Stockholm, Sweden, employed as IC designer. Dr. Qazi's research interests include the design of multi-standard

flexible RF front-ends and $\Delta\Sigma$ modulators for A/D converters.

Jerzy J. Dąbrowski (M'03 – SM'12) received his Ph.D. and D.S. degrees in electronics from the Silesian University of Technology, Gliwice, Poland. Currently he is Associate Professor with Linköping University, Linköping, Sweden. His recent research interests are in design, modeling and testability of mixed-signal and RF ICs. Dr. Dąbrowski published over 100 research papers, one monograph, and two book chapters. He also holds 12 patents (as co-author) in switched-

mode power supplies and electronic instrumentation.

Figure 1. LNTA complementary DS architectures, a) common source
b) common gate.

Figure 4. Circuit schematic of proposed wideband LNTA.

Figure 2. Differential LNTA implementing DS and capacitive cross-coupling technique (simplified schematic).

Figure 3. S11 and linearity improvement by resistive source degeneration.

Figure 5. LNTA circuit for noise analysis.

Figure 6. NF comparison of analytical model (12-18) and SpectreRF® circuit simulation for proposed LNTA.

Figure 7. a) Schematic of conventional inverter, b) Simulation of third-order transconductances of PMOS g_{3p} , NMOS g_{3n} and output g_3 .

Figure 8. a) Schematic of resistive-feedback technique, b) Simulation of third-order transconductances of PMOS g_{3p} , NMOS g_{3n} and output g_3 with $W_p/L_p = 29\mu\text{m}/65\text{nm}$, $W_n/L_n = 48\mu\text{m}/65\text{nm}$.

Figure 9. Equivalent circuit of a proposed wideband LNTA.

Figure 10. The third-order voltage gain H_3 (41) versus the bias voltage V_{gsn} .

Figure 11. IIP3 comparison of analytical expression (42) and SpectreRF® simulation for LNTA, using two-tone 40 MHz spacing.

Figure 12. Monte-Carlo simulation of LNTA IIP3 obtained with 50 iterations at $f_{RF} = 3$ GHz, 40 MHz spacing, $C_L = 1$ pF.

Figure 13. Architecture of selective two-stage RF front-end.

Figure 14. Circuit schematic of LNTA2.

Figure 15. Chip photo [7].

Figure 16. Measured S_{11} around LO frequencies for $C_{BB} = 40$ pF.

TABLE I.
NF VERSUS (γ/α) COMPARISON OF (3) AND (21)

(γ/α)	2/3	1	1.5	2	2.5	3
$NF_{cross-coupling}$ (dB)	1.25	1.76	2.43	3.01	3.52	3.98
$NF_{proposed}$ (dB)	0.88	1.07	1.34	1.59	1.83	2.06
ΔNF (dB)	0.37	0.69	1.09	1.42	1.69	1.92

TABLE II
PERFORMANCE COMPARISON

Author/ year	Architecture	CMOS process	NF (dB)	Av(dB)/Gm	IIP3 (dBm)	S11 (dB)	Power (mW)	BW (GHz)
H.M. Geddada [15] TMTT-14	LNTA	45 nm	3 min	-1.7 ^(a)	10.8 ^(a)	< -9	30.2	0.1 – 2
M. Mehrpoo [26] RFIC -13	LTNA	65 nm	5.9	100mS	20	< -10	11.3	0.8 – 2.2
L. Zhang [27] TCASII-15	LTNA	65 nm	6.2 min	242mS ^(*)	6.5	< -9	72	0.6 – 10.5 ^(*)
This work ^(**)	LNTA	65 nm	1.3 – 1.9	14^(b)	18	< -11	16.5	0.5 – 3
D. Murphy [4] JSCC-12	Front-end	40 nm	1.9/ (5.5–8) ^(c)	58	+13/15 ^(c)	< -8.8	50 – 100	0.8 – 2.9
A. Mirzaei [28] JSCC -11	Front-end	65 nm	5.3	55	-6.3	< -10	34.2	2.14
M. Darvishi [29] JSCC -13	Front-end	65 nm	2.8	25	+26	N/A	18-57	0.1 – 1.2
This work	Front-end	65 nm	3.2 – 5.3	45-25	20	< -9	46-113	0.5 – 3

^{a)} with (load) $Z_{RF} = 30 \Omega$, ^{b)} at 2GHz, $C_{load} = 0.2$ pF (80 Ω), ^{*}) Simulation results, ^{**)} **Post-layout simulation with pad, bonding wire parasitics of 1nH and 2 Ω ,**
^(c) Noise Cancellation ON/Noise cancellation OFF.