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Tunable Selective Receiver Front-End with Impedance Transformation Filtering

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ABSTRACT

A highly selective impedance transformation filtering technique suitable for tunable selective RF receivers is proposed in this paper. To achieve blocker rejection comparable to SAW filters, we use a two stage architecture based on a low noise trans-conductance amplifier (LNTA). The filter rejection is captured by a linear periodically varying (LPV) model that includes band limitation by the LNTA output impedance and the related parasitic capacitances of the impedance transformation circuit. This model is also used to estimate "back folding" by interferers placed at harmonic frequencies. Discussed is also the effect of thermal noise folding and phase noise on the circuit noise figure. As a proof of concept a chip design of a tunable RF front-end using 65 nm CMOS technology is presented. In measurements the circuit achieves blocker rejection competitive to SAW filters with noise figure 3.2–5.2 dB, out of band IIP3 > +17 dBm and blocker P_{1dB} > +5 dBm over frequency range of 0.5—3 GHz.

KEY WORDS: SAW-less receiver; N-path filter; wideband selective RF front-end

1. INTRODUCTION

The idea behind the impedance transformation technique dates back to 1960's when the so-called *N*-path filter was first proposed [1]. Recently, a similarity between such a 4-path filter and a quadrature passive mixer with capacitive load has been noticed and investigated that also resulted in several implementations and models of tunable RF filters in CMOS technology [2]–[11]. In fact, it is the passive mixer transparency that enables simultaneous signal down- and up-conversion necessary in this case. With a low-pass impedance at baseband, the up-converted voltage signal appears band-limited accordingly that can be thought as impedance transformation in frequency from baseband to RF. Selectivity, achieved in this way, presents high Q factors which are attractive in RF filtering. In effect, filters designed using this technique are good candidates to replace inflexible SAW filters in modern wireless systems and, in particular, in software defined- or cognitive radio (SDR/CR). However, as the rejection of one such a filter is usually less than 20 dB, using another filter section or a more selective baseband impedance can be necessary in a SAW-less scenario to suppress interference and avoid significant intermodulation effects or gain compression. Resilience to out-of-band blockers, in extreme cases up to 0 dBm at antenna input, is the main challenge in this case while maintaining noise figure and intermodulation performance over the wide range of frequencies used in personal and data communication systems.

To attain a more selective baseband impedance, quadrature coupled g_m-C cells were proposed providing fourth and sixth order RF filtering that largely improves blocker rejection [13], [20]. However, the filter noise figure suffers, in particular due to 1/f noise of the g_m-C cells. To mitigate this problem the baseband circuit can be adopted to a low-IF scenario [16]. Interestingly, in this case also some image rejection can be achieved already at RF.

Lately, the impedance transformation technique has been supplemented by the noise cancelling technique [14]. This approach looks superior to the earlier work for breaking the trade-off between the blocker rejection and noise figure. However, the proposed circuit requires fine calibration that in practice can be difficult to attain.

In this paper we present a tunable receiver front-end with high blocker rejection achieved by two stage impedance transformation. The front-end design is based on a low noise transconductance amplifier (LNTA) [15] which is well suited to attenuate out-of-band blockers for a high ratio between its output impedance and on-resistance of switches used in the impedance transformation circuit. We discuss the filter gain and blocker rejection in terms of band limitation introduced by LNTA and parasitic capacitances of the filter circuitry. Using a linear periodically varying (LPV) model in the time domain, we arrive at a compact formula for gain which is compliant with SpectreRF® simulation and it is easier to use than [9, eq. 1]. Other models such as in [6]–[8] do

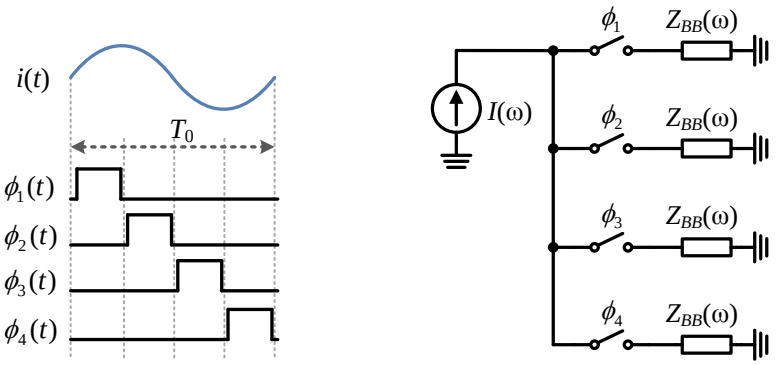


Figure 1. Model of impedance transformation based filter using 4-phase architecture.

not address this band limitation phenomenon even though it largely affects the filter performance.

We also present the effect of clock phase noise and by the derived model we show that the attained blocker rejection does not help to diminish the reciprocal mixing effect. The LNTA noise folding model showing the effect on the front-end noise figure is presented as well. The obtained estimates match well the simulation results.

Although the impedance-transformation filters using N-path structures can be discussed for an arbitrary N value, for the sake of clarity we limit our discussion to $N = 4$. Moreover, when addressing RF bands well above 1 GHz, using larger values of N is problematic from the practical point of view since an N-path filter necessitates N-phase non-overlapping clock, while its performance cannot be compromised. The minimum source clock frequency is $Nf_{RF}/2$ whereas the necessary duty factor is $1/N$ and should be well balanced over all clock phases.

We validate our discussion by chip design of a tunable selective RF front-end in 65 nm CMOS technology. In a two-stage architecture with a four-phase clock the blocker rejection competitive to SAW filters is attained with good noise figure and high IIP3 over a band of 0.5—3 GHz.

The paper is arranged as follows. In Section 2 we present the filter main mechanism and next, we derive estimates for the filter gain using LPV model including the inherent band limitation of the circuit. Also the "back folding" effect by interferers at odd harmonic frequencies is addressed. In Section 3 we discuss blocker rejection and demonstrate the effect of sizing the MOS switches. A support of blocker rejection by input impedance mismatch is also considered.

Section 4 provides thermal- and phase noise analysis of the circuit. In Section 5 implementation of a complete RF front-end in 65 nm CMOS technology is presented including experimental results. Conclusions are formulated in the last section.

2. FILTER CHARACTERIZATION

2.1. Filter mechanism

Using the model shown in Figure 1 the effect of impedance up-conversion resulting in a tunable narrowband selectivity achieved at RF can be demonstrated [5]. Assuming $Z_{BB}(\omega)$ to be low-pass and ignoring all higher harmonics the impedance seen by the source around the local oscillator frequency can be expressed by

$$Z_{in}(\omega) \cong R_{sw} + a_1^2\left[Z_{BB}(\omega+\omega_0) + Z_{BB}(\omega-\omega_0)\right] \tag{1}$$

where R_{sw} is the on-resistance of the switches, ω_0 is the angle frequency of the switching clock and $a_1 = \sqrt{2}/\pi$. In practice, the up-converted term is of interest and for a capacitive load $Z_{BB}(\omega) = 1/(j\omega C_{BB})$ from (1) we find

$$Z_{in}(\omega) \cong R_{SW} + \frac{a_1^2}{j(\omega-\omega_0)C_{BB}}, \quad (\omega \approx \omega_0) \tag{2}$$

This up-converted impedance can serve signal amplification in vicinity of the clock frequency ω_0. Ideally, in this model the corresponding RF voltage goes to infinity as $Z_{in}(\omega_0) \to \infty$, but in practice it is limited by a finite output impedance of the source. Including the source impedance modeled as ($R_{out} \parallel C_{out}$) the filter bandwidth for

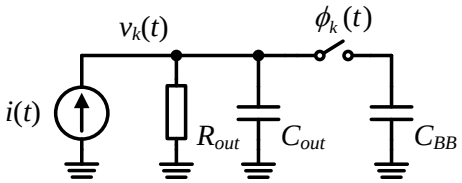


Figure 2. Model of multi-phase capacitance up-conversion circuit in *k*-th phase of clock.

$C_{BB} >> C_{out}$ can be estimated from [9]

$$BW_{-3\text{dB}} \cong \frac{1}{4\pi R_{out} C_{BB}} \quad [\text{Hz}] \tag{3}$$

In this way a very large Q-factor of the filter can be easily attained. On the other hand, a low value of $Z_{in}(\omega)$ at offset frequencies $(\omega - \omega_0)$ supports attenuation of interference provided the resistance of the used switches is small. In this case, also the useful offset range is limited by the "comb" characteristics of $Z_{in}(\omega)$ which tends to peak at odd harmonic frequencies of the clock. Still it is also limited by the source impedance in parallel.

2.2. Filter gain

For the received signal close to the clock frequency ω_0 the filter gain can be estimated using a linear periodically varying (LPV) model as shown in Figure 2 for one of the phases of the non-overlapping 4-phase clock with 25% duty cycle. We assume the source output impedance as $(R_{out} \parallel C_{out})$ and $R_{sw} << R_{out}$. For a sinusoidal input signal at clock frequency ω_0 and switching function $\phi_k(t) = 1$ ($k = 1,\ldots 4$), the voltage at the source can be found as a superposition of the steady-state and transient response

$$v_k(t) = \frac{A\sin(\omega_0 t + (k-1)\pi/2 - \varphi)}{\sqrt{1+(\omega_0 T)^2}} + \Delta V_k \exp\frac{-t}{T} \tag{4}$$

where $A = I_0 R_{out}$ with I_0 as an amplitude of the sinusoidal source current $i(t)$, whereas $T = R_{out}(C_{out} + C_{BB})$ and $\varphi = \tan^{-1}(\omega_0 T)$. Importantly, the charge on capacitor C_{out} from (k-1)-th phase (incident with path k-1) is shared with C_{BB} capacitor in path k (of k-th clock phase) that results in band limitation of the filter.

By careful time-domain analysis as we devise in Appendix-A, the signal gain in the 4-path architecture at the clock frequency ω_0 can be calculated as

$$K_{sig}(\omega) \cong g_m R_{out} \times \frac{8(1-m)}{\pi^2(1+jm)}, \quad \omega \cong \omega_0 \tag{5}$$

where g_m is the amplifier transconductance and m reflects band limitation by the source impedance $(R_{out} \parallel C_{out})$ and is defined as

$$m = \frac{\omega_0 R_{out} C_{out}}{\omega_0 R_{out} C_{out} + \pi/2} \tag{6}$$

As seen C_{BB} has no effect on the filter gain (5) while we assume $C_{BB} >> C_{out}$ and also $\omega_0 T >> 1$. When the band limitation is omitted, assuming $C_{out} \to 0$ ($m \to 0$), (5) presents the result reported also in the previous work [8],[9]. The dependence of filter gain (5) on the clock frequency for different values of C_{out} is illustrated in Figure 3 and is compliant with the simulation results (shown by dots) where ideal switches with low on-resistance are used ($R_{sw} \approx 0$). On the other hand, the characteristics obtained with the model presented in [9, eq. 1] while accurate for $R_{sw} > 0$, for $R_{sw} = 0$ tend to overestimate the filter gain by up to 4 dB.

Knowing the front-end gain (5) also the input impedance of the up-conversion circuit can be found as

$$Z_{in}(\omega) = Z_{out}(\omega) \times \frac{8(1-m)}{\pi^2(1+jm) - 8(1-m)}, \quad \omega \cong \omega_0 \tag{7}$$

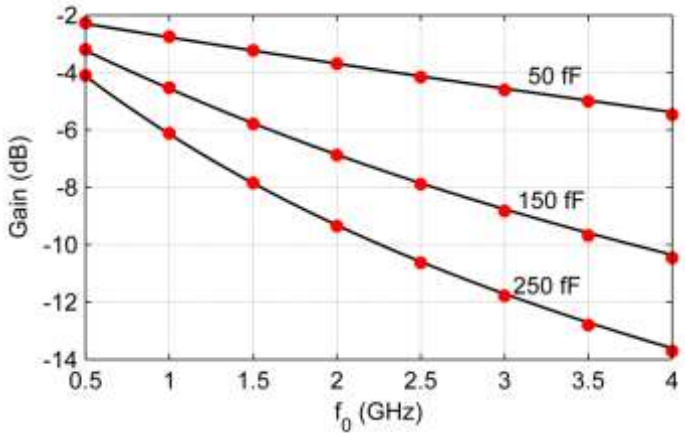


Figure 3. Normalized filter gain vs clock frequency for R_{out} = 550 Ω and C_{BB} >> C_{out}. and $R_{sw} \approx 0$. Model of this work (solid line) superimposed on SpectreRF® simulation (dots).

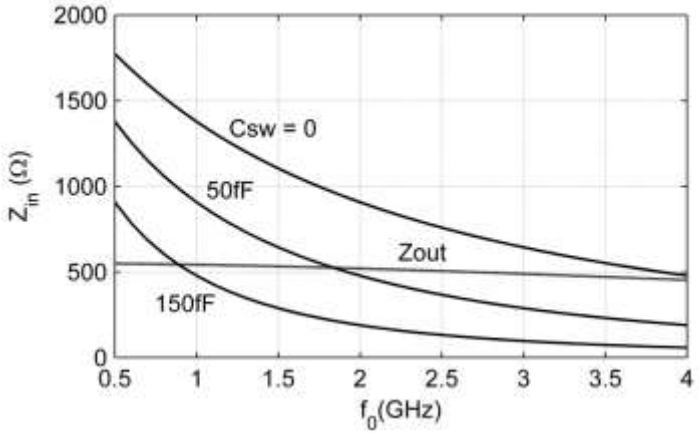


Figure 4. Input impedance of 4-path filter vs clock frequency for different parasitic capacitances of switches.

For $C_{out} \to 0$, also $m \to 0$ and $Z_{out}(\omega) \to R_{out}$ showing (7) to be $8R_{out}/(\pi^2-8)$ as also reported in [8]. Figure 4 shows the impedance $|Z_{in}(f_0)|$ for different capacitance values added by the circuit switches. The LNTA output impedance is also plotted for comparison. Its inherent capacitance and resistance are assumed 50 fF and 550 Ω, respectively that means C_{out} = 50 fF + C_{sw}. The plots show the input impedance value to drop below the output impedance of LNTA at higher frequencies that also reflects the change in the filter gain shown in Figure 3.

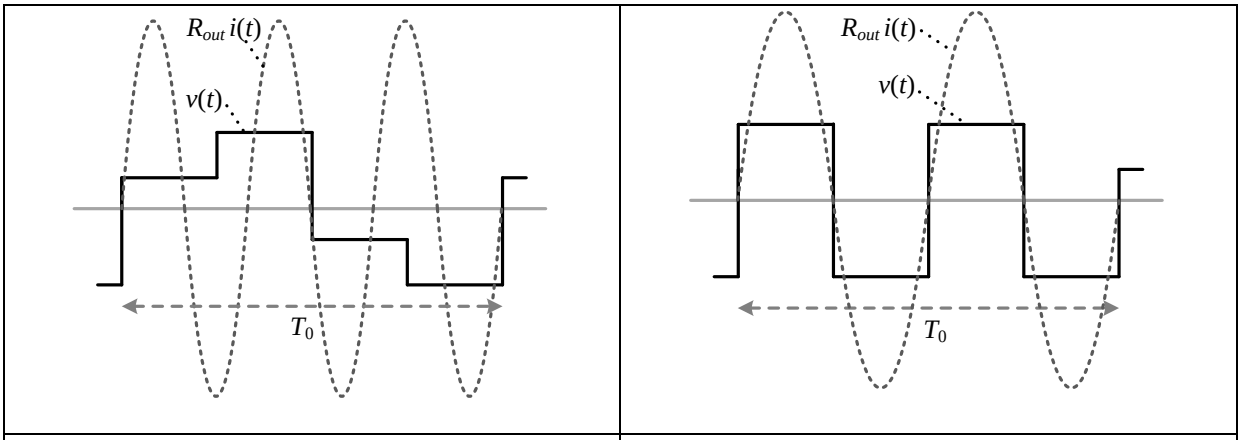
For the input tone at a harmonic frequency $n\omega_0$ the same LPV model can be used. In this case the RF voltage in the k-th clock phase (k = 1, .. 4) can be expressed as

$$v_k(t) = \frac{A\sin\left(n\omega_0 t + (k-1)n\pi/2 - \varphi\right)}{\sqrt{1+(n\omega_0 T)^2}} + \Delta V_k \exp\frac{-t}{T} \tag{8}$$

It can be proven that for an odd n value the corresponding output waveform is proportional to $v(t)$ with a factor $1/n$, where $v(t)$ is obtained for input at ω_0 as derived in Appendix A. It means there is "back folding" from frequencies around harmonics $n\omega_0$ to the desired band around ω_0 [8] and the corresponding voltage gain is $|K_{sig}(\omega_0)|/n$ (n = 3, 5, 7, …).

However, for even values of n the output appears as a regular square wave at frequency $n\omega_0$ (not at ω_0) so there is no back folding in this case as also illustrated in Figure 5 for n = 2. In other words for odd n the waveform period is T_0 whereas for even n it is T_0/n. On the other hand, the even values of n are of less interest since the filter is typically designed as a differential circuit cancelling thereby the respective spectral components.

We notice that the back folding in the N-path filter is similar to signal down-conversion achieved with a sub-sampling mixer. The latter picks up signals from frequencies around $n\omega_0$ for both odd and even values of n.



(*a*) (*b*)

Figure 5. Voltage waveforms in 4-path filter for input tones at (a) 3rd harmonic (b) 2nd harmonic frequency of clock $f_0 = 1/T_0$

Unlike the *N*-path filter, it usually requires the sampled voltage to settle when the switch is on (to avoid distortion). On the other hand, the *N*-path filter performance tends to suffer from clock overlapping or too low duty cycle [8] that, in practice at GHz frequencies, is difficult to be completely evaded. Hence, sub-harmonic clocking of the *N*-path filter can be considered an option similar to sub-sampling useful in some applications.

Additionally, we find that the amplitude of the odd harmonics of $v(t)$ is proportional to the fundamental with a factor $1/n$ so the voltage gain

$$\left|K(n\omega_0)\right| = \frac{\left|K_{sig}(\omega_0)\right|}{n^2} \tag{9}$$

which, in fact, gives gain values at odd numbered peaks of this RF "comb filter". In practice, it means the gain for an interferer at $n\omega_0$ is by $40\log n$ [dB] less than for the signal at ω_0 (i.e. 19 dB for $n = 3$ and 28 dB for $n = 5$) that is also compliant with the result reported in [8]. The complete frequency response of the filter obtained by simulation for different values of switch resistance is depicted in Figure 6. In fact, the maximum gain of the filter is attained at a frequency slightly lower than f_0 and this shift depends mostly on the C_{out}/C_{BB} ratio [20].

3. BLOCKER REJECTION

3.1. Gain for blockers

One possible solution to achieve blocker rejection is using a current mode front-end where LNA is a transconductance amplifier (LNTA) followed by a passive multi-phase mixer which in this case serves also capacitance up-conversion. While the LNTA output impedance is high the up-conversion circuit offers a low impedance load at offset frequencies (out of band) that makes the front-end gain for blockers low. The low gain is also useful in terms of the front-end linearity. The LNTA voltage gain for out-of-band blockers is proportional to the output impedance of the amplifier in parallel with the on-resistance of the switches, while the up-converted baseband impedance approaches zero

$$K_{bl}(\omega_0 + \Delta\omega) = g_m\left(R_{sw} \| Z_{out}(\omega_0 + \Delta\omega)\right), \quad |\Delta\omega| >> 0 \tag{10}$$

where g_m is the transconductance of LNTA. Clearly, a possibly low switch resistance is of interest in this case. By defining the blocker rejection around ω_0 as $\eta(\omega_0+\Delta\omega) = \left| K_{bl}(\omega_0+\Delta\omega)/K_{sig}(\omega_0) \right|$ where $|\Delta\omega| >> 0$ except for the area around odd harmonic frequencies at $n\omega_0$, using (10) we have

$$\eta(\omega_0 + \Delta\omega) = \frac{g_m R_{out}}{\left|K_{sig}(\omega_0)\right| \times \sqrt{\left(1 + \frac{R_{out}}{R_{sw}}\right)^2 + \left((\omega_0 + \Delta\omega)C_{out}R\right)^2}} \tag{11}$$

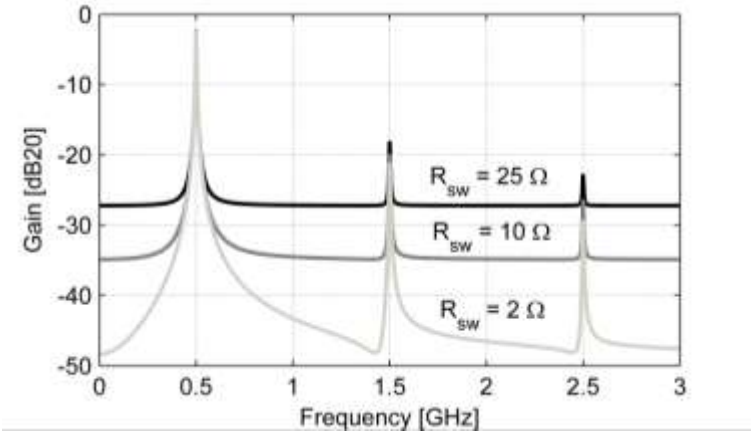


Figure 6. Complete frequency response of differential 4-path filter for f_0 = 0.5 GHz and different R_{sw} values.

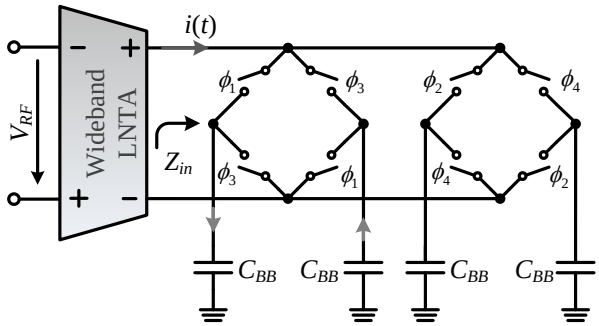


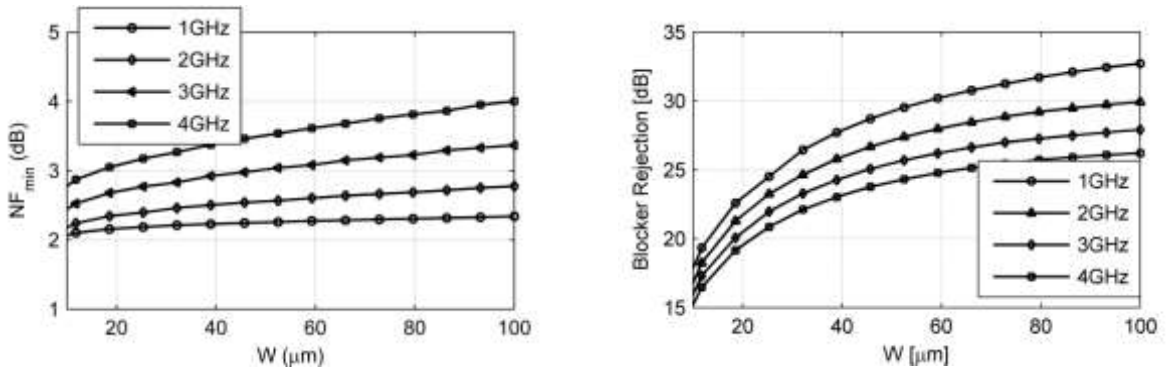
Figure 7. Receiver front-end implementing baseband capacitance up-conversion technique in differential architecture.

where $R = R_{out} \parallel R_{sw}$. For typical values of R_{sw} and C_{out} (11) can be simplified to

$$\eta(\omega_0 + \Delta\omega) \cong \frac{g_m R_{out}}{\left|K_{sig}(\omega_0)\right|} \times \frac{R_{sw}}{R_{out}} \tag{12}$$

where the first term can be recognized as an inverse of the normalized filter gain. This model shows the rejection to change with clock frequency according to the signal gain. For example, if the filter with C_{out} = 150 fF can provide a rejection of -30 dB at 1 GHz then it will drop to -24 dB at 4 GHz according to the gain reduction (Figure 3).

An experimental front-end composed of a trans-conductance low noise amplifier (LNTA) [15] and a tunable 4-path filter that is also used as a quadrature mixer (Figure 7), shows the design tradeoffs in terms of size of the MOS switches. The circuit is designed in 65 nm CMOS. Large size of switches only slightly improves the filter rejection since C_{out}.is elevated and K_{sig} decreases accordingly. As a result the front-end NF is degraded too as illustrated in Figure 8.



(*a*) (*b*)

Figure 8. (*a*) Simulated NF and (*b*) Rejection of receiver front-end vs. size of filter switches.

Importantly, not only a high blocker rejection is of interest, but also the respective gain for blockers. This demand appears critical for blockers with maximum power, i.e. up to 0dBm (632 mV_{pp}) which should be tolerated without gain compression. For this purpose the gain for blockers should be less than 0 dB ($K_{bl} < 1$) that also puts a constraint on the signal gain

$$K_{sig}(\omega_0) < 1/\eta(\omega_0 + \Delta\omega) \tag{13}$$

Clearly, this condition is in line with the demands placed on the receiver linearity. Additionally, also the voltage headroom for the transistors of LNTA must be increased that can be achieved by elevating the supply voltage. A dedicated start-up /shut-down circuit is designed which keeps all the terminal voltages within the safe limit of 1.2V while V_{DD} for LNTA is elevated to 2.5V.

3.2. Effect of input impedance mismatch

The resilience to blockers can also be supported by intentional impedance mismatch at the LNTA input. In practice, a mismatch effect is inevitable and usually it is considered harmful. However, when the front-end input impedance tends to be less than the antenna matching impedance a limited mismatch can be beneficial. To see this, we can express the front-end input voltage in terms of a reflection coefficient Γ using the formula

$$V_{in} = (1+\Gamma)V_{match} \tag{14}$$

where V_{match} is the input voltage under perfect matching conditions. In order to achieve $|V_{in}| < |V_{match}|$, from (14) we can find

$$\mathrm{Re}\Gamma < -|\Gamma|^2/2 \tag{15}$$

that is illustrated by the dashed area in Figure 9. For all these points on the Smith chart the normalized input resistance R < 1 (outside the blue circle) while X can vary accordingly. For example, for a return loss equal -10 dB we have $|\Gamma|^2 = 0.1$ (red line in Figure 9). Then provided Im Γ << Re Γ the attenuation for the input voltage can be as low as

$$|1+\Gamma|_{\min} = \sqrt{1+|\Gamma|^2 + 2(\mathrm{Re}\Gamma)_{\min}} = \sqrt{1.1 - 2\cdot 0.316} = 0.684$$

that largely prevents blockers from overloading the receiver front-end even though only 10% of the available signal power is lost. In this case the corresponding normalized resistance, R ≈ 0.52. On the contrary for $(\mathrm{Re}\,\Gamma)_{mx}$ the input voltage can be as high as 1.316 V_{match}, with R ≈ 1.92 that exacerbates the blocker problem.

The input matching useful to tolerate blockers in our LNTA has been achieved with CG stage where g_m > 1/50Ω was of interest resulting in R_{in} < 50Ω. The necessary correction of the input resistance was obtained by resistive source degeneration that also allowed to tune the Γ value ($S11$). Importantly this mechanism provides extra means to tolerate blockers in excess of 0 dBm that is difficult to overestimate in this application.

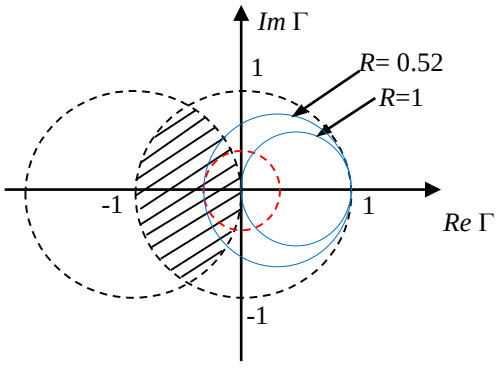


Figure 9. Reflection coefficients reducing input voltage (dashed area).

4. NOISE FIGURE ANALYSIS

The selectivity and blocker rejection come at a price of increased noise figure. To discuss this effect we consider injection of the LNTA noise into the filter and also the reciprocal mixing due to phase noise of the 4-phase clock.

4.1. Noise injection

To capture the front-end noise model we consider the LNTA equivalent loading impedance equal to $Z_{in}(\omega_0)$ as defined by (7) for which the amplifier noise factor is

$$F = 1 + \frac{I_n^2}{g_m^2 V_{ref}^2} \tag{16}$$

where g_m and I_n^2 is the LNTA transconductance and the output-referred inherent noise, respectively. When $Z_{in}(\omega_0)$ is replaced by the 4-path filter the amplifier wideband noise is subject to folding by higher harmonics, achieving in this way a larger gain compared to the signal. This mechanism is different from noise aliasing in a typical SC circuit since in this case the equivalent noise bandwidth [17] is less than the switching frequency. As discussed in Sec. II only the interferers at odd harmonic frequencies contribute to the signal band (at fundamental frequency ω_0). As the respective gain values in the 4-path filter are $\left|K_{sig}(\omega_0)\right|/n$ so the noise folding at the LNTA output can be described by

$$e_n^2 = \left(I_n^2 / g_m^2\right) \times \left|K_{sig}(\omega_0)\right|^2 \sum_{k=1}^{+\infty} \frac{1}{(2k-1)^2} \tag{17}$$

where we neglect the noise contribution of the switches assuming $R_{sw} << R_{out}$. The reference noise undergoes folding in the same way

$$e_{n,ref}^2 = V_{ref}^2 \times \left|K_{sig}(\omega_0)\right|^2 \sum_{k=1}^{+\infty} \frac{1}{(2k-1)^2} \tag{18}$$

Hence, the noise factor can be calculated as

$$F = \frac{e_{n,ref}^2 + e_n^2}{\left|K_{sig}(\omega_0)\right|^2 V_{ref}^2} \tag{19}$$

Using the identity $\sum_{k=1}^{+\infty} \frac{1}{(2k-1)^2} = \frac{\pi^2}{8}$ we rewrite (19) as

$$F = \frac{\pi^2}{8} \times \left(1 + \frac{I_n^2}{g_m^2 V_{ref}^2}\right) \tag{20}$$

As compared to (16) the noise factor (20) is increased $\pi^2/8$ times (0.91 dB) that is a good prediction of the simulation results. For verification we picked up $Z_{in}(\omega_0)$ from simulation since it largely depends on the LNTA output impedance as devised by (7). Next, we synthesized $Z_{in}(\omega_0)$ by RC elements and resimulated the LNTA with such a load that was free from noise folding. As compared to the actual filter the noise figure for different cases was reduced by 1 – 1.1 dB that is close to the prediction shown above.

4.2. Phase noise

To analyze the phase noise effect, first, we use the filter model shown in Figure 1 [9]. In this case, phase noise (or jitter) can be captured in the time domain as a difference between the noisy- and noiseless switching function incident with *k*-th filter branch

$$\varepsilon_k(t) = \phi_k^*(t) - \phi_k(t) \tag{21}$$

As both edges of the clock are affected by the phase noise, $\varepsilon_k(t)$ is a waveform composed of two narrow pulses per period with random widths and amplitudes +1 or −1. The corresponding current noise is a product of $\varepsilon_k(t)$ and a blocker represented by the current $g_m A_{bl} \cos(\omega_{bl} t)$. Then the related spectral density of voltage noise at baseband can be found from

$$S_{BBk}(\omega) = \frac{g_m^2 A_{bl}^2 |Z_{BB}(\omega)|^2}{4} \left(S_k(\omega - \omega_{bl}) + S_k(\omega + \omega_{bl}) \right) \tag{22}$$

where $S_k(\omega)$ is the PSD of $\varepsilon_k(t)$. If $S_k(\omega)$ is approximately flat around ω_{bl} then (22) can be simplified to

$$S_{BBk}(\omega) \approx \frac{g_m^2 A_{bl}^2 |Z_{BB}(\omega)|^2}{2} S_k(\omega_{bl}) \tag{23}$$

This baseband noise is band limited by $Z_{BB}(\omega)$ so the corresponding noise at RF (i.e. up-converted to ω_0) is due to the first harmonic of the switching function $\phi_k(t)$

$$S_{RFk}(\omega) \approx \frac{a_1^2 g_m^2 A_{bl}^2 S_k(\omega_{bl})}{4} |Z_{BB}(\omega - \omega_0)|^2 \tag{24}$$

Assuming noise from the other branches (clock phases) to be uncorrelated we find the total noise PSD at RF as $S_{RF}(\omega) = 4S_{RFk}(\omega)$. Importantly, this result shows that the reciprocal mixing product (24) does not depend on the blocker rejection if $S_k(\omega_{bl})$ is constant for the respective ω_{bl} frequencies that has also been verified by simulation. For a 0dBV blocker, LNTA model with R_{out} = 550Ω, g_m = 14.5mS (unloaded gain = 18 dB) and edge-to-edge clock jitter with flat PSD defined in Verilog-A the noise PSD was captured at the filter output showing no effect of the offset frequency which was varied from 10 MHz to 200 MHz. However, a significant noise reduction was observed due to C_{out} as shown in Figure 10 for two values of clock jitter.

For illustration let us consider the reciprocal mixing noise at $(\omega_{bl} - \omega_0)$ to be −165 dBV/Hz. If we assume the filter signal gain of 13 dB, NF = 3 dB (F = 2), and the reference noise -174 dBm/Hz (-187 dBV/Hz), then the inherent output referred noise is -187 dBV/Hz + 13 dB = -174 dBV/Hz that is 9dB below the reciprocal mixing component.

This means the phase noise will raise the inherent noise ×(1+8) and accordingly the noise factor from 2 to 10 (NF = 10 dB). For the blocker power reduced by 3 dB the corresponding noise factor would be F = 6 (NF = 7.8 dB).

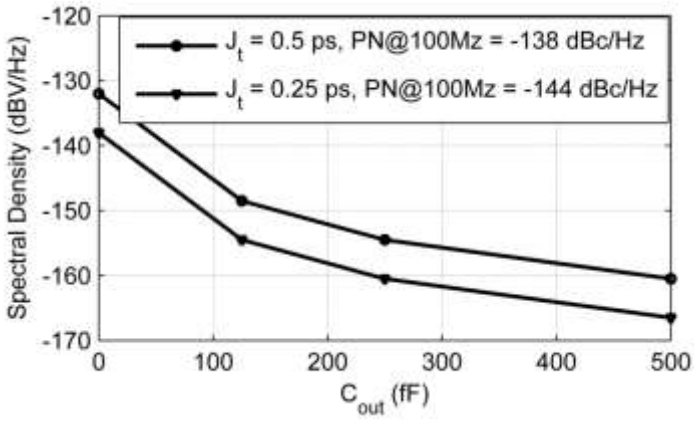


Figure10: Noise PSD at the output of 4-path single ended filter for 0dBV blocker and 18 dB unloaded gain.

5. IMPLEMENTATION

To tolerate large blockers the rejection provided by one impedance transformation filter is usually insufficient. One solution to this problem is an extra *N*-path circuit embedded into the LNA [10], [11]. However, in this architecture the rejection cannot be improved much because of loading effects in the LNA circuit.

To meet rejection typical of SAW filters we propose a two-stage architecture where separation between the stages is achieved by a high input impedance buffer incorporated in the second LNTA (Figure 11). The circuit is differential and designed in 65 nm CMOS. In this architecture the second stage also serves IQ down-conversion while the first stage helps to relax the requirements placed on linearity (IIP2) of the down-converter and on phase noise of the clock. It should be noted that an extra attenuation of the blocker by β dB results in reduction of the reciprocal mixing noise by β dB and of the intermodulation product (IM2) by 2β dB. However, if the received signal is strong, rejection by the first stage can be sufficient so the second stage can be disabled (to save power) while the first stage can be used for down-conversion as well.

Importantly, each LNTA stage provides attenuation rather than gain for blockers (at offset frequencies). Hence, the blockers can be well tolerated by the receiver chain and the out-of-band linearity (IIP2/IIP3) of the receiver is largely improved in the intermodulation tests. Also the demands for the baseband filter and the dynamic range of the following A/D converter are mitigated.

In Appendix-B we show that for the two stage filter its IIP3 can be estimated from

$$\frac{1}{P_{IIP3}} = \frac{1}{P_{IIP31}} + \frac{G_{B1}\eta_1}{P_{IIP32}} \tag{25}$$

The advantage provided both by the blocker attenuation and rejection of the first stage (with low $G_{B1}\eta_1$) is evident. In practice, this mechanism allows to eliminate the IP3 contribution of the second stage.

5.1. LNTAs

Like for any receiver the performance of the RF amplifier is critical in this design. The amplifier makes use of the derivative superposition technique, transistor source degeneration, and capacitive cross-coupling to achieve both high linearity and low noise figure over a wide frequency range. The tradeoff between NF and S11 (large size of transistors makes the input impedance low) is mitigated by using the source degeneration resistors R_S. Off-chip inductors of 50 nH each are large enough to guarantee S11 < -10 dB also at frequencies below 1 GHz. Similarly, the coupling capacitances are chosen C_S > 10 pF to avoid reduction of LNTA gain. Four of them (connected to transistor gates) are integrated at the expense of the silicon area overhead. The sizes of the MOS transistors M_n, M_p are chosen to attain the best possible third-order g_m cancellation. For a purely capacitive load the LNTA achieves NF < 1.4 dB and IIP3 > 12 dBm over the range of 0.8 – 5 GHz [15].

Although the first front-end stage is selective and provides attenuation at the offset frequencies, the gain of LNTA1 can be compressed by large blockers due to the limited voltage headroom available with 65 nm devices. To cope with this problem and tolerate blockers up to 0 dBm (632 mV_{pp}) we have used elevated supply voltage of 2.5 V for LNTA1 (Figure 12). Still 1.2 V devices have been used to take advantage of their lower threshold voltage compared to 2.5 V devices available in this technology as well. Since voltage stress could result in low reliability or damage of the devices, in this case, all bias voltages were applied to LNTA1 trough an off-chip high-RC time constant circuit, shown in Figure 13. During startup or shutdown the circuit keeps the bias and terminal voltages within safe limits for 1.2V devices as illustrated in Figure 14.

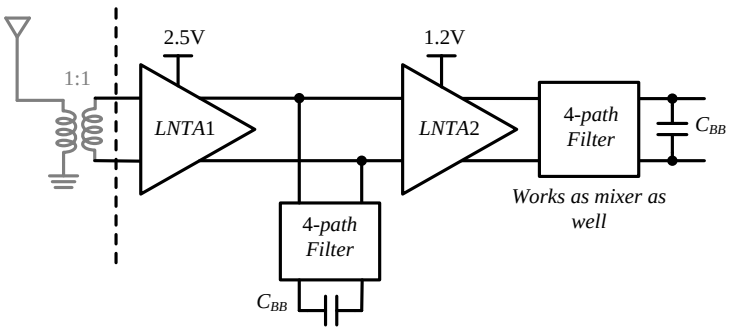


Figure 11. Architecture of selective two-stage RF front-end

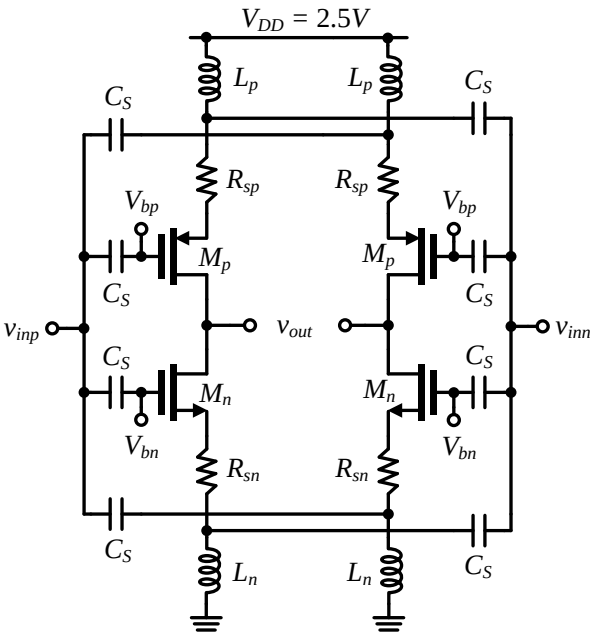


Figure 12. LNTA1 schematic.

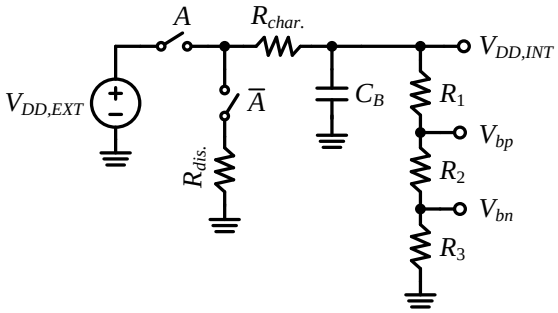
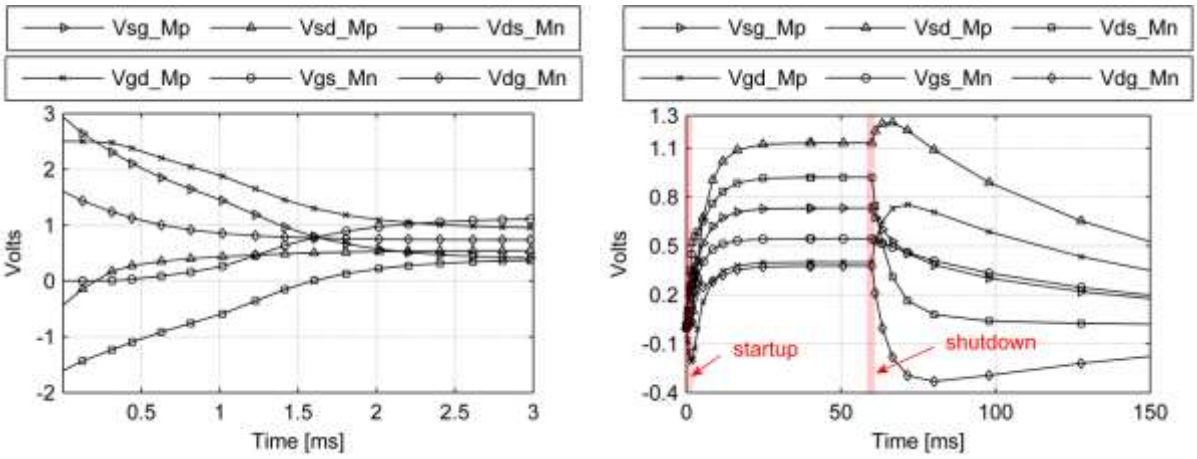


Figure 13. Startup circuitry for LNTA1.



(*a*) (*b*)

Figure 14.Terminal voltages of LNTA 1 (*a*) Without startup circuitry. (*b*) With startup circuitry.

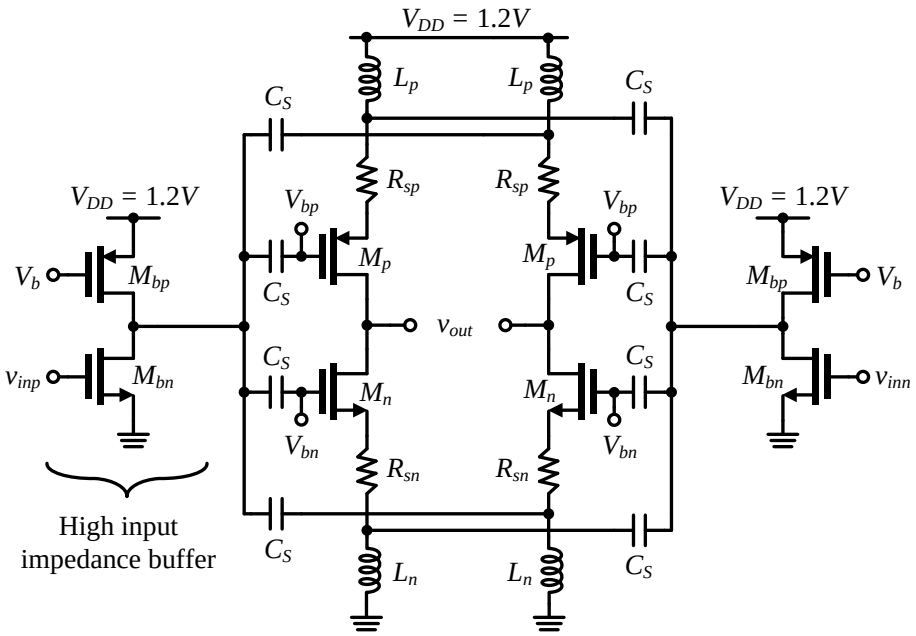


Figure 15. LNTA2 schematic.

The amplifier in the second stage, LNTA2 (Figure 15), also makes use of the same circuit architecture as LNTA1. However, to prevent loading of the first stage a simple CMOS buffer is placed in front of LNTA2 (otherwise the filter transfer function could be degraded). Taking advantage of blocker rejection by the first stage this circuit operates with standard 1.2V supply and in this way it saves power.

The front-end blocks are coupled by 5pF MIM capacitors which provide significant parasitic capacitances from their bottom plate to ground. These capacitances increase the capacitance C_{out} (discussed in Sec. II-B) which limits the amplifier gain at higher frequencies and thereby degrades the NF. On the other hand, reducing of the coupling capacitances leads to higher reactance values that add to the on-resistances of switches. As a result the attenuation of blockers at offset frequencies is deteriorated, especially in the lower frequency range.

5.2. Impedance transformation circuit

As already discussed, switches with a very large aspect ratio must be avoided to prevent gain and noise figure degradation. In this design the width of switches was chosen 60 μm and to mitigate the tradeoff between the performance possible to attain in lower and higher frequency bands, increased overdrive voltage was used. This has been obtained by reducing the source/drain bias of the transistor switches below $V_{DD}/2$ rather than raising the gate voltage beyond V_{dd} that creates reliability issues. Specifically, if we acknowledge $R_{sw} \propto (V_{GS} - V_T)^{-1}$ and the rejection for the out-of-band blockers to be $\eta(\omega_0+\Delta\omega) \propto R_{sw}$, then with overdrive increase of ΔV the rejection can be improved by

$$\Delta\eta(\omega_0 + \Delta\omega) = -20\log\left(1 + \frac{\Delta V}{V_{GS} - V_T}\right) \tag{26}$$

For NMOS 65 nm devices with V_{GS} = 0.6V, V_T = 0.3V and ΔV = 0.2V ideally results in $\Delta\eta$ = – 4.4dB.

To program the front-end bandwidth the baseband capacitors in both stages have been designed as small capacitor banks providing C_{BB} = 10, 20, 40 pF. As a result the bandwidth can be programmed in the range of 2 – 12 MHz. at 0.5GHz LO frequency and from 6 – 40 MHz at 3GHz LO frequency due to filter Q reduction. When narrower than standard bandwidth, the programmed BW also allows attenuating in-band blockers that need to be tolerated by receivers with fixed band-select filters at the expense of high demands for linearity. In particular, the demands for very high IIP2 in zero-IF or low-IF receivers render precise on-chip calibration circuits indispensable that is largely mitigated in the presented solution.

5.3. Clock Generation

The filter characteristics are sensitive to the clock duty cycle that ideally should be 25%. Clock overlapping must be avoided as it can result in complete destruction of the filter shape. On the other hand the non-zero rise and fall times of the clock make the effective duty cycle less than 25%. In effect, the filter input impedance is increased [8] that is critical at large offset frequencies where, ideally, it should be R_{sw}. This limits the attenuation for blockers and results in lower filter rejection in a practical circuit.

For the design of 4-phase clock generator we have adopted a high speed dual edge dynamic flip-flop [18] shown in Figure 16(a). By employing this flip flop in divide-by-4 circuit (Figure 16(b)) only a twice of the required output clock frequency is necessary to generate the 25% duty cycle clock. For example in order to achieve a 3GHz 25% duty cycle clock, a 6 GHz external signal need to be interfaced with the chip instead of 12 GHz as typically required. This largely reduces the hassle of handling very high frequency signaling. Furthermore power consumption is approximately halved as compared to traditional approach. The complete 4-phase clock generator is presented in Figure 17.

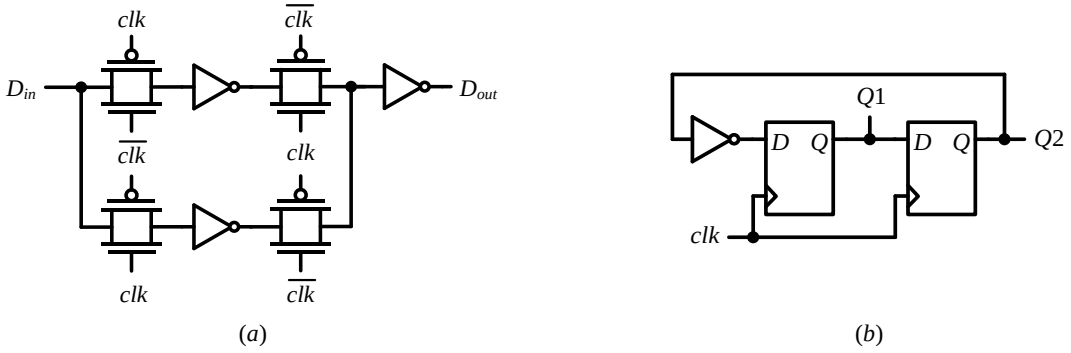


Figure 16. (*a*) Dual edge dynamic flip-flop (b) Divide by 4 circuits.

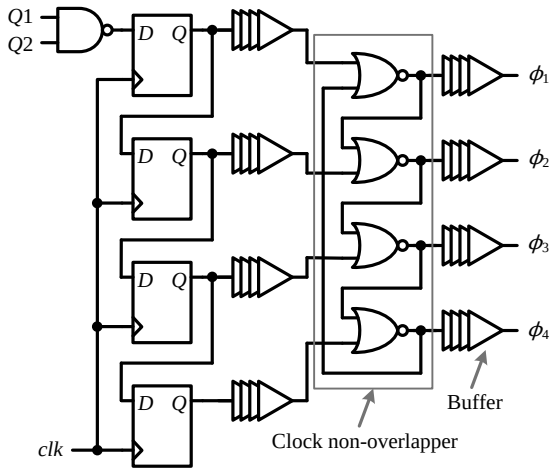


Figure 17. 4-phase clock generation circuit.

To achieve an adequate performance at such high frequencies a very careful layout design, addressing the matching of delay paths etc. is indispensible for this block

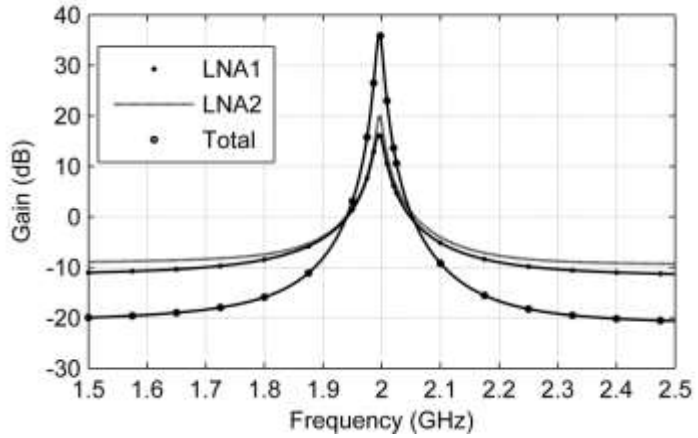


Figure 18. Sample simulated selectivity comparison obtained with first, second and combined two stages (C_{BB} = 40 pF).

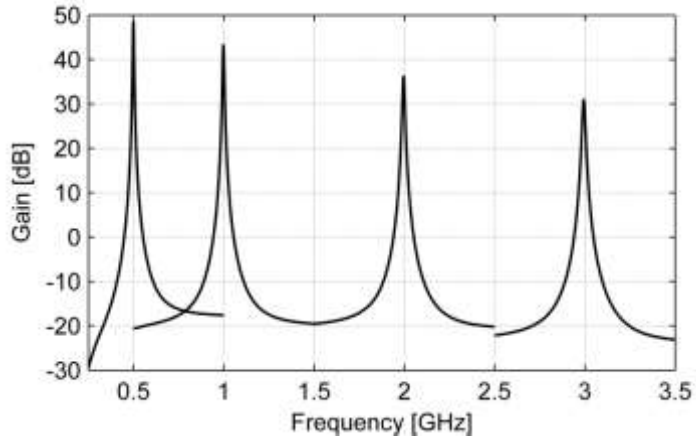


Figure 19. Simulated selectivity of the two-stage front end over different LO frequencies. (C_{BB} = 40 pF).

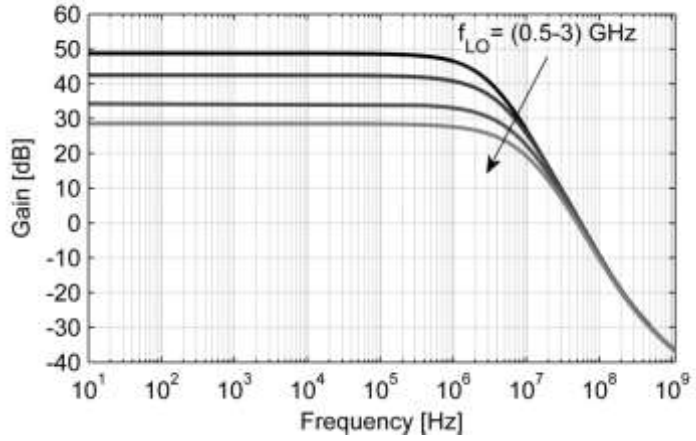


Figure 20. Simulated baseband frequency response for LO frequencies (0.5–3) GHz. (C_{BB} = 40pF).

5.4. Experimental results

In simulations shown in Figure 18 the filter at 2 GHz clock frequency demonstrates blocker attenuation in excess of 10 dB for offsets Δf > 100 MHz and up to 20 dB for higher offsets when C_{BB} = 40pF. The maximum blocker rejection by the first stage is 27 dB and it is increased to 55 dB by the second stage. Simulated

frequency response of the two stage front-end at RF for LO frequencies 0.5–3 GHz is also presented in Figure 19. From the plot the band limitation caused by parasitic capacitances at RF is evident. The corresponding baseband frequency response (Figure 20) for C_{BB} = 40pF also highlights the gain reduction at higher LO frequencies.

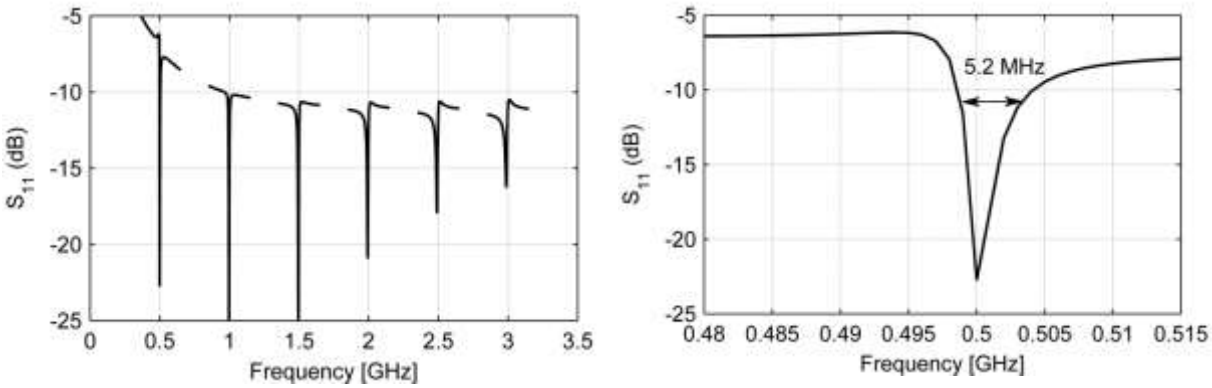
Measured S11 for different LO frequencies is shown in Figure 21(a). Within the whole range of 0.5–3 GHz frequencies S11 is below -10 dB in the bandwidth of interest. This is demonstrated for the case of 0.5 GHz LO in Figure 21(b).

The measured blocker rejection (Figure 22) is less than simulated for two reasons: 1) the signal gain is reduced by parasitic caps more than expected by the simulation models; 2) the practical clock duty cycle is less than 25% that elevates the gain at offset frequencies. Moreover, those imperfections are more pronounced towards higher clock frequencies. Nevertheless the achieved rejection is competitive to that offered by SAW filters.

The front-end signal gain between the input and baseband in the second stage is plotted in Figure 23. The measured gain is lower by 3 – 5 dB as explained above. The drop of gain transforms directly on the front-end NF that increases with clock frequency as illustrated in Figure 24. As compared to simulations the measured NF is raised by 1 – 1.3 dB that is mostly a result of the gain reduction in the first stage. In the presence of a blocker NF suffers due to reciprocal mixing and compression. At 2 GHz clock frequency with a 0dBm blocker @100MHz offset the NF is raised to ~12dB as compared to 4.5dB.

With two-stage blocker rejection the front-end achieves IIP3 as high as +20 dBm with 100 MHz spacing towards low clock frequencies and it drops to +17 dBm at 3 GHz frequency.

As shown in Figure 25 the circuit benefits from the lower gain value that can be explained using (25). In this case, IIP3 of each stage tends to increase while the effect of reduced rejection η_1 does not prevail.



(*a*) (*b*)

Figure 21. (*a*) Measured S_{11} around LO frequencies stepped by 500 MHz for C_{BB} = 40pF (*b*) Zoomed in version of (*a*) around 0.5 GHz LO frequency.

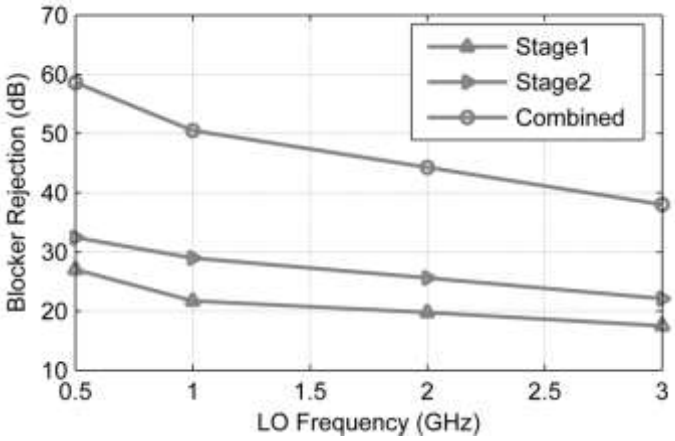


Figure 22. Measured blocker rejection within the front-end

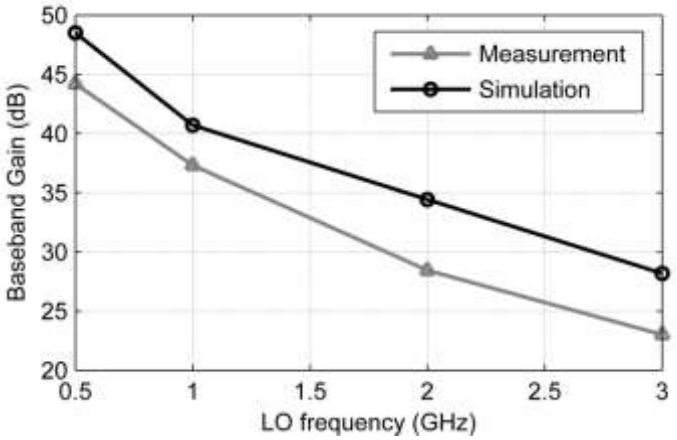


Figure 23. Baseband voltage gain of the front-end.

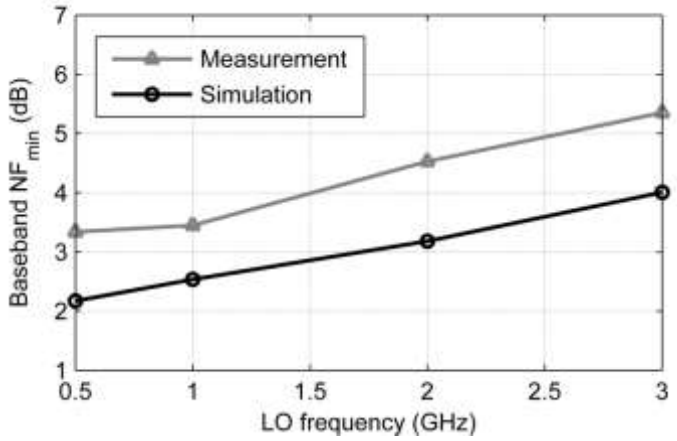


Figure 24. NF of two-stage front-end vs. LO frequency.

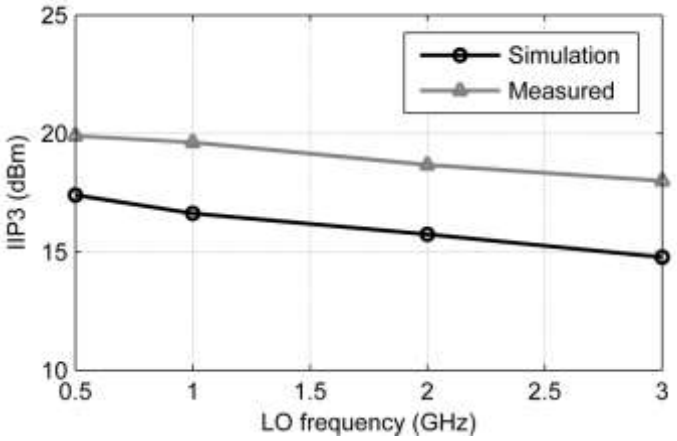


Figure 25. IIP3 @100 MHz spacing of two-stage front-end.

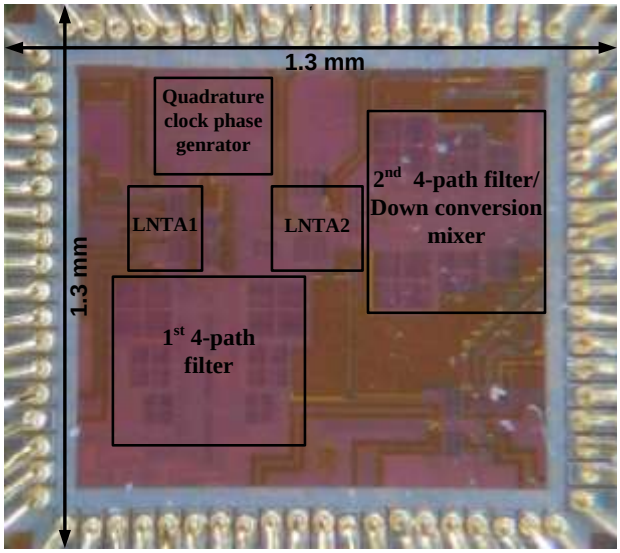


Figure 26. Chip photo (65 nm CMOS)

The chip photo is shown in Figure 26. A significant portion of the chip area is occupied by the banks of baseband capacitors C_{BB}, which allow for bandwidth programming. The maximum power consumption at 3 GHz amounts for 113 mW and it drops to 46 mW at 0.5 GHz.

Table I
Front end Performance Summary and Comparison

	This work	[6] (a)	[14] (a)	[13]
Technology	65 nm	65nm	40 nm	65 nm
System	Front-end	Front-end	Front-end	BP RF Filter
Frequency [GHz]	0.5 – 3	0.1-2.4	0.8 – 2.9	0.1 – 1.2
Gain [dB]	45 – 25	40 – 70 (b)	58	1.5
NF [dB]	3.2 – 5.3	3 – 5	1.9/(5.5 – 8) (c)	10
NF@0dBm blocker [dB]	12@100 MHz offset for 2 GHz LO	N/A	4.1/7.2@80 MHz (d) offset for 1.5 GHz LO	N/A
Out-of-band IIP3@100MHz [dBm]	+20	+25	+13/15 (c)	+29
Blocker P_{1dB}@100MHz [dBm]	+5	+10	0/+4 (c)	NA
Power Consumption [mW]	46 – 113	37 – 70	50 – 100	21.4
Chip area [mm^2]	1.7	2.5	1.1	1

(a) 8-path filtering
(b) Gain achieved by BB amplifiers
(c) Noise Cancellation ON/Noise cancellation OFF.
(d) Single Ended/Differential Architecture

In Table I we compare this work with the state-of-the-art designs. The reported performances should be compared to our work with reservations since [6] and [14] address 8-path filters, whereas in [13] no amplifier is used. Hence, the latter provides superior out-of-band IIP3 but the lack of gain results in high NF, accordingly.

Our two-stage architecture unlike the other designs provides superior blocker rejection which compares well with SAW filters. This largely mitigates the requirements for IIP2 in down-conversion. Also the reciprocal mixing is reduced in this way. On the other hand, very high linearity and good NF put the presented work well in line with the others.

6. CONCLUSIONS

In this paper we have investigated RF filtering based on four-path impedance transformation technique useful for software-defined radio or cognitive radio. Using low-noise transconductance amplifiers and switches with low on-resistance, a blocker rejection competitive to SAW filters was attained (> 40 dB for $f_0 \leq 2$ GHz) in a two-stage setup without compromising the noise figure and IP3. Gain compression for the largest blockers

(0 dBm) due to limited voltage headroom of the 65 nm CMOS devices has been avoided by using elevated supply voltage and a deliberate input impedance mismatch. The chip design was supported by detailed analysis of the filter gain, blocker rejection, noise figure, and phase noise. Several tradeoffs such as blocker attenuation vs. noise figure or signal gain vs. reciprocal mixing noise have challenged the design.

The main advantage of the two-stage tunable RF filter is in high blocker rejection that largely mitigates the demands for IP2 calibration of the down-conversion mixer, i.e. of the second filter stage. While the gain of the first stage helps to keep the front-end noise figure low, the attenuation for out-of-band blockers limits the IM3 product of the second stage and thereby the front-end IIP3 is high. In the same way the phase noise effect (i.e. reciprocal mixing) in the second stage is largely limited. On the other hand, the blocker rejection does not help to reduce the reciprocal mixing in the first stage and thereby, the demands placed on the clock phase noise are high, like in single stage solutions [14].

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APPENDIX A

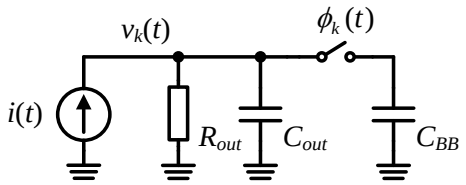

Figure A1. Model of multi-phase capacitance up-conversion circuit.

We assume the source output impedance as ($R_{out} \parallel C_{out}$) and $R_{sw} << R_{out}$. For a sinusoidal input signal at clock frequency ω_0 and $\phi_k(t) = 1$, the voltage at the source can be found as a superposition of the steady-state and transient response

$$v_k(t) = \frac{A\sin(\omega_0 t + (k-1)\pi/2 - \varphi)}{\sqrt{1+(\omega_0 T)^2}} + \Delta V_k \exp\frac{-t}{T} \tag{A1}$$

where $A = I_0 R_{out}$ with I_0 as an amplitude of the sinusoidal source current $i(t)$, whereas $T = R_{out}(C_{out} + C_{BB})$ and $\varphi = \tan^{-1}(\omega_0 T)$. When we define $v_k(0) = V_{kON}$ and and for 4-phase clock $v_k(T_0/4) = V_{kOFF}$ where $T_0 = 2\pi/\omega_0$ then from (A1)

$$\begin{aligned} V_{kON} &= \frac{A\sin((k-1)\pi/2 - \varphi)}{\sqrt{1+(\omega_0 T)^2}} + \Delta V_k \\ V_{kOFF} &= \frac{A\sin(k\pi/2 - \varphi)}{\sqrt{1+(\omega_0 T)^2}} + \Delta V_k \exp\frac{-T_0}{4T} \end{aligned} \tag{A2}$$

Moreover, we observe that the circuit is periodically time varying (LPTV) where the charge on cap C_{out} is shared with the C_{BB} caps connected one by one over the full clock cycle. That means the voltage V_{kON} is subject to V_{kOFF} from the previous clock cycle (for $\phi_k(t) = 0$ C_{BB} retains its charge) and the voltage from the previous phase $V_{k\text{-}1OFF}$ provided by charge on C_{out}.

$$V_{kON} = \frac{C_{BB}}{C_{BB}+C_{out}} V_{kOFF} + \frac{C_{out}}{C_{BB}+C_{out}} V_{k-1OFF} \tag{A3}$$

where according to the periodic behavior, for $k = 1$ we have $V_{k\text{-}1OFF} = V_{4OFF}$. Since $\omega_0 T >> 1$ and $\varphi \approx \pi/2$ (A2) can be simplified to

$$V_{kON} \cong \frac{-A\sin(k\pi/2)}{\omega_0 T} + \Delta V_k \tag{A4}$$

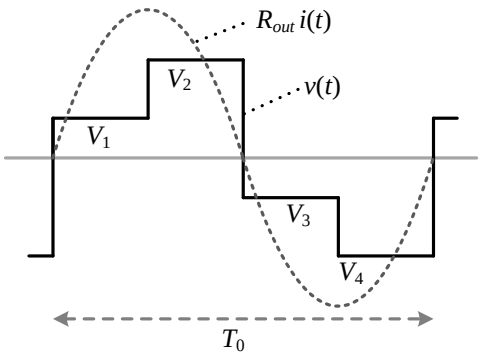

Figure A2. Waveforms in 4-path capacitance up-conversion circuit.

$$V_{kOFF} \cong \frac{A\sin\left((k-1)\pi/2\right)}{\omega_0 T} + \Delta V_k \exp\frac{-T_0}{4T} \tag{A5}$$

Solving (A3), (A4) and (A5) and assuming $T_0 << T$ we find

$$V_{kOFF} \cong A_k + mV_{k-1OFF} \tag{A6}$$

where

$$\begin{aligned} m &= \frac{\omega_0 R_{out} C_{out}}{\omega_0 R_{out} C_{out} + \pi/2} \\ A_k &= A \times \frac{\sin\left(k\pi/2\right) - \cos\left(k\pi/2\right)}{\omega_0 R_{out} C_{out} + \pi/2} \end{aligned} \tag{A7}$$

Using substitution $\left(\omega_0 R_{out} C_{out} + \pi/2\right)^{-1} = 2(1-m)/\pi$, finally we find

$$\begin{aligned} V_{1OFF} &= \frac{2A}{\pi} \times \frac{1 - m - m^2 + m^3}{1 + m + m^2 + m^3} \\ V_{2OFF} &= \frac{2A}{\pi} \times \frac{1 + m - m^2 - m^3}{1 + m + m^2 + m^3} \\ V_{3OFF} &= -V_{1OFF} \\ V_{4OFF} &= -V_{2OFF} \end{aligned} \tag{A8}$$

Note that the polynomials in (A8), defined in variable *m*, reflect the 4-phase clocking scheme. Moreover, we observe that the steady-state component in (A1) is practically negligible since $\omega_0 T >> 1$ and hence, we can assume $V_{kON} \cong V_{kOFF}$ and define it as V_k for $k = 1,\ldots 4$. The respective waveform $v(t)$ over the four phases of the clock is depicted in Figure A2. We also observe that $V_2 > V_1$ unless $m = 0$ that reflects inertial behavior of the filter due to band limitation by the source impedance.

To find the filter gain at the fundamental frequency ω_0 we calculate the first harmonic of $v(t)$ defined as

$$v_{fund}(t) = a_1 \sin(\omega_0 t + \alpha_1) \tag{A9}$$

where the amplitude and phase are

$$a_1 = \frac{2\sqrt{2}A}{\pi}\sqrt{V_1^2 + V_2^2}, \quad \alpha_1 = \tan^{-1}\frac{V_1 + V_2}{V_2 - V_1} - \frac{\pi}{2} \tag{A10}$$

For the input voltage $v_{in}(t) = A\sin\omega_0 t$ the gain of the filter is $k_V = a_1 \exp(j\alpha_1)/A$. Using (A9-A10) k_V is found as

$$k_V = \frac{8}{\pi^2} \times \frac{(1-m)(1-jm)}{1+m^2} \tag{A11}$$

APPENDIX B

For the first stage, IIP3 can be found from

$$IIP3_1 = P_B + \frac{P_B - (P_{IM31} - G_1)}{2} \tag{B1}$$

where all quantities are in dB scale and P_{IM31} is the IM3 product at the output of this stage, G_1 is the respective signal power gain, P_B is the blocker power at the input (in each tone). Converting (B1) to linear scale we have

$$P_{IIP31} = P_B \sqrt{\frac{P_B G_1}{P_{IM31}}} \tag{B2}$$

Similarly for the second stage with 2-tone input, with power of $G_{B1}P_B$ in each tone (G_{B1} is gain for the blocker in the first stage)

$$P_{IIP32} = G_{B1} P_B \sqrt{\frac{P_B G_{B1} G_2}{P_{IM32}}} \tag{B3}$$

where G_2 is the respective signal power gain. The IM3 product at the output of the cascade is composed of P_{IM32} and P_{IM31} amplified by the second stage. We note that the respective components add in amplitude rather than in power and hence we have

$$P_{IM3} = \left(\sqrt{G_2 P_{IM31}} + \sqrt{P_{IM32}} \right)^2 \tag{B4}$$

Using (B2) and (B3) we can rewrite (B4) as

$$P_{IM3} = P_B^3 \left(\frac{\sqrt{G_1 G_2}}{P_{IM31}} + \frac{\sqrt{G_{B1}^3 G_2}}{P_{IM32}} \right)^2 \tag{B5}$$

The total IIP3 of the two stages can be expressed in a similar way

$$P_{IIP3} = P_B \sqrt{\frac{P_B G_1 G_2}{P_{IM3}}} \tag{B6}$$

By combination of (B5) and (B6) we find

$$\frac{1}{P_{IIP3}} = \frac{1}{P_{IIP31}} + \frac{G_{B1} \sqrt{G_{B1} / G_1}}{P_{IIP32}} \tag{B7}$$

where $\sqrt{G_{B1} / G_1}$ can be considered as rejection η_1.