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Design of a 12.8 ENOB, 1 kS/s Pipelined SAR ADC in 0.35- μ m CMOS

Kairang Chen · Prakash Harikumar · Atila Alvandpour

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Abstract This paper presents a 15-bit, two-stage pipelined successive approximation register (SAR) analog-to-digital converter (ADC) suitable for low-power, cost-effective sensor readout circuits. The use of aggressive gain reduction in the residue amplifier combined with a suitable capacitive array DAC topology in the second stage simplifies the design of the operational transconductance amplifier (OTA) while eliminating excessive capacitive load and consequent power consumption. An elaborate power consumption analysis of the entire ADC was performed to determine the number of bits in each stage of the pipeline. Choice of a segmented capacitive array DAC and attenuation capacitor-based DAC for the first and second stages respectively enable significant reduction in power consumption and area. Fabricated in a low-cost 0.35- μ m CMOS process, the prototype ADC achieves a peak SNDR of 78.9 dB corresponding to an effective number of bits (ENOB) of 12.8 bits at a sampling frequency of 1 kS/s and provides an FoM of 157.6 dB. Without any form of calibration, the ADC maintains an ENOB > 12.1 bits upto the Nyquist bandwidth of 500 Hz while consuming 6.7 μ W. Core area of the ADC is 0.679 mm².

Keywords pipelined SAR ADC · high resolution · OTA · capacitive DAC

1 Introduction

High-resolution (≥ 12 bits), low-sampling rate (several kS/s) ADCs are required in wireless sensor networks which are employed for monitoring bio-potential signals, environmental conditions and industrial processes [1]. These sensor nodes

are usually powered by batteries or energy-harvesting sources and hence low power consumption is paramount for the constituent ADCs. Distributed wireless sensor networks usually employ tens or hundreds of autonomously-powered sensor nodes to acquire, condition and relay data to a central location. Hence it is advantageous to fabricate the associated electronics including ADCs in a low-cost, standard CMOS process.

Even though the SAR ADC is renowned for its excellent power efficiency at moderate resolutions [2], the design of SAR ADCs with effective number of bits (ENOB) above 12 bits [1, 3–5] poses formidable challenges due to the requirements on comparator noise and capacitor matching. The pipelined SAR ADC also known as the SAR-assisted pipeline ADC harnesses the advantages of SAR and pipelined ADCs to realize high resolution and improved sampling rate. By incorporating a SAR ADC as the sub-ADC in the pipeline stages, the need for high-accuracy comparators and active front-end sample-and-hold can be obviated [6]. For a given resolution, the pipelined SAR ADC requires lesser number of stages compared to a conventional pipelined ADC which translates into substantial power savings. The speed bottleneck caused by the sequential SAR algorithm is alleviated in the pipelined SAR ADC especially for high resolutions. However, the pipelined SAR ADC requires a high-gain operational transconductance amplifier (OTA) to amplify the residue between stages with sufficient accuracy. Since the open-loop DC gain requirement of the residue amplifier increases exponentially with the total resolution of the ADC, the design of high-gain OTAs constitutes a major challenge for implementing high-resolution pipelined SAR ADCs.

Several works have employed inter-stage gain reduction in pipelined SAR ADCs to relax the requirements on the DC gain and output swing of the residue amplifier. Gain reduction also increases the feedback factor of the amplifier and thus improves the closed-loop bandwidth [6]. In [6],

Kairang Chen · Prakash Harikumar · Atila Alvandpour
Department of Electrical Engineering, Linköping University,
Linköping, Sweden
E-mail: kairang.chen@liu.se, prakash.harikumar@liu.se,
atila.alvandpour@liu.se

a gain reduction factor of $1/2$ has been used. Higher gain reduction factors will require increased resolution/sampling capacitance for the second stage sub-ADC to compensate for the reduced signal swing [7]. In this work, a gain reduction factor of $1/8$ has been used for the residue amplifier. The increased capacitance requirement in the second stage has been alleviated by choosing a binary-weighted capacitive DAC with attenuation capacitor. In high-resolution SAR ADCs, matching constraints necessitate large unit capacitors in the capacitive array which entails substantial power consumption and chip area. We have used a segmented capacitive array DAC in the first stage which meets the targeted static linearity with a lower unit capacitance compared to a conventional binary-weighted capacitive DAC. By choosing the proper number of bits for segmentation, the power consumption due to the binary-to-thermometer decoder has been kept low. Based on an exhaustive analysis of the power consumption of the different sub-blocks of a 15-bit pipelined SAR ADC, 7 bits and 9 bits were allocated to the first and second pipeline stages respectively which provided a good trade-off between implementation complexity and power savings. The prototype ADC achieves a peak ENOB of 12.8 bits while consuming $6.7 \mu\text{W}$ at a sampling frequency of 1 kS/s .

This paper is organized as follows. Section 2 provides an overview of the two-stage pipelined SAR ADC architecture. Section 3 describes the important features of the proposed ADC architecture. Section 4 discusses the implementation details of the ADC while Section 5 presents the measurement results and comparison to prior art. Finally, conclusions are drawn in Section 6.

2 Overview of the two-stage pipelined SAR ADC

The general architecture of the two-stage pipelined SAR ADC is shown in Fig. 1 [6]. To simplify the discussion, a single-ended version is shown. The resolutions for the first-stage and second-stage sub-ADCs are N_1 bits and N_2 bits respectively. An OTA with capacitive feedback implements the residue amplification between the pipeline stages. Because the second stage has one bit redundancy [8], the total resolution of the ADC is given by $N = N_1 + N_2 - 1$. Since the open-loop DC gain of the OTA grows exponentially with N , a very large DC gain is required for high-resolution pipelined ADCs [7, 9, 10].

Figure 2 shows the time sequence of the two-stage pipelined SAR ADC, where f_s is the sampling frequency of the first stage and f_r is the sampling frequency of the second stage. The input signal V_{in} is sampled by switch S_0 during phase f_s . During phase f_r , the switches S_1 and S_2 are turned on and the residue voltage from the first stage is amplified and sampled by the second stage sub-ADC. To increase the settling time available for input sampling and residue generation, the duration t_p for the phases f_s and f_r is set to $2/f_{clk}$ where f_{clk} is

Fig. 1 Two-stage pipelined SAR ADC architecture.

the system clock frequency of the pipelined SAR ADC [8]. The time interval for determining each output bit is $1/f_{clk}$. For odd N , the clock frequency can be derived as

Fig. 2 Time sequence of the two-stage pipelined SAR ADC.

$$f_{clk} = \begin{cases} (N_1 + 2t_p + 1)f_s & N_1 \geq N_2 \\ (N_2 + t_p + 1)f_s & N_1 = N_2 - 2 \\ (N_2 + t_p)f_s & N_1 < N_2. \end{cases}$$

If the total resolution N is even, then the clock frequency can be derived as

$$f_{clk} = \begin{cases} (N_1 + 2t_p + 1)f_s & N_1 > N_2 \\ (N_2 + t_p + 2)f_s & N_1 = N_2 - 1 \\ (N_2 + t_p)f_s & N_1 < N_2. \end{cases}$$

It is to be mentioned that the first-stage sub-ADC requires $N_1 + 1$ clock cycles to convert the N_1 bits and form the residue.

3 Features of the proposed ADC

Figure 3 shows the circuit details of the proposed ADC architecture. A single-ended version is shown for clarity while the actual implementation is fully differential. This section motivates the important design choices for the ADC implementation along with the relevant analyses. Selection of DAC topologies for the SAR stages, gain reduction in the residue amplifier and allocation of stage resolution are described.

Fig. 3 Proposed ADC architecture.

3.1 First-stage DAC topology

The static linearity of the first-stage SAR ADC shown in Fig. 3 is dominated by capacitor mismatch in the corresponding capacitive array DAC. For the conventional binary-weighted capacitive DAC, the maximum error caused by mismatch of capacitors occurs during the MSB code transition from '011...1' to '100...0' where all the capacitors switch states [11]. The worst-case standard deviation of the differential nonlinearity (DNL) for the N_1 bit first-stage DAC is given by [11]

$$\sigma_{DNL,max} \approx \frac{\sqrt{2^{N_1} - 1}}{2^{N_1}} \frac{\sigma_{C_{u1}}}{C_{u1}} V_{REF}, \quad (1)$$

where $\sigma_{C_{u1}}$ is the standard deviation and C_{u1} is the mismatch-limited unit capacitor of the sub-DAC. For the pipelined SAR ADC, although the resolution of the first stage is N_1 , the accuracy for the first stage must meet the total resolution N which requires

$$3\sigma_{DNL,max} < \frac{V_{REF}}{2^N} \quad (2)$$

where $V_{REF}/2^N$ is the least significant bit (LSB) of the N -bit ADC. Combining (1) and (2), we get

$$\frac{\sigma_{C_{u1}}}{C_{u1}} < \frac{1}{3 \cdot 2^{N-N_1} \cdot \sqrt{2^{N_1} - 1}}. \quad (3)$$

For a typical metal-insulator-metal (MIM) capacitor [2],

$$\frac{\sigma_{C_{u1}}}{C_{u1}} = \frac{K_\sigma}{\sqrt{2A}}, \quad C_{u1} = K_c \cdot A, \quad (4)$$

where A is the capacitor area, K_σ is the mismatch parameter and K_c is the capacitor density. Substituting (4) into (3), the mismatch-limited unit capacitor of the first-stage DAC can be derived as

$$C_{u1} > 4.5 K_\sigma^2 K_c 2^{2(N-N_1)} (2^{N_1} - 1). \quad (5)$$

Utilizing (1) and (4), $\sigma_{DNL,max}$ for the conventional binary-weighted capacitive DAC can be formulated as

$$\sigma_{DNL,max} \approx \frac{\sqrt{2^{N_1} - 1}}{2^{N_1}} \frac{K_\sigma \sqrt{K_c}}{\sqrt{2C_{u1}}} V_{REF}. \quad (6)$$

For the poly-insulator-poly (PIP) capacitor in 0.35- μm CMOS process, $K_\sigma = 0.45\%$ and $K_c = 0.86 \text{ fF}/\mu\text{m}^2$. Let the first stage DAC of the 15-bit ADC be implemented using a conventional binary-weighted array with $N_1 = 7$ bits. From (5), the minimum mismatch-limited unit PIP capacitor is 652 fF which results in a total capacitance of 83.4 pF for the first stage. The reason for choosing $N_1 = 7$ bits will be explained in Section 3.3.4.

It is desirable to lower the total capacitance of the DAC array to avail power and area savings. The required value of the mismatch-limited unit capacitor can be lowered without compromising linearity performance by using a segmented capacitive array DAC in the first stage. Since the number of capacitors to be switched during conversions is reduced in a segmented DAC, less voltage variation is caused by capacitor mismatch. The segmented first-stage DAC is composed of a k -bit unary-weighted array and an $(N_1 - k)$ -bit binary-weighted array where the k bits correspond to the MSBs of the array. The value of each capacitor in the unary-weighted array is $2^{N_1-k} C_{u1}$. The worst-case standard deviation of the DNL can be found as [11]

$$\sigma_{DNL,max} \approx \frac{\sqrt{2^{N_1-k+1} - 1}}{2^{N_1}} \frac{\sigma_{C_{u1}}}{C_{u1}} V_{REF}. \quad (7)$$

Substituting (4) into (7), $\sigma_{DNL,max}$ for the segmented binary-weighted capacitive DAC can be formulated as

$$\sigma_{DNL,max} \approx \frac{\sqrt{2^{N_1-k+1} - 1}}{2^{N_1}} \frac{K_\sigma \sqrt{K_c}}{\sqrt{2C_{u1}}} V_{REF}. \quad (8)$$

Comparing (6) and (8), it is seen that the $\sigma_{DNL,max}$ for the segmented DAC is $\sqrt{2^{k-1}}$ times lower than that of the conventional binary-weighted DAC. Using the same derivation procedure as for (5), the mismatch-limited unit capacitor for the first-stage segmented DAC can be obtained as

$$C_{u1} > 4.5 K_\sigma^2 K_c 2^{2(N-N_1)} (2^{N_1-k+1} - 1), \quad (9)$$

which is 2^{k-1} times lower than the C_{u1} for the conventional binary-weighted DAC. It is to be mentioned that the segmented DAC requires a binary-to-thermometer decoder and additional switches which lead to extra power consumption and chip area. Hence an excessive degree of segmentation

will outweigh the benefits of reduced DAC capacitance. In this work, a segmentation degree of $k = 3$ was chosen for the first stage DAC as a trade-off between lower unit capacitance value and increased complexity/power consumption in the digital logic. Fig. 4 plots $3\sigma_{DNL,max}$ vs. C_{u1} from (6) and (8) with $V_{REF} = 3.3$ V together with Monte Carlo simulations for the segmented DAC using PIP capacitors. Monte Carlo simulations involved 100 runs simulating the worst-case DAC switching scenario for each C_{u1} value. For the 15-bit ADC with $V_{REF} = 3.3$ V, $LSB = 100.7 \mu V$. It is seen from Fig. 4 that the segmented DAC requires only $C_{u1} = 159$ fF compared to $C_{u1} = 652$ fF for the conventional DAC to satisfy the condition in (2). The corresponding total capacitance of the segmented first-stage DAC is 20.35 pF.

Fig. 4 $3\sigma_{DNL,max}$ versus C_{u1} .

Since the DAC array capacitance of the first stage is used for sampling the inputs of the ADC, the kT/C noise of the sampling switches also imposes a restriction on the minimum value of the unit capacitance. For the first stage of the pipelined SAR ADC, the thermal noise from the sampling switches should be below the quantization noise of the 15-bit ADC. From [12], the thermal-noise limited unit capacitance is computed as

$$C_{u1,n} = 12kT \frac{2^{2N-N_1}}{V_{FS}^2} \quad (10)$$

where k is the Boltzmann constant, T is the absolute temperature and V_{FS} is the full-scale range of the ADC. For $N = 15$, $N_1 = 7$, $T = 300$ K and $V_{FS} = 3.3$ V, $C_{u1,n} = 38$ fF which is significantly lower than the mismatch-limited C_{u1} . Apart from mismatch and noise, the technology process also sets a lower limit on the unit capacitance through minimum feature sizes. The final value of unit capacitance is chosen as $\max(C_{u1}, C_{u1,n}, C_{pro})$, where C_{pro} is the process-limited unit capacitor. In this work, the mismatch-limited C_{u1} sets the unit capacitance in the first-stage DAC.

3.2 Gain reduction and second-stage DAC topology

An OTA with capacitive feedback implements the residue amplifier as shown in Fig. 3. The error in the amplified residue due to the finite DC gain of the OTA must be less than 1 LSB of the N -bit pipeline ADC which requires

$$\frac{V_{res}}{A\beta} < \frac{V_{REF}}{2^N}, \quad (11)$$

where A is the DC gain of the OTA and β is the feedback factor. The maximum value of the residue voltage from the first-stage is

$$V_{res} = \frac{V_{REF}}{2^{N_1}}. \quad (12)$$

Substituting (12) in (11), the requirement on A is obtained as

$$A > \frac{2^{N-N_1}}{\beta}. \quad (13)$$

The proposed ADC has $N_1 = 7$. Without any form of inter-stage gain reduction, the value of $C_f = 2C_{u1}$. The resulting feedback factor is

$$\beta = \frac{2C_{u1}}{2C_{u1} + 2^{N_1}C_{u1}} \approx 2^{1-N_1} \quad (14)$$

Using the value of β from (14) in (13) gives

$$A > 2^{N-1} \quad (15)$$

Thus the 15-bit ADC without gain reduction will require $A > 84.3$ dB. Allocating a 6 dB margin to maintain performance over process, supply voltage, and temperature (PVT) variations leads to $A > 90$ dB. Also the maximum amplitude of the amplified residue will be $V_{REF}/2$ which demands rail-to-rail output swing for the OTA. Since the design of an OTA with such specifications constitutes a formidable challenge, gain reduction has been employed in the residue amplifier to relax the OTA specifications.

To effect gain reduction, we set $C_f = 2^m C_{u1}$ where m is an integer. The value of m is sufficiently lower than N_1 so that the feedback factor $\beta \approx 2^{m-N_1}$. Consequently

$$A > 2^{N-m}. \quad (16)$$

Thus the DC gain requirement for the OTA is reduced 2^{m-1} times compared to (15). However, the signal swing at the input of the second-stage SAR ADC in Fig. 3 is proportionately reduced. Maintaining the same SNR for the second-stage ADC requires sufficient lowering of the noise floor.

The output voltage of a two-stage pipelined ADC (V_{pip}) with 1-bit redundancy in the first stage is given by

$$\begin{aligned} V_{pip} &= \frac{V_{REF}}{2^{N_1} C_{u1}} \sum_{i=0}^{N_1-1} 2^i C_{u1} D_i + \frac{1}{G} \left(\frac{V_{REF}}{2^{N_2} C_{u2}} \sum_{i=0}^{N_2-2} 2^i C_{u2} D_i \right) \\ &= \frac{V_{REF}}{2} D_{N_1-1} + \dots + \frac{V_{REF}}{2^{N_1}} D_0 + \frac{1}{2^{N_1-1}} \\ &\quad \left(\frac{V_{REF}}{2^2} D_{N_2-2} + \dots + \frac{V_{REF}}{2^{N_2}} D_0 \right). \end{aligned} \quad (17)$$

where the inter-stage gain $G = 2^{N_1-1}$. When gain reduction with $C_f = 2^m C_{u1}$ is applied, the output voltage becomes

$$\begin{aligned} V_{pip} &= \frac{V_{REF}}{2^{N_1} C_{u1}} \sum_{i=0}^{N_1-1} 2^i C_{u1} D_i + \frac{1}{G} \left(\frac{V_{REF}}{2^{N_2} C_{u2}} \sum_{i=0}^{N_2-2} 2^i C_{u2} D_i \right) \\ &= \frac{V_{REF}}{2} D_{N_1-1} + \dots + \frac{V_{REF}}{2^{N_1}} D_0 + \frac{1}{2^{N_1-m}} \\ &\quad \left(\frac{V_{REF}}{2^2} D_{N_2-2} + \dots + \frac{V_{REF}}{2^{N_2}} D_0 \right). \end{aligned} \quad (18)$$

where the inter-stage gain $G = 2^{N_1-m}$. By comparing (18) and (17), it is evident that the total capacitance of the second-stage SAR ADC has to be increased 2^{m-1} times in order to obtain the same output voltage. The resulting total capacitance required in the second stage is

$$C_{total} = 2^{m-1} \cdot 2^{N_2} C_{u2}. \quad (19)$$

where the C_{u2} is the unit capacitance and $2^{N_2} C_{u2}$ is the total capacitance of the conventional binary-weighted DAC. An extra capacitor C_x has been added as shown in Fig. 3 to satisfy the total capacitance requirement. Hence inter-stage gain reduction involves a trade-off between relaxed OTA specifications and increased capacitance in the second stage. In this work, $m = 3$ has been chosen which provides a lower DC gain requirement $A > 72.2$ dB for the OTA and reduced output swing of $V_{REF}/8$ which corresponds to a differential output swing of 0.825 V pp. The design of the OTA is thus considerably simplified.

The choice of $m = 3$ entails a four-fold increase in the second-stage input capacitance as seen from (19). The N_2 -bit second-stage sub-ADC requires $3\sigma_{DNL,max} < V_{REF}/2^{N_2}$ to satisfy the linearity requirement. Utilizing a procedure similar to the derivation of (5), C_{u2} for a conventional binary-weighted DAC is obtained as

$$C_{u2} > 4.5 K_{\sigma}^2 K_c (2^{N_2} - 1). \quad (20)$$

A binary-weighted DAC with attenuation capacitor consisting of an M -bit main-DAC and S -bit sub-DAC as shown in Fig. 3 where $M + S = N_2$ has been implemented in this work to mitigate the total capacitance requirement in the

DAC. For the second-stage DAC, $N_2 = 9$, $M = 5$ and $S = 4$ resulting in a total effective capacitance of

$$C_{total} = 2^{m-1} \cdot 2^M C_{u2}. \quad (21)$$

The mismatch-limited unit capacitance for the attenuation capacitor based DAC is given by [13]

$$C_{u2} > 4.5 K_{\sigma}^2 K_c 2^{2(N_2-M)} (2^M - 1). \quad (22)$$

It can be readily seen from (20) and (22) that the attenuation-based DAC imposes a large C_{u2} value. However the C_{u2} values from (20) and (22) are much lower than the process-limited minimum PIP capacitor. Hence a C_{u2} value which is adequately larger than the process-limited capacitor has to be used in both the DACs. Comparing (19) and (21) using the same C_{u2} value, it is found that the attenuation-based DAC reduces the total capacitance of the second-stage DAC by a factor 1/16. Finally the extra capacitor used is given by

$$C_x = (2^{m-1} - 1) \cdot 2^M C_{u2}. \quad (23)$$

3.3 Analysis of the ADC power consumption

In low sampling rate SAR ADCs, a substantial portion of the total power consumption is due to the capacitive DAC [2, 14]. Proper choice of unit capacitance and DAC topology is crucial for minimizing the power consumption in SAR ADCs. For the 15-bit pipelined SAR ADC, the resolutions N_1 and N_2 for the first and second stage sub-ADCs have been determined with the aid of power consumption analysis for the entire ADC. The choice of the segmentation degree k in the second stage ADC is also elaborated upon in this section.

3.3.1 DACs in the pipeline stages

The DAC power consumption is directly proportional to the total capacitance. The first-stage ADC utilizes a segmented DAC which achieves the targeted DNL performance using a lower unit capacitance as discussed in Section 3.1. The average power consumption of the segmented N_1 -bit DAC with a unary-weighted segment of k MSBs and $N_1 - k$ binary-weighted LSBs is given by [15] as

$$P_{DAC_seg} \approx 0.66 \cdot 2^{N_1} f_s C_{u1} V_{REF}^2 \cdot (0.6 + 0.4 \left(\frac{1}{2}\right)^{k-1}), \quad (24)$$

where C_{u1} is the unit capacitor of the first stage. In the second stage, a binary-weighted capacitive DAC with attenuation capacitor has been employed to mitigate the increased capacitance requirement due to gain reduction as shown in Section 3.2. The power consumption of the attenuation capacitor based DAC is computed as the sum of the power consumption of the M -bit main DAC and S -bit sub-DAC.

Following the analysis in [16], the power consumption of the attenuation capacitor based DAC is given by

$$P_{DAC_att} = P_{1,main_DAC} + P_{sub_DAC}, \quad (25)$$

where

$$P_{1,main_DAC} \approx 2^M f_s C_{u2} V_{REF}^2 \cdot \left(\frac{5}{6} - \frac{1}{2} \left(\sum_{i=1}^{M-1} \frac{D_i}{2^i} \right)^2 \right) \quad (26)$$

$$P_{sub_DAC} \approx 2^S f_s C_{u2} V_{REF}^2 \cdot \left(\frac{5}{6} - \frac{1}{2} \left(\sum_{i=1}^{S-1} \frac{D_{M+i}}{2^i} \right)^2 \right). \quad (27)$$

Since an additional capacitor C_x given by (23) is required to maintain the same SNR, the power consumption of the DAC needs to be modified accordingly. The charge on the DAC capacitors varies according to the DAC output voltage V_{DAC_i} where V_{DAC_i} is given by

$$V_{DAC_i} = \frac{\sum_{i=1}^{M-1} 2^i C_{u2} D_i}{C_{total}} V_{REF}. \quad (28)$$

For the M-bit main-DAC, the total capacitance is increased to $C_{M_total} = 2^{M+m-1} C_{u2}$ which means that $V_{DAC,i}$ of the main DAC is reduced 2^{m-1} times. Hence the power consumption for the main DAC is also reduced with the same ratio resulting in

$$P_{2,main_DAC} \approx 2^M f_s C_{u2} V_{REF}^2 \cdot \left(\frac{5}{6} - \frac{1}{2} \left(\sum_{i=1}^{M-1} \frac{D_i}{2^i} \right)^2 \right) \frac{1}{2^{m-1}}. \quad (29)$$

When it comes to the sub-DAC, the total capacitance is given by

$$C_{S_total} = 2^S C_{u2} + C_{S0}, \quad (30)$$

where C_{S0} , the total capacitance from the main-DAC, is expressed as

$$C_{S0} = C_a || (2^{M+m-1} - 1) C_{u2}. \quad (31)$$

where the $C_a = \frac{2^S}{2^S - 1} C_{u2}$ is the attenuation capacitor. With larger capacitance in the main DAC, C_{S0} more closely approximates C_a indicating that the total capacitance of the sub-DAC does not change due to the addition of C_x . Hence the power consumption of the sub-DAC is still given by (27). The total power consumption for the attenuation DAC with C_x is given by

$$P_{DAC_att} = P_{2,main_DAC} + P_{sub_DAC}. \quad (32)$$

A simplified expression for (32) using $D_i = 1$ is obtained as

$$P_{DAC_att} \approx 0.66 \cdot f_s C_{u2} V_{REF}^2 \left(\frac{2^M}{2^{m-1}} + 2^S \right). \quad (33)$$

3.3.2 OTA and Dynamic Comparator

The OTA amplifies the residue signal for conversion in the second pipeline stage. Following the analysis in [17], the power consumption of the OTA can be expressed as

$$P_{ota} = 2V_{FS}^2 f_s C_{LA} \left(1 + (1 + |G|) N \ln 2 \cdot \frac{V_{eff}}{V_{FS}} \right), \quad (34)$$

where C_{LA} is the capacitive load of the OTA, V_{FS} is the full-scale range of the ADC and $G = 2^{N_1-m}$ is the closed-loop voltage gain. For a classical MOS transistor in strong inversion, the parameter $V_{eff} = (V_{gs} - V_T)/2$, where V_{gs} and V_T are the gate-to-source and threshold voltages respectively [17]. Because the amplifier operates only during the sampling phase of the second stage, the OTA load capacitance can be approximated to the total capacitance of the second-stage DAC which means that the additional C_x will increase the power consumption of the OTA.

The dynamic latch comparator is used in the first and second stage SAR ADCs. It only consumes dynamic power during the reset and regeneration phases. Normally, the duty cycle of the clock signal is 50%. So, the reset and regeneration time are the same ideally. As shown in [17], the power consumption for the regeneration phase can be derived as

$$P_{c,reg_i} = 2 \ln 2 \cdot N_i f_{clk} C_{LC_i} V_{FS} V_{eff} \quad i = 1, 2, \quad (35)$$

where i is the stage number and C_{LC_i} is the capacitive load of the comparator which is determined by the thermal noise of the i^{th} stage. For the reset phase, it is a process of discharge. We assume that the voltage drops from V_{FS} to 0. The power consumption for the reset phase can be derived as

$$P_{c,rst_i} = 2 f_{clk} V_{FS}^2 C_{LC_i} \quad i = 1, 2. \quad (36)$$

So the total power consumption for the dynamic latch comparator is

$$\begin{aligned} P_{c,tot_i} &= P_{c,reg_i} + P_{c,rst_i} \\ &= 2 \ln 2 \cdot N_i f_{clk} C_{LC_i} V_{FS} V_{eff} + 2 f_{clk} V_{FS}^2 C_{LC_i} \quad i = 1, 2 \end{aligned} \quad (37)$$

3.3.3 Digital blocks

The conventional method to build the SAR logic is to use D-type Flip Flops (DFF). Based on the analysis provided in [12], the power consumption of the synchronous SAR logic in each pipeline stage can be expressed as

$$P_{sar_i} = 16 N_i \alpha f_{clk} C_{min} V_{DD}^2 \quad i = 1, 2, \quad (38)$$

where C_{min} is the input parasitic capacitor of a minimum-sized inverter, V_{DD} is the supply voltage, and α represents the total switching activity of the SAR logic.

A binary-to-thermometer decoder is required for implementing the segmented DAC. The power consumption for a k -bit decoder is given by [15]

$$P_{dec} \approx 6\alpha 2^k f_{clk} C_{min} V_{DD}^2. \quad (39)$$

3.3.4 Power consumption of the pipelined SAR ADC

Ignoring the power consumption of the switches and the leakage currents, the total power consumption is found using (24), (33), (34), (37), (38), and (39) as

$$P_{total} = P_{DAC_seg} + P_{DAC_att} + P_{ota} + P_{dec} + \sum_{i=1}^2 (P_{sar_i} + P_{c,tot_i}). \quad (40)$$

In order to predict the power consumption bound for the two-stage pipelined SAR ADC, the following typical CMOS parameters are used. For 0.35- μm CMOS, $V_{eff} = 300$ mV and $C_{min} = C_{pro} = 3$ fF [17]. For the first stage, the mismatch-limited PIP capacitor given by (9) is used for the analysis. With $T=300$ K, $k=3$, $m=3$, $\alpha=0.4$ and $V_{DD} = V_{REF} = V_{FS} = 3.3$ V, Fig. 5 plots the total ADC power given by (40) as a function of the first-stage resolution N_1 for three different scenarios of the second-stage unit capacitor C_{u2} . The mismatch-limited power bound in Fig. 5 is of little use when $N_1 > 6$ bits because the mismatch-limited C_{u2} is smaller than the process-limited capacitor as illustrated in Section 3.2. In contrast, the mismatch-limited C_{u2} dominates the power consumption for $N_1 < 6$ bits. In this work, the ADC is pipelined with $N_1 = 7$ bits and $N_2 = 9$ bits as a compromise between lower power consumption and increased complexity in the second-stage sub-ADC.

Fig. 5 Predicted power bounds for the 15-bit pipelined SAR ADC.

As per the discussion in Section 3.2, it is necessary to make a trade-off between the inter-stage gain reduction factor m and the increased power consumption due to larger

capacitance in the second stage sub-ADC. Fig. 6 plots the OTA power consumption according to (34) as a function of m . The value of C_{LA} is given by (21) where $C_{u2} = 3$ fF, the process-limited unit capacitance and $M = 5$. Based on Fig. 6, $m = 3$ has been chosen which considerably relaxes the OTA specifications without entailing excessive power consumption due to the increased capacitive load.

Fig. 6 OTA energy consumption versus inter-stage gain reduction factor.

In order to find the optimal degree of segmentation k for the first-stage DAC, the power consumption of the segmented DAC, associated decoder and first-stage SAR logic was analyzed as a function of k . For this purpose, expressions in (24), (39) and (38) were used with the aforementioned values for the constituent parameters and $N_1 = 7$. The resulting plots are shown in Fig. 7. The total power in Fig. 7 is computed as the sum of (24), (38) and (39). It is seen that choosing $k \leq 2$ or $k > 5$ increases the total power consumption of the sub-ADC. As a compromise $k = 3$ was chosen.

4 Implementation details

This section describes the implementation details of the various circuit blocks.

4.1 First-stage sub-ADC

Based on the analysis in Section 3.3.4, the first pipeline stage has a resolution of 7 bits and utilizes a segmented DAC with $k = 3$. Incorporating some design margin for the unit capacitor $C_{u1} = 159$ computed using Fig. 4, a PIP capacitor with the value of 212 fF was chosen to design the segmented DAC resulting in a total capacitance of 27 pF for the first

Fig. 7 Energy consumption of segmented SAR ADC versus k .

stage. Fig. 8 shows the schematic of the 3-to-7 binary-to-thermometer decoder required for the unary-weighted 3-bit DAC segment which consists of basic logic gates.

Fig. 8 3-to-7 binary to unary thermometer decoder.

The block diagram of the SAR control logic for the first stage sub-ADC consisting of two separate shift registers is illustrated in Fig. 9. The upper DFF chain is triggered by a "set" signal which subsequently generates the switch control signals ($D14 \cdots D8$) for the DAC. Seven DFFs in the upper row generate the bit approximation pulses while the DFFs in the lower row store the output C_{out} of the comparator. The additional four DFFs on the far right side of Fig. 9 generate the sampling signals f_s and f_r as shown in Fig. 2 for the first-stage and second-stage respectively.

For the input sampling switch S_0 in Fig. 3, the bootstrap technique [18] is used for improved linearity. Simulation results indicate a linearity corresponding to 18.1 bits for S_0 with a sampling capacitance of 27 pF and 1 kS/s sampling frequency which is sufficient for the 15-bit ADC. The conventional dynamic latch comparator [19] is used to generate the digital output bits. Simple inverters have been used to implement the DAC switches in both pipeline stages.

Fig. 9 SAR control logic.

4.2 OTA

According to the analysis in Section 3.2, the inter-stage gain reduction factor $m = 3$ lowers the open-loop DC gain of the OTA to 72.25 dB while the maximum differential output swing is relaxed to 0.825 V pp. A simple two-stage OTA with Miller compensation as shown in Fig. 10 was implemented in this work. With $V_{DD} = 3.3$ V, the simulated open-loop DC gain of the OTA is 89.7 dB which affords > 10 dB design margin. The unity-gain frequency and phase margin are 298 kHz and 72° respectively with a load capacitance of ≈ 2 pF which corresponds to the second-stage DAC capacitance. The HD3 is -69.09 dB with a differential output swing of 0.825 V pp. Switched capacitor common-mode feedback (CMFB) circuits were used for both stages of the OTA.

Fig. 10 Two-stage OTA with Miller compensation.

4.3 Second-stage sub-ADC

A 9-bit SAR ADC with attenuation capacitor based DAC forms the second-stage sub-ADC. The DAC consists of a 5-bit main-DAC and 4-bit sub-DAC. Owing to the use of gain reduction, the total capacitance is given by (21) where $m = 3$ and $M = 5$. A unit PIP capacitor $C_{u2} = 15$ fF was chosen yielding a total capacitance of 1.94 pF. The SAR logic for the second stage is similar to that shown in Fig. 9. However, the four DFFs in Fig. 9 that generate the sampling signals f_s and f_r are omitted in the second stage. Since the resolution of

this stage is 9-bit, a transmission gate was used to design the sampling switch S_2 shown in Fig. 3. The same dynamic latch comparator topology as in the first stage is used to generate the digital output bits.

5 Measurement Results

The fully differential 15-bit ADC with a core area of $900\ \mu\text{m} \times 754\ \mu\text{m}$ was fabricated in a one-poly-four-metal (1P4M) 0.35- μm CMOS process. The core was packaged in a JLCC44 package. The chip micrograph is shown in Fig.11. The unmarked area in Fig.11 includes decoupling capacitors and I/O buffers. Fig.12 shows the measured FFT spectrum of the

Fig. 11 Chip micrograph of the ADC.

ADC operating at a sampling rate of 1 kS/s with near-DC (10 Hz) and near-Nyquist (490.97 Hz) input tones. The amplitude of the input signal was set to -0.066 dBFS. A clock frequency of $f_{clk} = 12\ \text{kHz}$ was used. The SNDR, SFDR and ENOB are 78.86 dB, 91.66 dB and 12.8 bits respectively with the near-DC input tone. For the near-Nyquist input tone SNDR, SFDR and ENOB are 74.84 dB, 92.87 dB and 12.1 bits respectively. The SNDR and SFDR over the range of input signal frequencies up to the Nyquist bandwidth for 1 kS/s are shown in Fig.13. An SNDR $> 74\ \text{dB}$ is maintained up to the Nyquist bandwidth. Histogram test was used to measure the static linearity of the ADC. A 5.127 Hz fully differential sinusoidal input tone was applied to the ADC. The measured differential nonlinearity (DNL) and integral nonlinearity (INL) of the ADC are shown in Fig. 14. The peak DNL and INL are 1.24/-0.93 LSB and 3.31/-2.94 LSB respectively.

With a supply voltage $V_{DD} = 3.15\ \text{V}$ for the OTA and $V_{DD} = 3\ \text{V}$ for the rest of the circuits, the total power consumption of the ADC is $6.7\ \mu\text{W}$. The OTA consumes $6.19\ \mu\text{W}$ while the sub-ADCs consume $0.522\ \mu\text{W}$. The OTA consumes $\approx 92\%$ of the total ADC power which is due to the static currents that always flow in the OTA. Switching on the

Fig. 12 Measured 4096-point FFT spectra with near-DC and near-Nyquist inputs at 1 kS/s.

Fig. 13 Measured SNDR and SFDR at 1 kS/s vs input frequency.

OTA only during the residue amplification phase and disabling it during the rest of the clock cycles can significantly reduce power consumption. Table 1 compares the proposed ADC with other high-resolution pipelined SAR, pipelined and $\Delta\Sigma$ ADCs. The Schreier FoM defined by

$$\text{FoM} = \text{SNDR} + 10 \log\left(\frac{BW}{P}\right) \quad (41)$$

has been used to compare the performance of the ADCs. The proposed ADC achieves a peak FoM of 157.6 dB. Compared to the implementations in 0.35- μm CMOS reported in [10], [20] and [21] this work achieves a superior FoM. The achieved FoM is very competitive in comparison to that of the $\Delta\Sigma$ ADCs in [22], [23] and [24] which have signal bandwidth similar to this work. Featuring an ENOB > 12 bits and power consumption of $6.7\ \mu\text{W}$ in a low-cost CMOS process, the proposed ADC offers an attractive choice for energy-constrained applications such as wireless sensor networks and biomedical implants.

Table 1 Comparison of the ADC with other high-resolution ADCs

	[10]	[25]	[20]	[7]	[21]	[22]	[23]	[24]	This work
CMOS (nm)	350	180	350 (BiCMOS)	130	350	350	180	65	350
Architecture	Pipelined	Pipelined	Pipelined	Pipelined SAR	Pipelined	$\Delta\Sigma$ Order (3)	$\Delta\Sigma$ Order(2)	$\Delta\Sigma$ Order(2)	Pipelined SAR
Resolution (bit)	14	16	14	14	12	-	-	-	15
SNDR (dB)	74	78.6	74	70.4	72.5	65	72	76	78.86
SFDR (dB)	94	96	100	79.6	84.4	-	-	-	91.66
BW (Hz)	37.5E+06	6.25E+06	40E+06	15E+06	10E+06	0.12E+03	0.256E+03	0.5E+03	0.5E+03
Power (W)	318E-03	385E-03	1200E-03	2.54E-03	56.3E-03	0.73E-06	13.3E-06	2.1E-06	6.71E-06
Calibration	No	Yes	No	No	Yes	No	No	No	No
DC gain (dB)	100	-	-	86	90	-	-	-	> 72.3
Area (mm ²)	7.8	15	-	0.24	20.6	0.35	0.51	0.033	0.679
FoM (dB)	154.7	160.7	149.2	168.1	155	147.2	144.8	159.8	157.6

Fig. 14 Measured DNL and INL at 1 kS/s.

6 Conclusion

In this paper, a high-resolution pipelined SAR ADC for low-power, low sampling rate applications was presented. A detailed analysis of the power consumption of the various sub-blocks facilitated the choice of suitable sub-ADC resolutions for the two pipeline stages. By employing substantial inter-stage gain reduction, the specifications of the OTA used in the residue amplifier were relaxed. Appropriate choice of DAC topologies in the sub-ADCs yielded considerable area and power savings by reducing the total capacitance requirement. Prototyped in a 0.35- μm CMOS process, the ADC achieves a competitive FoM among related works while maintaining an ENOB > 12.1 bits upto the Nyquist bandwidth.

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Kairang Chen received the B.Eng. degree in electronics and communication engineering from Guizhou University, China, in 2009, and the M.S. degree in communication engineering from Chongqing University, China, in 2012. Since 2012, he has been pursuing the Ph.D degree in electrical engineering at Linköping University. His research interests include the design of low-power and high-resolution analog-to-digital converters.

Prakash Harikumar received the Master of Science degree in electrical engineering from Linköping University, Sweden in 2011. He is currently working towards the Ph.D degree at the Division of Integrated Circuits and Systems at Linköping University. His research mainly focuses on analog-to-digital converters and analog front-end circuits.

Atila Alvandpour received the M.S. and Ph.D. degrees from Linköping University, Sweden, in 1995 and 1999, respectively. From 1999 to 2003, he was a senior research scientist with Circuit Research Lab, Intel Corporation. In 2003, he joined the department of Electrical Engineering, Linköping University, as a Professor of VLSI design, and currently he is the head of the Integrated Circuits and Systems Division. His research interests include various issues in design of integrated circuits and systems in advanced nano-scale technologies, with special focus on data converters, sensor readout and data acquisition systems, energy-harvesting and power management systems, low-power wireless sensors, and high-performance digital/analog baseband and RF frontends for multi-Gigabit/s radio transceivers. He has published more than 100 papers in international journals and conferences, and holds 24 U.S. patents. Prof. Alvandpour is a senior member of IEEE, and has served as a member of technical program committees for many IEEE and other international conferences, including the IEEE Solid-State Circuits Conference, ISSCC, and the European Solid-State Circuits Conference, ESSCIRC. He has also served as guest editor for IEEE Journal of Solid-State Circuits.