Data retention in organic ferroelectric resistive switches

Vsevolod Khikhlovskyi, Albert J. J. M. van Breemen, Rene A. J. Janssen, Gerwin H. Gelinck
and Martijn Kemerink

Linköping University Post Print

N.B.: When citing this work, cite the original article.

Data retention in organic ferroelectric resistive switches

Authors

Vsevolod Khikhlovskyi, Albert J.J.M. van Breemen, René A.J. Janssen, Gerwin H. Gelinck and Martijn Kemerink

Prof. Dr. M. Kemerink,
E-mail: martijn.kemerink@liu.se
Department of Physics, Chemistry and Biology (IFM),
Linköping University,
P. O. Box SE-581 83 Linköping, Sweden

V. Khikhlovskyi, Prof. Dr. R.A.J. Janssen, Prof. Dr. G.H. Gelinck, Prof. Dr. M. Kemerink
Department of Applied Physics,
Eindhoven University of Technology,
P. O. Box 513, 5600 MB Eindhoven, The Netherlands

Dr. A.J.J.M. van Breemen, Prof. Dr. G.H. Gelinck,
Holst Centre, TNO,
High Tech Campus 31, 5656 AE Eindhoven, The Netherlands

Abstract

Solution-processed organic ferroelectric resistive switches could become the long-missing non-volatile memory elements in organic electronic devices. To this end, data retention in these devices should be characterized, understood and controlled. First, it is shown that the measurement protocol can strongly affect the 'apparent' retention time and a suitable protocol is identified. Second, it is shown by experimental and theoretical methods that partial depolarization of the ferroelectric is the major mechanism responsible for imperfect data retention. This depolarization occurs in close vicinity to the semiconductor-ferroelectric interface, is driven by energy minimization and is inherently present in this type of phase-separated polymer blends. Third, a direct relation between data retention and the charge injection barrier height of the resistive switch is demonstrated experimentally and numerically. Tuning the injection barrier height allows to improve retention by many orders of magnitude in time, albeit at the cost of a reduced on/off ratio.

Corresponding Author

E-mail address: martijn.kemerink@liu.se

1. Introduction

There is an increasing demand for non-volatile memory elements in organic electronics. [1,2] Solution-processed organic ferroelectric resistive switches have recently been proposed as a very promising practical realization of a non-volatile memory that can be read out non-destructively and is compatible with flexible electronics and large area applications.[3,4] The organic ferroelectric resistive switch consists of a thin film made of a polymeric semiconductor-ferroelectric blend sandwiched between two electrodes. The phase separation in the blend is driven by a spinodal decomposition process which results in sub-micron sized semiconductor domains embedded in an insulating ferroelectric matrix.[5-8] Thus, transport of charge carriers, which is needed for the resistive read out, is possible only via the semiconducting phase. The working principle of the resistive switch relies on a modulation of the barrier for charge injection from the metal electrode into the semiconductor by the polarization charges in the ferroelectric.[9,7] This makes it possible to switch the device between high- and low- resistive states. The non-volatility and bistability of the resistive switch stem from the remnant polarization of the ferroelectric part of the blend.

Data retention is a crucial parameter for memory elements. It is known that the depolarization phenomenon that occurs in the ferroelectric is the major factor that harms the device performance.[10] However, the detailed mechanism of information loss, especially at the local scale, is unknown. Moreover, although there are a number of publications in which data retention of organic resistive switches is studied,[11-13] the exact measurement scheme was not always specified. This hampers both comparison between reports and the assessment of the actual relevance for applications.

Here we address the related questions regarding the importance of a well-chosen measurement protocol, the mechanism of the information loss, and ways to mitigate data retention. We show that the data retention is intimately linked to the morphology of the phase-separated polymer blend and is due to polarization loss in a narrow region around the semiconducting domains. From theoretical considerations we show that the polarization in this region is inherently instable. As such, the mechanism governing retention in our devices is fundamentally different from those in ferroelectric-only devices[14,15] and in semiconductor-ferroelectric-metal multilayers.[16,17] Mitigation of this fundamental problem is however possible. We find a direct relation between data retention and the charge injection barrier height of the resistive switch which allows to improve retention by many orders of magnitude in time, albeit at the cost of a reduced on/off ratio.

2. Results and discussion

Figure 1a shows the hysteretic current-voltage (I-V) curve measured on the device fabricated with a P(VDF-TrFE):F8BT 9:1 blend. The contribution from electron transport to the total current is thought to be negligible because of the low electron mobility in F8BT [19] even when the use of Ba as top electrode material warrants a close to ohmic electron injection. A bilayer of 100 nm Au and 1 nm MoOx was chosen as bottom electrode for hole injection. The work-function of this electrode is estimated to be ~5.0 eV [18] because of the presence of MoOx. Since the energy level of the highest occupied molecular orbital (HOMO) of F8BT amounts to 5.9 eV vs. vacuum, the hole injection barrier is of the order of 1 eV. An important advantage of using MoOx is that it was found to prevent the formation of a so-called wetting layer of F8BT – a thin semi-continuous layer of F8BT at the bottom electrode due to a favourable interaction between F8BT and gold. [6] The asymmetry between the positive and negative branches of the I-V curve results from the unequal top and bottom contacts. Without ferroelectric polarization the large charge injection barrier limits hole injection and, therefore, the current in the device is low. However, the injection barrier can be tuned with the assistance of the stray field of the ferroelectric polarization charges.[7, 9] The ascending curve in Figure 1a shows that upon increasing the applied voltage the ferroelectric becomes polarized which consequently lowers the injection barrier, leading to a significant current increase which occurs at around the coercive voltage of +10 V.[20] As the ferroelectric preserves its polarization state when the applied voltage is turned off, the descending part of the I-V curve does not follow the ascending one. Thus the positive part of the I-V sweep demonstrates significant hysteresis behaviour and the device can be programmed to the ON and OFF states. The resistive switch is characterized by the I_{ON}/I_{OFF} ratio of ~10^3, the ratio of the ascending and descending curves, measured at a particular read-out voltage (dashed line in Figure 1a).
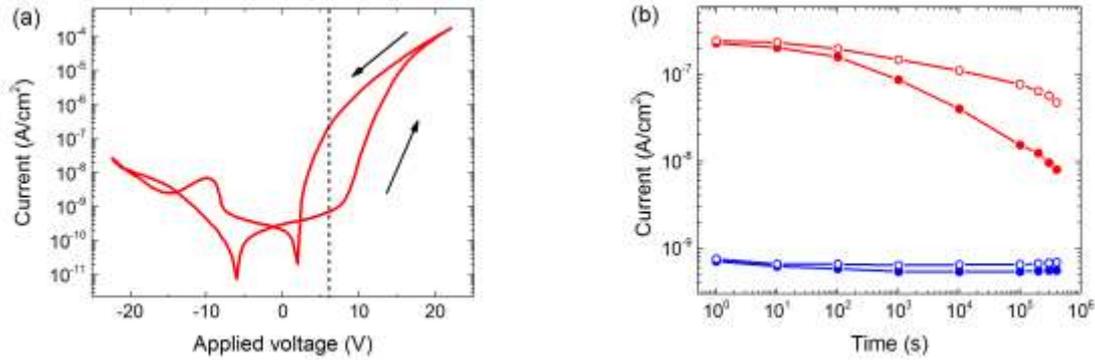
Figure 1. Electrical and memory characteristics of a ferroelectric memory switch fabricated based on a P(VDF-TrFE):F8BT 9:1 blend with Au/MoOx bottom and Ba/Al top electrodes. (a) Hysteretic current-voltage sweep. Arrows indicate the scan direction, the dashed line at 6 V marks the read-out voltage used in the retention measurements in panel b. (b) Data retention. The device was programmed in the ON and the OFF states by applying ± 18.5 V respectively. Red and blue circles represent device current in the ON and the OFF states respectively. Filled and open circles correspond to short-circuit and constant read voltage protocols, respectively (see text).

Retention measurements on the same device were done by programming the device to the ON and OFF states and subsequently monitoring the corresponding I_{ON} and I_{OFF} currents over time at the read-out voltage shown in Figure 1a. It is important to notice that such measurements can be done using at least two different protocols – short-circuit and constant applied voltage respectively. In the former case the read-out voltage is only occasionally applied to the otherwise short circuited device to detect the I_{ON}, I_{OFF} currents. In the latter case the device remains constantly under (read-out) bias. Figure 1b shows the data retention of the device in Figure 1a. An important finding is that the same device appears to show significantly better memory characteristics when characterized in constant read voltage mode. This is because the polarization state of the ferroelectric is partially prevented from the depolarization by the applied field. In contrast, in the short-circuit mode the device is left undisturbed. This method is representative for actual operational conditions in non-volatile memory devices and should therefore be preferably used. It is used in the rest of the text.

The reason that the off-state current in Fig. 1(a) is higher for the constant read voltage protocol (open symbols) than for the short-circuit protocol (closed symbols) is that in the constant read voltage protocol the OFF-state is stabilized by a negative bias (-6 V). When reading at +6V for comparison with the ON-state current, a small transient ionic contribution results. The same ionic current causes the hysteresis in Fig. 1(a). It should be stressed that in all experiments shown herein, the OFF-current is determined by injection and transport in the semiconducting phase and not by leakage through the ferroelectric phase.

In order to understand the underlying mechanism of the information loss the depolarization in the ferroelectric phase of the device was studied using the double-wave method (DWM). In the DWM a sequence of one 'set' and two (identical) 'probe' pulses is applied and the corresponding switching currents are measured[20] (Figure S1 in SI). The set signal is used to set the desired polarization state of the ferroelectric. The probe pulses are used for studying the prepared ferroelectric polarization. The response to the first probing pulse will contain both the (interesting) switching current and the (undesired) leakage and displacement currents. As the response to the second pulse contains only the latter contributions, these can be subtracted to obtain the switching current. The DWM is more accurate when the switching currents are large compared to the background. This condition is met in reverse bias (Figure 1a) – the device demonstrates a low current at the negative voltage. Thus the DWM is applied by first setting the memory to the ON state and therefore switches at reverse (negative) bias where the current is low. By knowing the saturated polarization of the ferroelectric the initial polarization state of the device can be retraced. Figure 2 shows the ascending part of the ferroelectric polarization hysteresis loop measured right after programming the device and after keeping it for 1 day (~10^5 s) at short-circuit conditions. The inset in Figure 2 represents the polarization retention of the ferroelectric capacitor of the same thickness and with the same electrodes. The polarization of the ferroelectric hardly changes during the retention measurements, irrespective of the presence of the semiconductor. The measured ferroelectric polarization is similar to that of the ferroelectric capacitor based on P(VDF-TrFE). In contrast, the I_{ON} current (Figure 1b) decays by at least one

order of magnitude during the same time (~10^5 s). Taking into account that in the ON state charge injection occurs in the vicinity of the semiconductor/ferroelectric interface, the most probable explanation is that only a very small fraction of the ferroelectric, around the semiconductor domains, loses polarization during the data retention measurements. An alternative scenario in which e.g. the semiconductor degrades can be ruled out by the fact that re-poling will bring back the original high-current ON state.
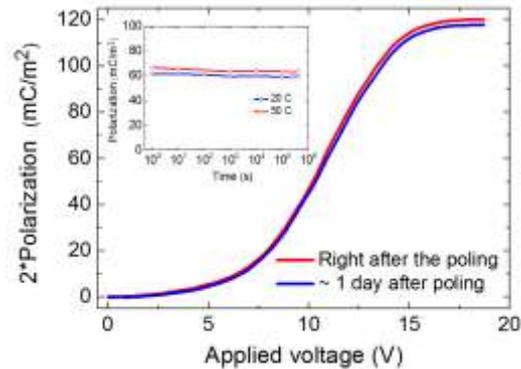

Figure 2. Retention of the ferroelectric part of the resistive switch. Red and blue curves correspond respectively to the ascending part of the ferroelectric hysteresis loop of the Au/MoOx/P(VDF-TrFE):F8BT/Ba/Al measured right after programming and after 1 day (~10^5 s) of keeping the device at short-circuit conditions. Inset: polarization retention of a ferroelectric capacitor, Au/MoOx/P(VDF-TrFE)/Ba/Al, at two different temperatures.

Figure 3 illustrates the proposed depolarization mechanism in the device. The mechanism is tightly related to the (well-established) morphology of these devices;[5-8] see SI for Atomic Force Microscopy images of our devices (Figure S2). We will consider the system's total energy to argue that the polarization of the ferroelectric in close vicinity to the semiconductor is inherently unstable. First, inclusion of a non-ferroelectric (semiconducting) domain in a ferroelectric matrix introduces a domain boundary and a corresponding stray field. The electrostatic
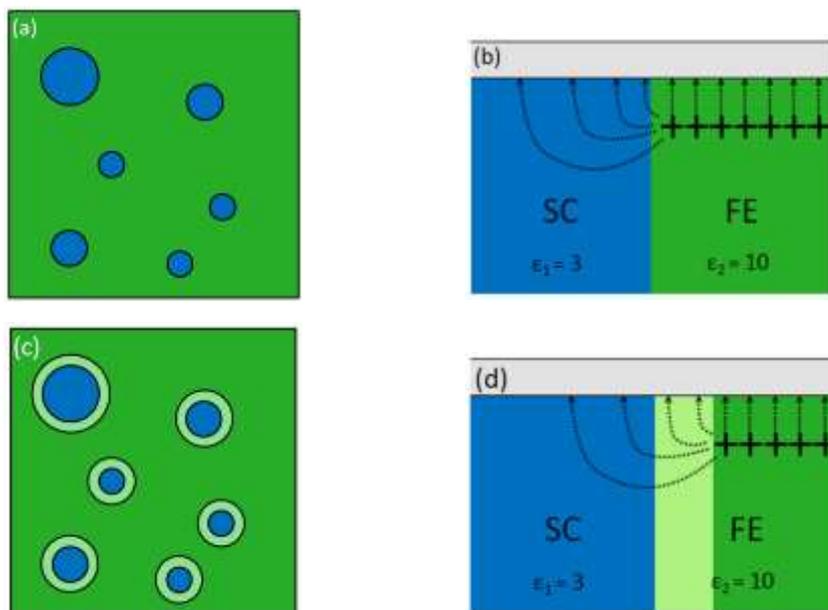

Figure 3. Schematic representation of the relation between the morphology and the depolarization phenomenon in the organic ferroelectric resistive switch. (a) Top view - circular semiconductor domains (blue), are embedded in the insulating ferroelectric matrix (green). (b) Corresponding cross-section, directly after poling. Plus signs indicate polarization charges. Arrows indicate electric fields. (c+d) As (a+b) with partially depolarized ferroelectric phase. Dark (light) green colours corresponds to the polarized (depolarized) ferroelectric regions. The polarization boundary has retracted into the high-dielectric constant region, minimizing total energy. Consequently, current injection, which is driven by the stray field extending into the semiconductor, is reduced.

energy associated with this stray field increases the total energy of the system, and is inversely proportional to the local dielectric constant. Hence there is a driving force for the polarization edge to move away from the semiconductor ($\varepsilon_r \approx 3$) into the ferroelectric ($\varepsilon_r \approx 10$) (Figure 3) due to the minimum energy principle. The driving force for retracting from the semiconductor domains is counteracted by the energy penalty associated with increasing the perimeter of the depolarized area - the latter mechanism is responsible for the instability of inverted domains below a critical size upon polarization reversal of a ferroelectric.[21-24] Growth of the depolarized area is therefore self-limiting. Once the stray field at its perimeter sits predominantly in the ferroelectric phase, there is no longer a driving force for further depolarization. This rationalizes why the vast majority of polarization charge is time-stable (Figure 2) whereas the I_{ON} current, that critically relies on the polarization at the semiconductor/ferroelectric interface, decreases by more than an order of magnitude (Figure 1b): recall that the injection current depends critically on the magnitude of the stray field in the semiconductor.[9]

In order to quantitatively analyze the microscopic depolarization mechanism described above the energy of the organic ferroelectric switch was calculated. As mentioned above there are two contributions to the total energy of the system: the domain wall (DW) energy and the electrostatic (E) energy. Hence the total energy of the simulated system is calculated as[21-23]:

$$W = W_{dw} + W_e \text{,}$$

(1)

where W_{dw} is the domain wall energy of a domain wall of height h, assumed to be equal to the film thickness, and radius r:

$$W_{dw} \approx (2\pi r h)\sigma_{dw}$$

(2)

which is determined by the domain wall energy $\sigma_{dw} \approx 60$ mJ/m^2 of the ferroelectric.[24]

The electrostatic energy W_e is given by:

$$W_e = \frac{1}{2}\int \varepsilon_0 E(\vec{r})D(\vec{r})d^3r$$

(3)

where $E(r)$ is the local electric field and $D(r)$ is the electric displacement; both are calculated using the drift-diffusion model outlined below.

Figure 4 shows the energy of the system depending on the distance between the polarization domain boundary in the ferroelectric and the semiconductor domain (Figure 3d). It is clear from Figure 4 that the total energy of the system crosses a minimum when the width of the depolarized ferroelectric reaches ~20-30 nm, so there is no driving force for further depolarization. The reason that the electrostatic energy term W_e goes down with distance is due to an (im)balance between two components: one related to the field between the polarization charges and their image charges in the metal electrodes, and one component related to the stray field at the polarization edge. The first component gives a positive contribution to the electrostatic energy, so increasing the depolarized area decreases this term. The second component is also a positive term that at larger distances is
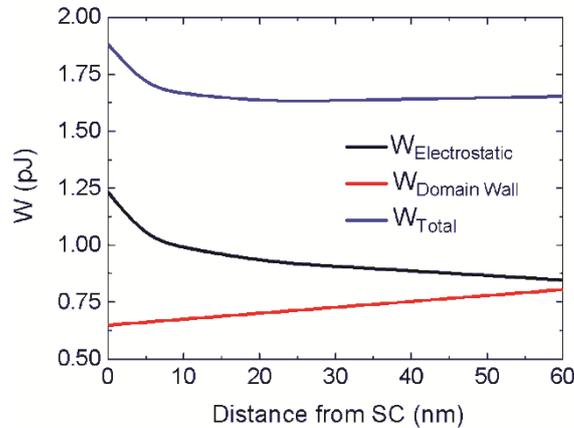

Figure 4. Total energy of a system consisting of a cylindrical semiconductor domain of radius 250 nm surrounded by 250 nm of ferroelectric (see Figure 3). Electrostatic, domain wall and total energy of the system are shown with black, red and blue curves respectively.

linear in the perimeter of the depolarized domain, i.e. increasing the distance increases this term. Since the first term dominates the electrostatic energy decreases far from the interface. However, the term W_{dw} that is associated with the domain wall energy increases with distance and causes the total energy W to increase once the stray field predominantly sits in the ferroelectric phase. Thus the bulk polarization is time stable – in line with the experimental results above.

As the depolarization occurs in a ~20-30 nm rim that is narrow in comparison to typical semiconductor domain sizes of several 100 of nm, the problem is essentially one dimensional and independent of domain size. Moreover, as the amount of injected charge is small compared to the polarization charge densities, the field distributions $E(r)$ and $D(r)$ that enter in Eq. 3 depend, in good approximation, only on the dielectric and ferroelectric properties of the materials. Hence, the shape of the curves in Figure 4 does not significantly depend on mobility, conductivity, energy levels or band gap of the semiconductor. Likewise, trapping effects in both the semiconductor and the ferroelectric [25] are expected to only cause minor quantitative differences due to the fact that the maximum associated charge densities are small compared to the surface polarization charge density in the ferroelectric. Concomitantly the associated depletion lengths are long compared to the relevant length scales in these thin film devices. We also checked that our results are robust in terms of the details of the ferroelectric. For example doubling the distance between the ferroelectric polarization charges and the electrode surface, mimicking the presence of a non-switchable 'dead layer', does not significantly change Figure 4 due to cancelation of (the changes in) the two terms making up W_e. Hence, the most viable method to suppress the driving force for depolarization is to increase the dielectric constant of the semiconductor. Such materials are currently pursued for photovoltaic purposes.[26, 27]

In the considerations above, the metal electrodes enter only as boundary conditions for $E(r)$ and $D(r)$. That means that the presence of a minimum in the total energy of the system does not depend on the choice of electrode: the system is fundamentally unstable. However, the kinetics of the depolarization may still depend on the electrode.[28, 29] This topic is beyond the purposes of the present paper.

Now the mechanism underlying the (partial) depolarization and the associated information loss, as well as its fundamental presence are established, we address the important question on how to mitigate its effects. To this end we compare the measured electrical characteristics of the resistive switches with large (Figure 4a) and small (Figure 4b) injection barriers. Thus, we compare two different polymer semiconductors, F8BT and PTAA, in the same device configuration with Mo/MoOx and MoOx/Ag serving as bottom and top electrodes respectively. The energies of HOMO and LUMO of F8BT amount to 5.9 and 3.3 eV, respectively,[19] the bottom electrode is most likely to provide hole injection into the F8BT over an injection barrier in the order of 1 eV. At the same time electron transport from the top electrode is suppressed. The I_{ON}/I_{OFF} ratio measured at the read-out voltage yields more than two orders of magnitude. Although this ratio is lower than for the memory diode with Ba/Al top contact (Figure 1a), we expect that the former device will be more stable towards oxygen and water degradation, and therefore does not need encapsulation.

To record the data in Figure 5b the same electrodes as in the case of Figure 5a were used, but F8BT was replaced with PTAA. Since for PTAA the HOMO and LUMO levels are at 5.25 and 2.3 eV, respectively,[30] the bottom electrode now provides hole injection into the PTAA over a low injection barrier in the order of 0.25 eV. Electron transport from the top electrode remains suppressed. It is not surprising that such a small injection barrier leads to a low I_{ON}/I_{OFF} ratio, in this case of about 2.5;[9, 31] at the same time, it is not unlikely that this ratio can be significantly improved by proper morphology and composition control.[8] It has to be noted that the difference between I_{ON} and I_{OFF} currents originates truly from the injection barrier modulation and not from spurious effects associated e.g. ionic impurities in the semiconductor. This we ruled out by measuring (hysteresis free) I-V characteristics for a bulk PTAA device with the same electrodes and at the same sweep speed (Figure S3). We also note that the large difference in OFF current between F8BT and PTAA is fully consistent with the differences in injection barrier heights as expected on basis of the simple Schottky model we applied above. [32] Figure 5c and Figure 5d show the data retention of both types of the devices. It is clear that the data retention of the resistive switch with large injection barrier, based on the F8BT, shows a similar trend as in Figure 1. At the same time the PTAA-based device shows a significant improvement as the ON state is hardly affected during the course of the measurement. Figure 6 shows a joint plot of the normalized I_{ON}/I_{OFF} ratio obtained from Figure 5c,d. Intuitively this result can be directly linked to the depolarization phenomenon at the semiconductor/ferroelectric

interface as described in Figure 3. The resistive switch with low injection barriers relies to a much lesser degree on the ferroelectric polarization charges than the one with large injection barriers. At the same time the absolute I_{ON}/I_{OFF} ratio of the F8BT-based device is always greater than the PTAA-based one.
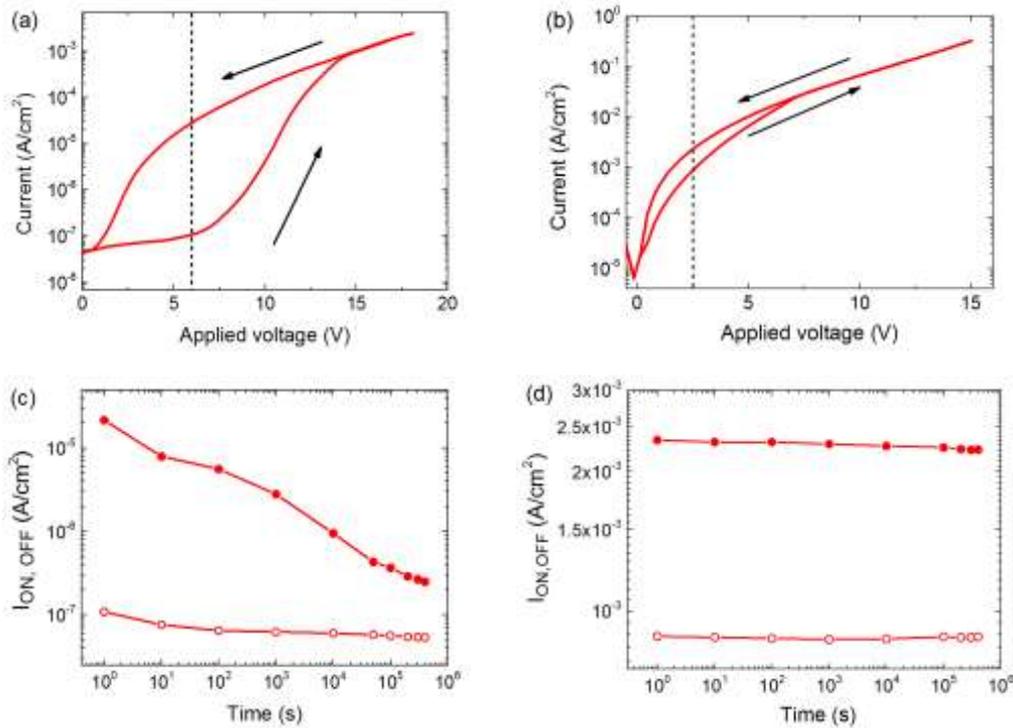

Figure 5. Electrical and memory characteristics of ferroelectric switches. Electrical characteristics of the ferroelectric resistive switch fabricated with: (a) A P(VDF-TrFE):F8BT 9:1 w/w blend with Mo/MoOx (bottom) and MoOx/Ag (top) electrodes. Arrows indicate the scan direction. (b) As (a) with a P(VDF-TrFE):PTAA 9:1 w/w blend. Arrows indicate the scan direction, dashed lines mark the read-out voltage used in the retention data measurements. (c, d) Data retention of the devices in (a) and (b), respectively after programming at $\pm$ 18.5 V (c) and $\pm$ 15 V (d). Filled and open circles represent the device current in the ON and the OFF states respectively.
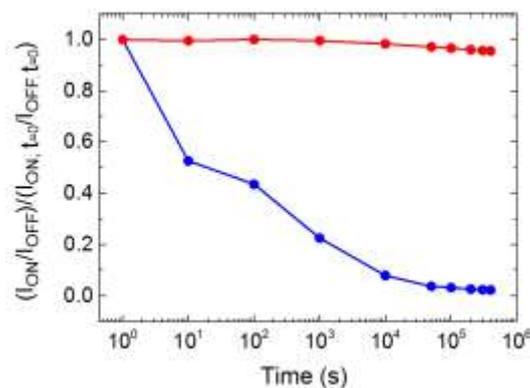

Figure 6. Comparison of the normalized I_{ON}/I_{OFF} ratio as measure for the relative data retention of the ferroelectric resistive switches in Figure 5c,d. Red and blue curves correspond to devices based on the PTAA (low injection barrier) and F8BT (high injection barrier) semiconductors respectively.

We note that the rate of the ON-current reduction in Fig. 5c above is higher than in Fig. 1b. It is tempting to correlate this with the higher ON-current in the former device. A more detailed analysis of the data shows that for both devices the ON-current is space charge limited, indicating the injected majority charge densities are equal and cannot explain the difference. Hence, the difference must be due to the bulk mobility or the effective

area, i.e. the fraction of domains contributing to the current. Especially the latter factor is known to be sensitive to day-to-day variations in processing. An interpretation in terms of differences in minority carrier injection can be ruled out as the device with the expected highest minority carrier injection (Ba/Al top contact) in fact has the lowest ON-current, opposite to what would be expected.

In order to substantiate the interpretation of the measurements presented above a 2D model for the charge transport in the organic ferroelectric switch was employed.[9] The phase separated morphology is simplified to a 2D structure of alternating ferroelectric and semiconducting slabs. Motion of electrons and holes and the electrostatic potential are described by the transport, continuity, and Poisson equations that are numerically

solved on a rectangular grid. The parameters of the blend used in the simulation and the electrical transport model are explained in detail in the Methods section and in the Supporting Information, respectively.

Figure 7a shows calculated absolute I_{ON} and I_{OFF} currents versus the ferroelectric polarization of the resistive switches with injection barriers. As expected the I_{ON}/I_{OFF} ratio of the resistive switch is directly correlated with the injection barrier height. The magnitudes of the ON currents are in good agreement with the experimentally obtained ones; the OFF currents are underestimated due to the absence of leakage in the simulations.[9] More importantly, when the polarization charge density is reduced, corresponding to depolarization in the interfacial areas in the actual experiment (Figure 3), the ON current decreases. This increase is more pronounced and sets in earlier for devices with a high injection barrier, c.f. Figure 5c,d. Figure 7b shows the corresponding normalized I_{ON}/I_{OFF} ratio, its inset shows the absolute I_{ON}/I_{OFF} ratio. Again, reading the polarization charge in the decreasing direction as a measure of time in the experiment, the similarity to Figure 6 is striking. Note in particular that due to the self-limiting nature of the depolarization process, see the discussion at Figure 3, the polarization charge will not vanish completely for long times. Hence from the numerical model a finite retention at long times is expected. Like in the experiment, the I_{ON} current of the device with largest injection barrier is most sensitive to polarization loss but has the largest I_{ON}/I_{OFF} ratio. This means that the cost of longer retention time is a lower I_{ON}/I_{OFF} ratio. This result is in a good agreement with Ref. 3 where good data retention was shown at the low read-out voltage i.e. low I_{ON}/I_{OFF} ratio. Unfortunately a low I_{ON}/I_{OFF} ratio limits the possibility of large scale integration of the resistive switches in simple crossbar arrays[33,34]; when combined with more advanced readout electronics the low-injection barrier devices could, however, form the basis for a stable organic memory.
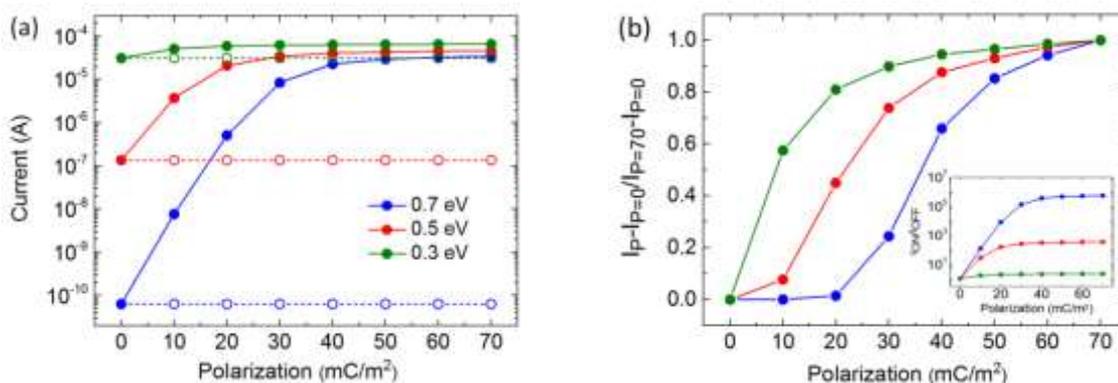

Figure 7. (a) Simulated absolute I_{ON} and I_{OFF} – currents vs. ferroelectric polarization of the resistive switch with different injection barriers (indicated in the figure) into the semiconductor. Solid and dashed lines represent I_{ON} and I_{OFF} currents respectively. (b) Corresponding normalized I_{ON}/I_{OFF} ratio and absolute I_{ON}/I_{OFF}-ratio (inset).

3. Conclusion

In summary, we have studied data retention in organic ferroelectric resistive switches based on phase separated blends of ferroelectric and semiconducting polymers. We show that the data retention is highly dependent on the measurement protocol. Devices measured while being continuously biased at the read-out voltage demonstrate misleading, but significantly better retention due to the fact that the polarization state of the ferroelectric is partially stabilized by the applied voltage. Detailed study of the data retention reveals that partial depolarization of the ferroelectric is the major mechanism responsible for limited data retention. This depolarization occurs mostly in the close vicinity of the semiconductor-ferroelectric interface. We argue, based on theoretical considerations, that the depolarization is driven by an energy minimization process and therefore inherently present in this type of phase-separated polymer blends. We also find a direct relation between the data retention and the charge injection barrier height of the resistive switches. We show by experiments and numerical simulations that the devices with a low injection barrier offer much better data retention than devices with a large injection barrier, albeit at the cost of a reduced on/off ratio. The most viable route to stable data retention in organic ferroelectric resistive switches seems therefore to use a semiconductor with a high (static) dielectric constant, which can suppress or even remove the driving force for depolarization.

4. Materials and methods

Poly[(9,9-di-n-octylfluorenyl-2,7-diyl)-alt-(benzo[2,1,3]thiadiazol-4,8-diyl)] (F8BT) (M_n = 4.9 kDa, D = 1.8) was synthesized according to a modified Suzuki polymerization.[35,36] Poly(bis(4-phenyl)2,3,4-trimethylphenyl)amine (PTAA) (M_n = 17.5 kDa) was purchased from Flexink and used as received. The ferroelectric polymer, Poly(vinylidene fluoride-co-trifluoroethylene) (P(VDF-TrFE)) (M_n = 220 kDa, 2.3 < D < 2.8 with a 77/23 VDF/TrFe ratio) was supplied by Solvay Specialty Polymers. Blend solution of P(VDF-TrFE):F8BT was prepared by co-dissolving P(VDF-TrFE) and F8BT (9:1 w/w) in a mixture of cyclohexanone and tetrahydrofuran 75:25 (v/v) at 50 °C overnight (50 mg mL^{-1}). P(VDF-TrFE):PTAA solution was prepared with the same ratio according to the same recipe with a single solvent cyclohexanone. Cleaned glass substrates with lithographically patterned Au/MoOx and Mo/MoOx contact electrodes of 0.44 mm^2 were used. Blend films were then spin coated in a nitrogen-filled glove box. The average film thickness was measured with a DEKTAK profilometer and found to be ~200 ± 10 nm. Subsequently, the samples were annealed at 135 °C for 1 hour followed by the deposition of the corresponding Ba/Al or MoOx/Au top electrode. Ferroelectric capacitors with Au/MoOx and Ba/Al electrodes were made according to the same fabrication recipe mentioned above using the same solvent mixture as for P(VDF-TrFE):F8BT. In electrical characterization experiments, the indicated biases are applied to the (MoOx) bottom electrode w.r.t. the top electrode.

The 2D drift-diffusion model used for simulating the ferroelectric-driven organic resistive switches takes into account the phase separated morphology, which is approximated by alternating slabs of ferroelectric and semiconductor materials such that both materials are always in contact with both electrodes. Zero mobility is assumed for the electrically insulating ferroelectric P(VDF-TrFE). In the ferroelectric slab a surface polarization charge density $\sigma_p \approx$ 70 mC/m^2 and a static relative dielectric constant ε_r = 10 were used. The organic semiconducting slabs were characterized by a typical (constant) hole mobility, μ_p = 6.5 × 10^{-11} m^2 V^{-1} s^{-1}, and ε_r = 3. A field-dependent charge injection into the semiconductor over a barrier of finite height is implemented by using the Emtage/O'Dwyer model.[37,38] Further details on the model can be found in.[7,9]

References

1. J.S. Meena, S.M. Sze, U.C. and T.-Y. Tseng, *Nanoscale Res. Lett.* **2014**, *9*, 526.
2. S.-T. Han, Y. Zhou, and V.A.L. Roy, Adv. Mater. **2013**, *25*, 5425–5449.
3. K. Asadi, D. M. de Leeuw, B. de Boer and P.W.M. Blom, *Nat. Mater.* **2008**, *7*, 547-550.
4. A.J.J.M. van Breemen, J.-L. van der Steen, G. van Heck, R. Wang, V. Khikhlovskyi, M. Kemerink, and G.H. Gelinck, *Appl. Phys. Express* **2014**, *7*, 031602.
5. K. Asadi, H.J. Wondergem, R.S. Moghaddam, C.R. McNeill, N. Stingelin, B. Noheda, P.W. M. Blom, and D.M. de Leeuw, *Adv. Funct. Mater.* **2011**, *21*, 1887.
6. V. Khikhlovskyi, A.J.J.M. van Breemen, J.J. Michels, R.A.J. Janssen, G.H. Gelinck, M. Kemerink, *J Polym. Sci. Pol. Phys.* **2015**, *53*, 1231–1237.
7. V. Khikhlovskyi, R. Wang, A.J.J.M. van Breemen, G.H. Gelinck, R.A.J. Janssen, and M. Kemerink, *J. Phys. Chem. C* **2014**, *118*, 3305.
8. A.J.J.M. van Breemen, T. Zaba, V. Khikhlovskyi, J. Michels, R. Janssen, M. Kemerink, and G. Gelinck, Surface Directed Phase Separation of Semiconductor Ferroelectric Polymer Blends and their Use in Non-Volatile Memories, *Adv. Funct. Mater.* **2015**, *25*, 278–286.
9. M. Kemerink, K. Asadi, P.W.M. Blom, D.M. de Leeuw, *Org. Electron.* **2012**, *13*, 147−152.
10. K. Asadi, J. Wildeman, P.W.M. Blom, and D.M. de Leeuw, *IEEE T Electron Devices* **2010**, *57*.
11. M.A. Khan, U.S. Bhansali, D. Cha, and H.N. Alshareef, *Adv. Funct. Mater.* **2013**, *23*, 2145–2152.
12. J. Hu, J. Zhang, Z. Fu, J. Weng, W. Chen, S. Ding, Y. Jiang, and G. Zhu, *ACS Appl. Mater. Interfaces* **2015**, *7*, 6325−6330.
13. S.H. Sung and B.W. Boudouris, *ACS Macro Lett.* **2015**, *4*, 293−297.
14. X. Zhang, H. Xu and Y. Zhang, *J. Phys. D: Appl. Phys.* **2011**, *44*, 155501-155507.

15. G.D. Zhu, Z.G. Zeng, L. Zhang, X.J. Yan, *J. Appl. Polym. Sci.* **2008**, *107*, 3945–3949.

16. R.C.G. Naber, K. Asadi, P.W.M. Blom, D.M. de Leeuw, and B. de Boer, *Adv. Mater.* **2010**, *22*, 9, 933–945.

17. R.C.G. Naber, M. Mulder, B. de Boer, P.W.M. Blom, D.M. de Leeuw, *Org. Electron.* **2006**, *7*, 132.

18. S. Chen, J.R. Manders, S.-W. Tsang and F. So, *J. Mater. Chem.* **2012**, *22*, 24202.

19. Y. Zhang and P.W.M. Blom, *Appl. Phys. Lett.* **2011**, *98*, 143504.

20. V. Khikhlovskyi, A.V. Gorbunov, A.J.J.M. van Breemen, R.A.J. Janssen, G.H. Gelinck, M. Kemerink, *Org. Electron.* **2013**, *14*, 3399–3405.

21. I. Lukyanchuk, P. Sharma, T. Nakajima, S. Okamura, J.F. Scott, and A. Gruverman, *Nano Lett.* **2014**, *14*, 6931−6935.

22. A.A. Thiele, *Bell System Techn. J.* **1969**, *48*, 3287.

23. A.A. Thiele, *Bell System Techn. J.* **1971**, *50*, 711.

24. W.J. Hu, D.-M. Juo, L. You, J. Wang, Y.-C. Chen, Y.-H. Chu & T. Wu, *Sci. Rep.* **2014**, *4*, 4772.

25. L. Pintilie, Charge Transport in Ferroelectric Thin Films, Ferroelectrics - Physical Effects, Dr. Mickaël Lallart (Ed.), ISBN: 978-953-307-453-5, **2011**.

26. S. Torabi, F. Jahani, I. Van Severen, C. Kanimozhi, S. Patil, R.W.A. Havenith, R.C. Chiechi, L. Lutsen, D.J.M. Vanderzande, T.J. Cleij, J.C. Hummelen, and L.J.A. Koster, *Adv. Funct. Mater.* doi: 10.1002/adfm.201402244.

27. L. J. A. Koster, S. E. Shaheen, J. C. Hummelen, *Adv. Energy Mater.* **2012**, *2*, 1246

28. R. C. G. Naber, P. W. M. Blom, A. W. Marsman, and D. M. de Leeuw, *Appl. Phys. Lett.* **2004**, *85*, 2032.

29. H. Xu, J. Zhong, X. Liu, and J. Chen, D. Shen, Appl. Phys. Lett. **2007**, *90*, 092903.

30. A. Intaniwet, C.A. Mills, P.J. Sellin, M. Shkunov, and J.L. Keddie, *Appl. Mater. Inter.* **2010**, *2*, 6, 1692–1699.

31. K. Asadi, T.G. de Boer, P.W.M. Blom, D.M. De Leeuw, *Adv. Funct. Mater.* **2009**, *19*, 3173.

32. C. Tengstedt, W. Osikowicz, W. R. Salaneck, I. D. Parker, C.-H. Hsu and M. Fahlman, *Appl. Phys. Lett.* **2006**, *88*, 053502.

33. N. Pimparkar, Q. Cao, J. A. Rogers, and M.A. Alam, *Nano Res.* **2009**, *2*, 167 175.

34. W.A. Goddard III, D. Brenner, S.E. Lyshevski, G.J. Iafrate, *Handbook of Nanoscience, Engineering, and Technology*, Third Edition, **2012**, *11-25*, CRC Press.

35. T. van Woudenbergh, J. Wildeman, P.W.M. Blom, J.J.A.M. Bastiaansen, B.M.W. Langeveld-Voss, *Adv. Funct. Mater.* **2004**, *14*, 677.

36. N. Miyaura, A. Suzuki, *Chem. Rev.* **1995**, *96*, 2457.

37. P.R. Emtage, J.J. O'Dwyer, *Phys. Rev. Lett.* **1966**, *16*, 356−358.

38. J.J.M. van der Holst, M.A. Uijttewaal, R. Balasubramanian, R. Coehoorn, P.A. Bobbert, G.A. de Wijs, R.A. de Groot, *Phys. Rev. B* **2009**, *79*, 085203.

Data retention in organic ferroelectric resistive switches is characterized, understood and controlled. Imperfect data retention results from partial depolarization near the ferroelectric-semiconductor interface. The retention time can be improved by orders of magnitude by tuning the injection barrier height, albeit at the cost of a reduced on/off ratio.

Memories, data retention, resistive switching, organic electronics, ferroelectrics

Vsevolod Khikhlovskyi, Albert J.J.M. van Breemen, René A.J. Janssen, Gerwin H. Gelinck and Martijn Kemerink

Data retention in organic ferroelectric resistive switches