

Design of a Low Power Cyclic/Algorithmic Analog- to-Digital Converter in a 130nm CMOS Process

IMST GmbH
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Design of a Low Power Cyclic/Algorithmic Analog-to-Digital Converter in a 130nm CMOS Process

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by

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Sammanfattning Abstract <p>Analog-to-digital converters are inevitable in the modern communication systems and there is always a need for the design of low-power converters. There are different A/D architectures to achieve medium resolution at medium speeds and among all those Cyclic/Algorithmic structure stands out due to its low hardware complexity and less die area costs. This thesis aims at discussing the ongoing trend in Cyclic/Algorithmic ADCs and their functionality. Some design techniques are studied on how to implement low power high resolution A/D converters. Also, non-ideal effects of SC implementation for Cyclic A/D converters are explored. Two kinds of Cyclic A/D architectures are compared. One is the conventional Cyclic ADC with RSD technique and the other is Cyclic ADC with Correlated Level Shift (CLS) technique. This ADC is a part of IMST Design + Systems International GmbH project work and was designed and simulated at IMST GmbH.</p> <p>This thesis presents the design of a 12-bit, 1 Msps, Cyclic/Algorithmic Analog-to-Digital Converter (ADC) using the "Redundant Signed Digit (RSD)" algorithm or 1.5-bit/stage architecture with switched-capacitor (SC) implementation. The design was carried out in 130nm CMOS process with a 1.5 V power supply. This ADC dissipates a power of 1.6 mW when run at full speed and works for full-scale input dynamic range. The op-amp used in the Cyclic ADC is a two-stage folded cascode structure with Class A output stage. This op-amp in typical corner dissipates 631 uW power at 1.5 V power supply and achieves a gain of 77 dB with a phase margin of 64° and a GBW of 54 MHz at 2 pF load.</p>

Nyckelord Redundant Signed Digit, Correlated level Shifting, Low power, High Speed, Folded cascode
--

ABSTRACT

Analog-to-digital converters are inevitable in the modern communication systems and there is always a need for the design of low-power converters. There are different A/D architectures to achieve medium resolution at medium speeds and among all those Cyclic/Algorithmic structure stands out due to its low hardware complexity and less die area costs. This thesis aims at discussing the ongoing trend in Cyclic/Algorithmic ADCs and their functionality. Some design techniques are studied on how to implement low power high resolution A/D converters. Also, non-ideal effects of SC implementation for Cyclic A/D converters are explored. Two kinds of Cyclic A/D architectures are compared. One is the conventional Cyclic ADC with RSD technique and the other is Cyclic ADC with Correlated Level Shift (CLS) technique. This ADC is a part of IMST Design + Systems International GmbH project work and was designed and simulated at IMST GmbH.

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TABLE OF CONTENTS

1	INTRODUCTION.....	1
1.1	MOTIVATION.....	1
1.2	THESIS ORGANIZATION.....	3
2	ADC PERFORMANCE CHARACTERISTICS.....	4
2.1	GENERAL CHARACTERISTICS OF ADC.....	4
2.2	STATIC CHARACTERISTICS OF ADC.....	5
2.2.1	<i>Offset and gain errors.....</i>	5
2.2.2	<i>Differential non-linearity error.....</i>	5
2.2.3	<i>Integral non-linearity error.....</i>	6
2.3	DYNAMIC CHARACTERISTICS OF ADC.....	6
2.3.1	<i>Signal-to-Noise ratio.....</i>	6
2.3.2	<i>Signal-to-Noise and Distortion ratio.....</i>	7
2.3.3	<i>Total Harmonic Distortion.....</i>	7
2.3.4	<i>Effective Number of Bits.....</i>	7
2.3.5	<i>Dynamic Range.....</i>	8
2.3.6	<i>Spurious-Free Dynamic Range.....</i>	8
2.4	SUMMARY.....	8
3	INTRODUCTION TO CYCLIC/ALGORITHMIC ADC.....	9
3.1	VARIOUS ADC ARCHITECTURES.....	9
3.2	CYCLIC/ALGORITHMIC ADC.....	10
3.2.1	<i>Operation of Cyclic ADC.....</i>	10
3.2.2	<i>Offset Effects on the Residue.....</i>	13
3.3	SUMMARY.....	14
4	RSD CYCLIC A/D CONVERTER.....	15
4.1	RSD ALGORITHM.....	15
4.2	TYPICAL IMPLEMENTATION OF RSD CYCLIC ADC.....	17
4.3	DIFFERENT NON-LINEARITIES.....	19
4.3.1	<i>Capacitor Mismatch errors.....</i>	19
4.3.2	<i>Thermal Noise.....</i>	20
4.3.3	<i>Finite Gain Errors of OTAs.....</i>	21
4.3.4	<i>Analog Switch Non-idealities.....</i>	22
4.3.5	<i>Correlated Level Shift Technique.....</i>	23
4.4	SUMMARY.....	24
5	CIRCUIT LEVEL IMPLEMENTATION.....	26
5.1	TWO-PHASE NON-OVERLAPPING CLOCK GENERATOR.....	26
5.1.1	<i>Clock Generator Design.....</i>	27
5.1.2	<i>Clock Generator Simulation Results.....</i>	27
5.2	SUB-ADC DESIGN.....	28
5.2.1	<i>Differential Comparator.....</i>	28
5.2.2	<i>Voltage Comparator.....</i>	30

5.2.3	<i>Comparator Simulation Results</i>	30
5.3	DAC SWITCH.....	32
5.4	SAMPLE-AND-HOLD STAGE.....	33
5.4.1	<i>Operational Amplifier</i>	34
5.4.2	<i>Op amp Simulation Results</i>	38
5.5	RESIDUAL AMPLIFIER/GAIN STAGE.....	43
5.6	SUMMARY.....	44
6	CIRCUIT PERFORMANCE	45
6.1	SUMMARY.....	49
7	CONCLUSION AND FUTURE WORK	51
7.1	CONCLUSION.....	51
7.2	FUTURE WORK.....	51
8	BIBLIOGRAPHY	53

LIST OF FIGURES

Figure 2-1 Ideal input-output characteristics of a 3-bit ADC	4
Figure 2-2 Quantization noise for a 3-bit ADC.....	5
Figure 2-3 Offset errors for a 3-bit ADC.....	6
Figure 2-4 gain error for a 3-bit ADC.....	6
Figure 2-5 INL and DNL errors for a 3-bit ADC.....	7
Figure 3-1 Conversion time vs Resolution for different ADC architectures (Sansen)	10
Figure 3-2 Generic Block Diagram of the cyclic ADC.....	11
Figure 3-3 Conventional Cyclic Converter flow chart.....	12
Figure 3-4 Residue Plot of a 1-bit/stage Cyclic ADC.....	13
Figure 3-5 Comparator Offset in Conventional Cyclic ADC.....	13
Figure 3-6 Loop Offset Error in Conventional Cyclic ADC.....	14
Figure 4-1 RSD Cyclic Converter Flow Chart.....	15
Figure 4-2 Residue Plot of a 1.5-bit/stage Architecture.....	16
Figure 4-3 Residue Plot with Comparator Offset at $-V_{ref}/2$	17
Figure 4-40 Residue Plot of a 1.5-bit/stage Architecture with Loop Offset Error .	17
Figure 4-5 Single Ended Implementation of RSD Cyclic ADC	18
Figure 4-6 Residual Amplifier showing CLS Technique	23
Figure 4-7 Clock Phases Required to Employ CLS Technique	24
Figure 5-1 Non-Overlapping Clock Phase Generator Design Block.....	26
Figure 5-2 Clock phases showing phases used to implement CLS Technique	27
Figure 5-3 Clock Phases showing phase required to implement Bottom-plate Sampling	28
Figure 5-4 Differential Comparator to generate the threshold levels $+V_{ref}/4$ and $-V_{ref}/4$	29
Figure 5-5 Pre-amplification stage of the Voltage Comparator.....	30
Figure 5-6 Decision-making Stage of the Voltage Comparator.....	31
Figure 5-7 Voltage Comparator Simulation Results.....	31
Figure 5-8 Offset Voltage Simulation to find Standard Deviation of the voltage comparator.....	32
Figure 5-9 DAC switch to Calculate the Analog Voltages for the Residual Amplifier	33
Figure 5-10 Schematic of SHA without using CLS Technique.....	34
Figure 5-11 Schematic of SHA using CLS technique	35
Figure 5-12 Biasing circuit of the Folded-cascode op-amp with class A output stage	35
Figure 5-13 Folded-Cascode op amp with Class A Output Stage.....	36
Figure 5-14 Folded-cascode op-amp with Class AB output stage.....	37
Figure 5-15 Biasing Circuit of the Folded-cascode op-amp with Class AB output stage.....	38
Figure 5-16 Continuous-time CMFB Circuit.....	39
Figure 5-17 Gain and Phase Plots of Folded-cascode op amp with class A output stage.....	40

Figure 5-18 Gain and Phase Plots of Folded-cascode op amp with class AB output stage.....	40
Figure 5-19 Graph showing Slew rate and Settling time of Folded-cascode op amp with class A output stage.....	41
Figure 5-20 Graph showing Slew rate and Settling time of Folded-cascode op amp with class AB output stage.....	41
Figure 5-21 Two stage Folded-cascode op-amp with class AB output stage simulation results at the corners.....	42
Figure 5-22 Two stage Folded-cascode op-amp with class A output stage simulation results at the corners.....	42
Figure 5-23 Schematic of Residual Amplifier without using CLS Technique.....	43
Figure 6-1 Simulation Result (From Top: Conversion Result, SHA Residue, RA Residue) -of RSD cyclic ADC with an input of 100 mV@100 Ksps without CLS Technique.....	45
Figure 6-2 Simulation Result of Cyclic ADC with an input of 900 mV@100 Ksps without CLS Technique.....	46
Figure 6-3 Simulation Result of RSD cyclic ADC with an input of 400 mV@1 Msps without CLS Technique.....	46
Figure 6-4 Simulation Result of RSD cyclic ADC with an input of 900 mV@100 Ksps with CLS Technique.....	47
Figure 6-5 Simulation Result of RSD cyclic ADC with an input of -600 mV@1 Msps with CLS Technique.....	47
Figure 6-6 Corners Simulation Result of RSD cyclic ADC with an input of 100 mV@100 Ksps without CLS Technique.....	48
Figure 6-7 Corners Simulation Result of RSD cyclic ADC with an input of 100 mV@100 Ksps with CLS Technique.....	49
Figure 6-8 Corners Simulation Result of RSD cyclic ADC with an input of 100 mV@1 Msps without CLS Technique.....	50

LIST OF TABLES

Table 1-1 Table of Specifications.....	1
Table 3-1 Various ADC Architectures	9
Table 5-1 Output Calculation in Differential Comparator.....	29
Table 5-2 Operation of DAC Switch	33
Table 5-3 Simulated Op amp Parameters	39
Table 6-1 Table showing the Simulation Results comparison between conventional and RSD cyclic ADCs.....	50

LIST OF ABBREVIATIONS AND SYMBOLS

Abbreviation	Spell-out	Reference
β	Feedback factor	Ch. 4
τ	Time Constant	Ch. 4
A_v	Open loop DC gain	Ch. 4
A/D	Analog-to-Digital	Ch. 1
ADC	Analog-to-Digital Converter	Ch. 2
C_f	Feedback Capacitor	Ch. 4
C_s	Sampling Capacitor	Ch. 4
C_{ld}	Load capacitor	Ch. 4
C_{ls}	Level Shift capacitor	Ch. 4
C_{f_RA}	Feedback capacitor of RA	Ch. 4
C_{f_SHA}	Feedback capacitor of SHA	Ch. 4
C_{s_RA}	Sampling capacitor of RA	Ch. 4
C_{s_SHA}	Sampling capacitor of SHA	Ch. 4
CLS	Correlated-Level Shift	Ch. 4
CMFB	Common-mode Feedback Circuit	Ch. 5
CMOS	Complementary Metal Oxide Semiconductor	Ch 5
DAC	Digital-to-Analog Converter	Ch. 5
DNL	Differential Non Linearity	Ch. 2
ENOB	Effective number of Bits	Ch. 2
f_{3-dB}	Closed loop 3-dB frequency	Ch. 4
f_s	Sampling frequency	Ch. 4
FFT	Fast Fourier Transform	Ch.2
FS	Full-Scale	Ch. 2
G	Closed loop gain	Ch. 4
GBW	Gain bandwidth Product	Ch. 4
INL	Integral Non Linearity	Ch. 2
k	Boltzmann's constant	Ch. 4
LSB	Least Significant Bit	Ch. 2
MSB	Most Significant Bit	Ch.2
N	Resolution of ADC	Ch. 1
Op amp	Operational Amplifier	Ch. 5
q	Quantization	Ch. 2
rms	Root Mean Square voltage	Ch. 2
RA	Residue Amplifier	Ch. 4
RSD	Redundant Signed Digit	Ch. 1
SAR	Successive Approximation Register	Ch. 3
SC	Switched Capacitor	Ch. 1
SHA	Sample-and-Hold Amplifier	Ch. 3
SNR	Signal-to-Noise Ratio	Ch. 2
t_s	Settling Time	Ch. 4
T	Temperature in Kelvin	Ch. 4
THD	Total Harmonic Distribution	Ch. 2

UGF	Unity gain Frequency	Ch. 4
V_{cm}	Common-mode voltage	Ch. 5
V_{dac}	Reference voltage	Ch. 4
V_{fs}	Full scale voltage	Ch. 3
V_{in}	Input voltage	Ch. 3
v_n	Noise voltage	Ch. 3
V_{out}	Output voltage	Ch. 3
V_{ref}	Reference voltage	Ch. 3
V_{refm}	Positive reference voltage	Ch. 4
V_{refn}	Negative reference voltage	Ch. 4

1 INTRODUCTION

Analog to Digital Converters acts as an interface between the analog real world and the digital world. They are inevitable in most of the applications employing electronic systems such as multimedia, mobile communications.etc,. An ADC executes three distinct operations, sampling the continuous amplitude and time signals, quantizing the sampled signal and finally assigning a digital code to the related quantized output.

1.1 MOTIVATION

In recent times there has been an increasing demand for ADCs with high speed, high resolution, smaller size and low power dissipation. Sensor applications like digital voltmeters, pressure or temperature sensors require ADCs with high resolutions where as battery-powered sensors need lower power dissipations. The portable media and wireless systems, now-a-days, due to their smaller device dimensions resulted in a rapid growth in the performance of integrated devices. Due to the down-scaling of such devices, there is a need for the reduction in the power consumption. This in turn necessitates the circuits to operate on reduced supply voltages. However, this might result in the limitation of achievable dynamic range of the analog circuitry. Also, noise along with the reduced supply voltages is an important factor that can degrade the signal power. This causes an increased power consumption of the circuit. Therefore, there is a need to design the analog circuits with lower supply voltages while maintaining the desired levels of performance.

There are various ADC architectures, that are later discussed, that can satisfy low power needs. To achieve lower power and high resolution ADC architectures employ switched capacitor circuits which are very popular in recent times. But SC circuits suffer from many non ideal effects such as offset errors in op-amp and comparators, charge injection in analog switches.etc,.

Process Technology	130 nm
Resolution	12-bits
Conversion Rate	Up to 1 Msps
Input Frequency	Up to 450 kHz
Power Supply	1.5 V
Reference Voltage	1 V
Power Consumption	1 mW @1 Msps
Input Range	-1 V to +1 V

Table 1-1 Table of Specifications

There are various techniques to compensate these effects. Among the many approaches Cyclic/successive approaches are well known to achieve medium resolution for small die area and low hardware complexity. This thesis presents a Cyclic/Algorithmic ADC employing Redundant Signed Digit (RSD) technique to achieve low power, medium resolution while eliminating the non ideal effects of SC circuits.

This thesis work primarily concentrates on building a Cyclic ADC that can have a resolution of 12-bits at conversion rates around 1 MHz. This ADC is to be built in a 130nm CMOS process with a power supply of 1.5 V. The ADC must be flexible in operating at rails. So, the output must operate rail-to-rail. The primary task at the beginning is to select a suitable architecture for cyclic ADC that can satisfy the above specifications. Various methods were looked into, but due to the time constraint the most traditional method CLS method was chosen. CLS method of developing the Cyclic ADC was looked into because this method was previously implemented on pipelined ADCs. Design of op-amps and comparator for the ADC was not considered as there were some models already available. But due to the adoption of RSD method for cyclic ADC, new models for the op-amp and comparator has to be developed. This is due to the fact that the previous model op-amp has a gain less than 46 dB that is not sufficient to implement RSD method. Also the previous comparator model has an offset problem and so a new voltage comparator has to be designed. Apart from these, a new non-overlapping clock phase generator has to be designed that can support both the RSD and CLS methods of implementation.

Most of the papers on Cyclic ADC had been concentrating on medium speeds up to 5 Msps. Achieving those speeds may require a two-stage RSD architecture (Choi, 2009) or some other special techniques like Digital calibration.etc., The paper by (Li, Ahn, Chang, & Moon, 2005; Gumenyuk & Bocharov, 2007) suggests the design of a 12-bit Algorithmic ADC at the conversion speeds of 5 Msps at 30 MHz clocking and a power consumption of 12 mW. To ensure high linearity and low-voltage operation, a resistor-based input sampling branch is employed. Also, a background calibration technique is proposed to mitigate capacitor mismatches and finite op-amp gain error in the MDAC stages. This is done via novel digital correction scheme involving two-channel ADC architecture.

The paper by (Kim, 2009) suggests an 11-bit Algorithmic ADC at speeds of 10 Msps at a power consumption of 10.5 mW. This ADC also employs two-stage RSD architecture and also several techniques like amplifier sharing, DC offset cancellation, and input memory effect suppression, resulting in reduced area and power, and high linearity.

Most of the other papers achieve very low speeds below 500 Ksps. The main constraint for achieving high speeds is the power consumption. But in the present thesis, the main challenge is to achieve medium speeds at a moderate power consumption which is tricky. This may require some special techniques to be adopted. But the specifications were checked by using conventional architecture making the requirements to be met much more difficult. There are many non idealities that are to be mitigated. But due to the time constraint the basic architecture have been tried out.

Most part of this thesis is influenced by (Abo, 1999) (Delic-Ibukic, 2004) (Sokalingam & Thibodeau, 2002) (Hai, 2011) (Atris, 2007). The underlying concept about Cyclic ADCs was studied from (Atris, 2007) and (Hai, 2011). A lot was learnt from these PhD theses about the operating principles and functioning of the ADC. The design of most of

the blocks in the ADC was influenced from (Abo, 1999) (Sockalingam & Thibodeau, 2002) and (Delic-Ibukic, 2004).

1.2 THESIS ORGANIZATION

This thesis comprises of eight chapters. Each chapter presents step-by-step insight into the design of Cyclic ADC while discussing various issues like non-idealities and compensation techniques. Two different architectures of cyclic converters are compared and simulation results were also shown for both the architectures.

Chapter 2 is a review of different performance metrics of ADCs that gives an extensive overview of analog to digital converters terminology.

Chapter 3 introduces the basic 1-bit/stage cyclic converter showing its vulnerability to different non-idealities. It also gives a brief overview of different analog to digital converter architectures.

Chapter 4 gives an in-depth coverage of a specific ADC architecture, namely RSD Cyclic ADC, also known as 1.5-bit/stage architecture. It also discusses different non-ideal errors associated with the design and gives the possible solutions to combat those errors. Also a possible implementation of the RSD converter is shown. Along with these details, a new technique called Correlated Level Shift is introduced as an alternative for conventional RSD technique.

Chapter 5 discusses the circuit level design of the discussed architectures. It focuses on the design and simulation results of different blocks involved in the design of a RSD Cyclic converter. The blocks used in the design of CLS RSD Cyclic converter are also discussed.

Chapter 6 shows the circuit performance for the given specifications. Both the architectures previously discussed were tested and the simulation results are shown.

Chapter 7 concludes with a brief summary of the design process and results of this thesis and also indicates the possible future work that can be carried out.

2 ADC PERFORMANCE CHARACTERISTICS

This chapter discusses various parameters that determine the performance of ADC. The performance of an ADC can be illustrated through

- a) General Characteristics
- b) Static Characteristics
- c) Dynamic Characteristics

The above metrics model the errors in an ADC and can analyze the performance.

2.1 GENERAL CHARACTERISTICS OF ADC

The transfer characteristic of the ADC represents the relation between the input samples and its corresponding output code. For an ideal ADC, the transfer characteristic is a uniform staircase function. The transfer function of an ideal 3-bit converter is shown below.

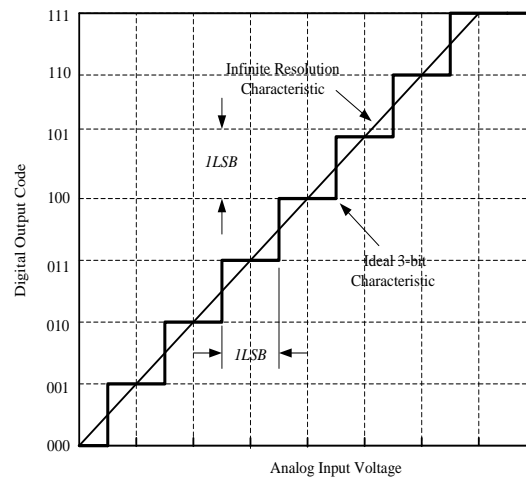


Figure 2-1 Ideal input-output characteristics of a 3-bit ADC

The quantization step (q) is given by

$$q = \frac{FS}{2^N} = 1 \text{ LSB} \quad (2.1)$$

Where, FS is full scale representing difference between the maximum and minimum voltage of the input. N is the resolution of the converter representing the number of bits in the digital output.

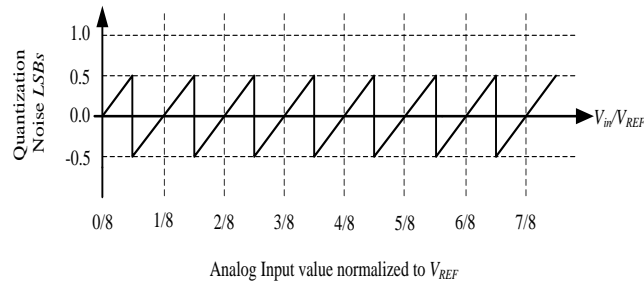


Figure 2-2 Quantization noise for a 3-bit ADC

Quantization noise is the error that occurs when the signal is converted into digital output. The quantization noise is the plot of the difference between the infinite resolution characteristic and ideal 3 bit characteristic as a function of the input voltage. For an ideal ADC the quantization noise lies between ± 0.5 LSB. The above plot shows the quantization noise as a function of the input (Allen & Holberg, 2002).

2.2 STATIC CHARACTERISTICS OF ADC

Static characteristics are related to the comparison of the ideal conversion characteristics with the measured ones. The primary characteristics that determine the static performance of ADCs are offset and gain errors, Integral non-linearity error (INL) and Differential non-linearity error (DNL).

2.2.1 OFFSET AND GAIN ERRORS

The horizontal difference between the real straight line obtained from the measured ADC and the infinite resolution characteristic of ideal ADC that passes through the origin is called the offset error.

Gain error is simply the change in the slope between the infinite resolution line and the actual measured line. This error is expressed as a percentage.

2.2.2 DIFFERENTIAL NON-LINEARITY ERROR

DNL of the ADC is defined as the measure of the separation between adjacent codes measured at each vertical step in percent of LSBs. It can be written as

$$DNL = (D_{cx} - 1)LSBs \quad (2.2)$$

where, D_{cx} is the size of actual vertical step in LSBs.

It is simply the variation of the measured quantization step from the ideal quantization step. If the DNL absolute value is less than 1 LSB, then the ADC has no missing codes.

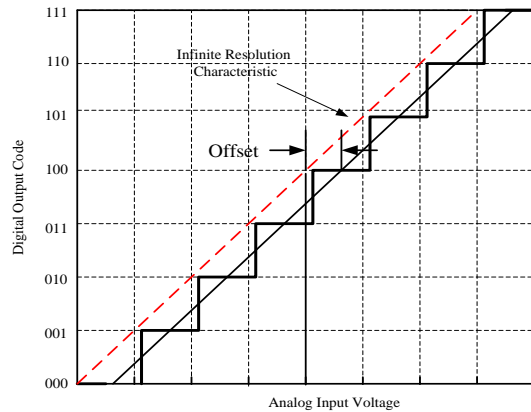


Figure 2-3 Offset errors for a 3-bit ADC

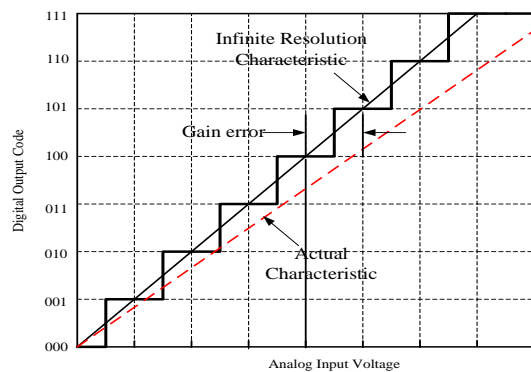


Figure 2-4 gain error for a 3-bit ADC

2.2.3 INTEGRAL NON-LINEARITY ERROR

INL of ADC is the maximum difference between the actual finite resolution characteristic and the ideal finite resolution characteristic measured vertically in percent of LSBs. It is the deviation of the mid-point codes from the ideal location on the infinite resolution characteristic. It can be obtained by summing the DNL errors.

2.3 DYNAMIC CHARACTERISTICS OF ADC

The frequency domain parameters obtained from the analysis of the digital output using a Fast Fourier Transform (FFT) determine the dynamic characteristics of ADC. These parameters are Signal-to-Noise (SNR) ratio, Total Harmonic Distortion (THD), Dynamic Range.etc.

2.3.1 SIGNAL-TO-NOISE RATIO

The Signal-to-Noise ratio is given by the ratio between the signal power and the power of the noise. Noise here represents quantization noise and noise in the circuit. For an ideal ADC, noise is only due to quantization noise. SNR is given by,

$$SNR_{max} = \frac{2^N \sqrt{6}}{2} \quad (2.3)$$

In terms of decibels, the maximum achievable SNR is,

$$SNR = (6.02N + 1.76) \text{ dB} \quad (2.4)$$

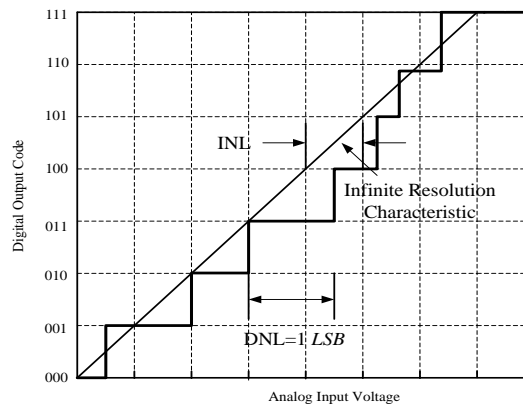


Figure 2-5 INL and DNL errors for a 3-bit ADC

2.3.2 SIGNAL-TO-NOISE AND DISTORTION RATIO

The Signal-to-Noise and Distortion ratio is given by the ratio of signal power and the power of the noise and harmonic distortion. In a non-ideal ADC all the functional parameters contribute to the noise.

2.3.3 TOTAL HARMONIC DISTORTION

Harmonic Distortion is present in non-linear systems whose signal power is spread into fundamental frequency tone as well as the harmonics. The power in those harmonics contributes to Total Harmonic Distortion (THD). It represents the ratio between the sum of amplitude H_k of harmonics of order k and the amplitude of the input signal.

$$THD = 20 \log \left(\frac{\sqrt{\sum H_k^2}}{A(f_{in})} \right) \text{ dB} \quad (2.5)$$

2.3.4 EFFECTIVE NUMBER OF BITS

The Effective Number of Bits (ENOB) is represented as

$$ENOB = \frac{SNDR - 1.76}{6.02} \text{ bits} \quad (2.6)$$

2.3.5 DYNAMIC RANGE

Dynamic range is defined as the range of input of a system for which the output is valid. The maximum input level is limited by the distortion whereas the minimum input is limited by noise. It is also defined as the value of input signal at which the SNDR is 0 dB .

2.3.6 SPURIOUS-FREE DYNAMIC RANGE

Spurious-free Dynamic Range is the ratio between the rms value of the amplitude of fundamental frequency tone and the rms value of the amplitude of largest tone with distortion (spurious spectral tone). It is the measurement of fidelity of the circuit.

2.4 SUMMARY

This chapter explained the performance metrics of ADC. The ADC's characteristics were explained in terms of dynamic and static ways. Different parameters that must be verified after the design are showcased. In this way, the designer can be sure of the dynamic and static characteristics of ADC that must be evaluated. All the parameters may or may not be verified for the working ADC but the most important ones to be looked out are SNR, SNDR, THD, ENOB, INL and DNL. Apart from these different papers suggest verification of different parameters.

3 INTRODUCTION TO CYCLIC/ALGORITHMIC ADC

This chapter discusses different types of architectures along with the comparisons and tradeoffs between these architectures. This chapter also focuses on introducing Cyclic ADCs along with the primary non-idealities involved in the design.

3.1 VARIOUS ADC ARCHITECTURES

There are many ADC architectures defined but they distinctly fall under 2 categories, Nyquist Rate Converters and Oversampled Converters.

Nyquist Rate Converters operate at sample frequency that is twice the bandwidth of the signal. They derive the name from the Nyquist principle where the sampling frequency must be at-least twice the signal bandwidth to adequately recover the signal.

Oversampled converters operate at frequencies that are much higher than the signal bandwidth. These types of converters are very accurate but are very power hungry at the same time. The advantage of oversampled converters is that the problem of aliasing is very much reduced as the frequency spectrum contains frequencies that are widely spread.

The table (Allen & Holberg, 2002) below shows the various architectures of ADCs

Conversion Rate	Type of ADC	Resolution
Slow	Integrating	Very high resolution > 14 bits
Medium	Successive Approximation 1-bit pipelined Algorithmic/Cyclic	Moderate resolution > 10 bits
Fast	Flash Multiple-bit pipelined Folding and Interpolating	Low resolution > 6 bits

Table 3-1 Various ADC Architectures

ADCs can be designed by using a wide variety of architectures. They have their own advantages and disadvantages. We can assume Conversion Time vs. Resolution and Area vs. Resolution as the two principle trade-offs in ADCs. The conversion time of Flash and Pipelined ADCs remain independent of the resolution. For the other structures the conversion time increases with the increase in resolution. On the other hand, area remains independent of the resolution in Incremental converters whereas it increases with the resolution for the other architectures.

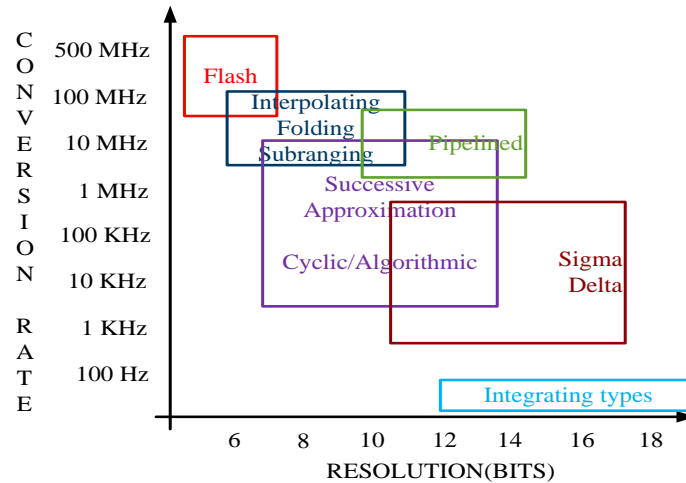


Figure 3-1 Conversion time vs Resolution for different ADC architectures (Sansen, 2006)

Flash ADCs are the fastest converters with speeds greater than 1 GS/s and resolution less than 6 bits. Folding and Interpolating also come under the same category of Flash ADCs. Pipelined ADCs have medium conversion rates and with a resolution around 6-14 bits. Delta-Sigma converters and Incremental structures achieve highest resolution of 15-20 bits at very low sampling speeds due to their high conversion time. Cyclic and SAR ADCs also have a resolution about 6-12 bits and with a lower sampling speeds than Pipelined architectures. But these structures can have low power consumption thus offering great efficiency.

3.2 CYCLIC/ALGORITHMIC ADC

Cyclic (or Algorithmic) ADC is similar to that of a Pipelined ADC with a single stage and the residual output fed back to the input. They are better compared to the Pipelined structures in terms of area but the conversion rates are low.

3.2.1 OPERATION OF CYCLIC ADC

In a Cyclic ADC, the output of one cycle is fed back to the input requiring N cycles for an N bit conversion. On each cycle, one effective digital bit is determined by comparing the input voltage to a reference and the residue is generated by multiplying the difference between the input and analog equivalent of the digital bit with two (M, R., M., & K., 2002).

One digital bit is computed every conversion cycle. That implies one digital word is obtained for every N clock cycles, where N is the resolution of ADC.

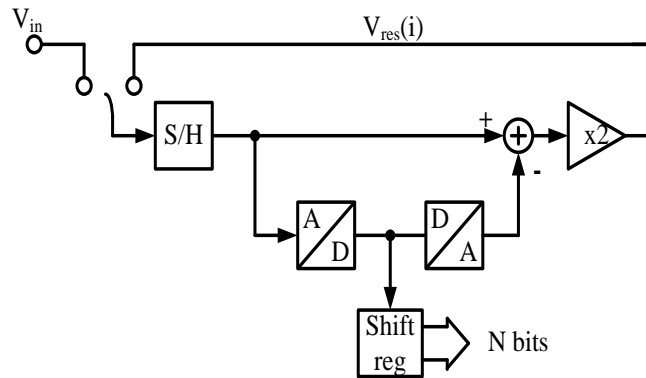


Figure 3-2 Generic Block Diagram of the cyclic ADC

An algorithmic stage, resolving N-bits primarily involves an SHA amplifier, a residue amplifier, a sub-ADC, DAC and a summing block. The block diagram of a cyclic ADC is shown in Figure 3-2.

In the first cycle, the input voltage V_{in} is sampled and at the same time, is compared to the reference voltage to generate bit d : $d = 1$ if $V_{in} > 0$, otherwise $d = 0$. This signal is passed to DAC switch which generates the analog estimate of the comparator result. This estimate is subtracted from the signal that is held on SHA amplifier to produce the analog residue voltage. This residue voltage swing is brought back to the full-scale reference level by a precise gain of 2 and is given by,

$$V_{res}(i+1) = 2 \times V_{res}(i) \pm d \times V_{ref} \quad (3.1)$$

$V_{res}(i)$ is the signal on i^{th} cycle and

$V(1) = V_{in}$ where V_{in} is the input signal.

V_{ref} is the reference signal.

d is the digital output from sub ADC that decides whether the reference signal is added or subtracted in the equation.

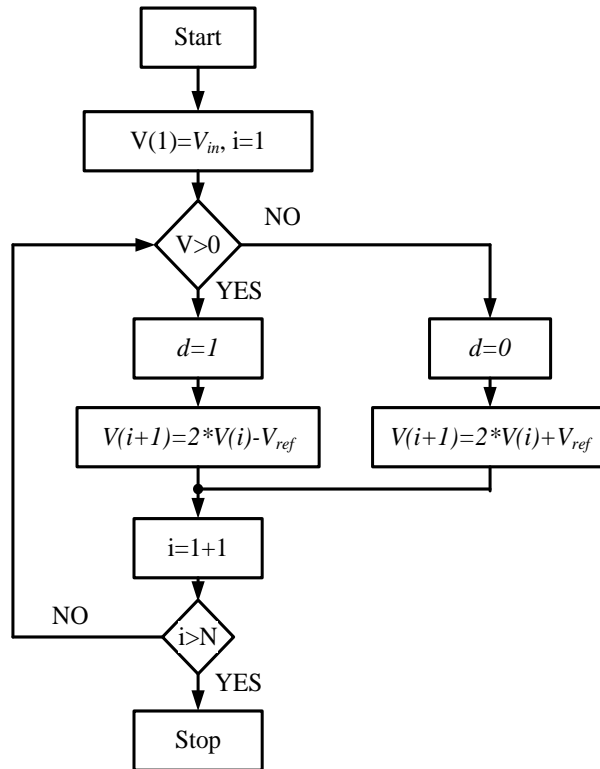


Figure 3-3 Conventional Cyclic Converter flow chart

This voltage is fed back to the input and the process continues until N-bits are evaluated. After the completion of one digital word, the SHA amplifier samples the input signal V_{in} again and the conversion process repeats. The operation of a cyclic converter is given as a flow chart in Figure 3-3.

For a 1-bit/stage architecture, as shown in the above flow chart, the sampled signal which ranges from $-V_{ref}$ to V_{ref} is quantized by sub-ADC. The sub-ADC output is then fed to DAC switch to generate the analog estimate of the input signal. The estimate is then subtracted from the sampled signal to generate the residual voltage. The residue voltage is then amplified by two such that the voltage is centered on zero. Then, this internal residue is sampled by the next cycle (Hai, 2011).

In the transfer function of a 1-bit/stage architecture, the output of the DAC switch can be either $-V_{ref}/2$ or $+V_{ref}/2$, depending on the inputs of 1 or 0, respectively. The output voltage or the residue voltage is given by

$$V_{res} = 2V_{in} \pm V_{ref} \quad (3.1)$$

We can see that the range of the residue voltage is same as that of the input range and so the residue is sampled during the next stage directly.

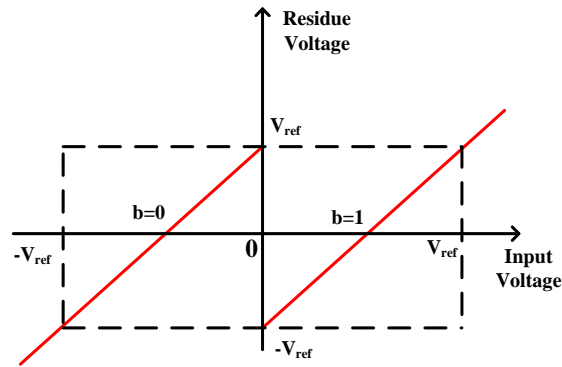


Figure 3-4 Residue Plot of a 1-bit/stage Cyclic ADC

Figure 3-4 Residue Plot of a 1-bit/stage Cyclic ADC shows the transfer characteristic of the 1-bit algorithmic stage. Comparator makes the decision of either $b = 0$ or $b = 1$ respectively, based on the input voltage greater than or less than the reference voltage.

3.2.2 OFFSET EFFECTS ON THE RESIDUE

Conventional Cyclic converters suffer from some non-ideal effects such as comparator inaccuracies and loop offset errors. The voltage residue must be in the range of $-V_{ref}$ to V_{ref} to ensure convergence. Any shift in these values results in comparator offsets. If the comparator offsets are large, it may result in missing codes.

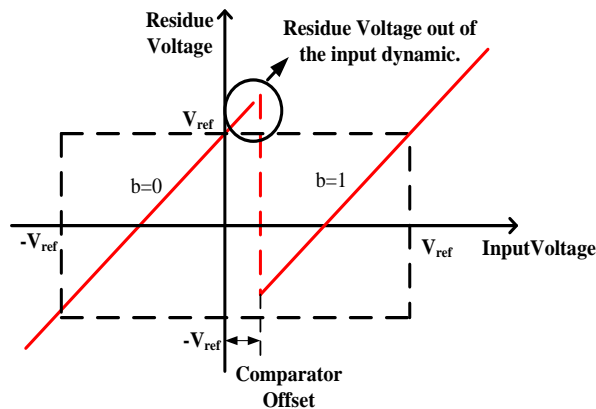


Figure 3-5 Comparator Offset in Conventional Cyclic ADC

Figure 3-5 shows the comparator offset in Cyclic ADCs, where it can be noticed that the shift in the reference voltage leading to residues out of the input dynamic range.

Conventional cyclic converters are sensitive to the loop offset errors that add up as a partial remainder at each conversion cycle. These errors cause integral and differential nonlinearities.

In Figure 3-6 the loop offset error is modeled by means of a vertical shift of the loop transfer characteristic. In the case of a conventional cyclic converter, an input signal value in the neighborhood of half the reference voltage leads to divergent residue voltage (Gennetti, Jespers, & Vandemeulebroecke, 1992).

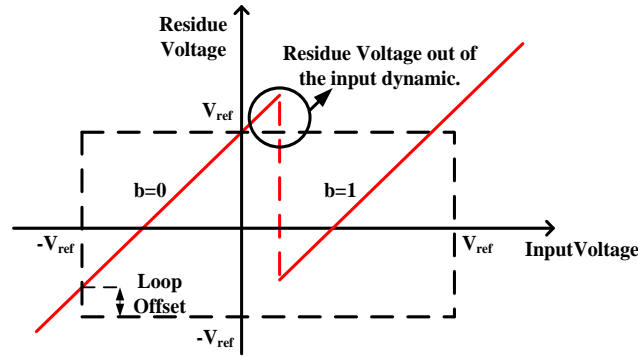


Figure 3-6 Loop Offset Error in Conventional Cyclic ADC

3.3 SUMMARY

This chapter showed the implementation of ADCs using different architectures mainly categorizing them into two types. Also, the architectures are compared based on the speed and resolution showcasing the prominence of Cyclic ADCs at medium speeds and medium resolution when compared with other architectures. The main advantages being low hardware complexity and die area cost. There may be different architectures suitable for the specifications given in chapter 1. But, the Cyclic ADC have been selected to be the best choice with respect to many trade-offs.

Also, the basic of Cyclic ADC was explained along with depicting its functioning in a flowchart. The functioning of Cyclic ADC was seen introducing the most prominent parts of the design. The flow chart tried to explain the operation of the Cyclic Algorithm. The whole architecture we discussed in this chapter is 1-bit/stage architecture which means the ADC can resolve only a single bit every clock cycle.

Also, the non-idealities that can limit the 1-bit/stage cyclic ADC were discussed, the main errors being the comparator offsets and loop offsets. It is also shown how these offsets can seriously limit the performance of the ADC. Apart from these errors the conventional cyclic converters suffer from many drawbacks but the main drawbacks being the offsets. So, it is enough to know the problems caused by the offsets and methods to suppress them. As the 1-bit/stage architecture cannot solve the effect of the offsets, it is not so useful to know about the other non-ideal effects. It is important to switch to some new architecture instead.

4 RSD CYCLIC A/D CONVERTER

This chapter presents the traditional aspects of RSD Cyclic converter. It also discusses the characteristics of these converters in combating the various non-idealities. Also comparisons between the features of conventional RSD Cyclic converters and RSD Cyclic converters employing CLS technique are shown.

4.1 RSD ALGORITHM

To overcome the offset errors in the conventional Cyclic ADC, a new architecture was proposed in (Gennetti, Vandemeulebroecke, & Jespers, 1988). The Redundant Signed Digit Algorithm facilitates high resolution conversion without having to use accurate voltage comparators. The architecture employing RSD algorithm is often referred to as 1.5-bit /stage architecture and is one of the most popular digital error correction techniques to overcome the effects of comparator and loop offsets.

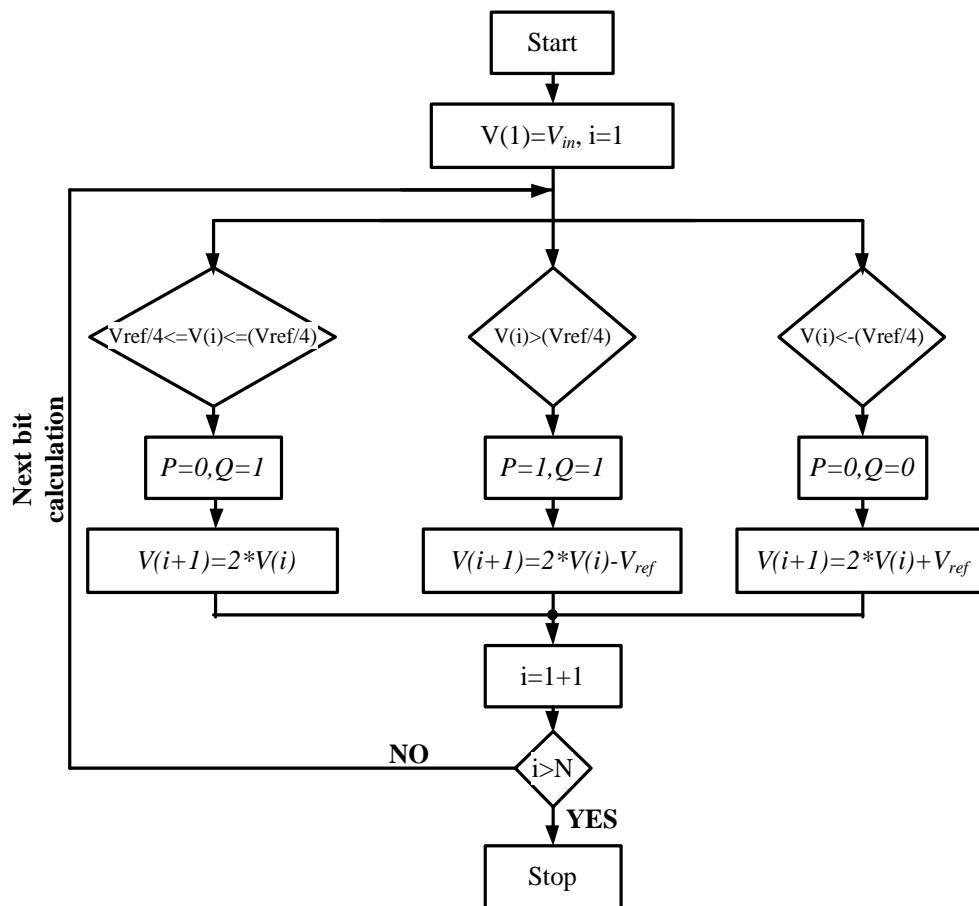


Figure 4-1 RSD Cyclic Converter Flow Chart

The flow chart in Figure 4-1 shows the typical implementation of the RSD Cyclic algorithm.

The conversion of an analog value into a binary value through RSD Cyclic algorithm is well defined in the paper (Gennetti, Jespers, & Vandemeulebroecke, 1992). For an

analog input voltage V_{in} , input voltage range of $[-V_{ref}, +V_{ref}]$ and to obtain a resolution of n-bits the following steps can be used. Let us define the threshold range V_{th} to be in between '0' and $V_{ref}/2$. If $V_{in} \geq V_{th}$, the residue voltage is given by $V_{res} = 2V_{in} - V_{ref}$ and the comparison result is '1'. If $V_{in} \leq V_{th}$, the residue voltage is given by $V_{res} = 2V_{in} + V_{ref}$ and the comparison result is '-1'. Otherwise the residue is given by $V_{res} = 2V_{in}$ and the comparison result is '0'. This procedure is repeated for n cycles until the digital word is obtained and for each stage the input will be the residue voltage from the previous cycle.

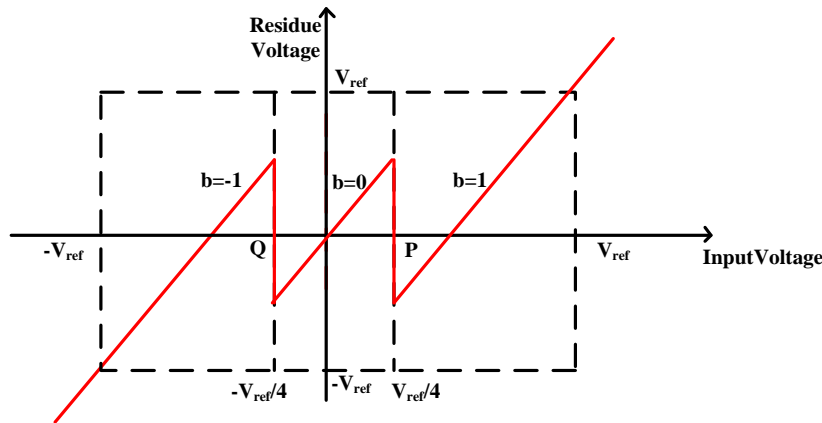


Figure 4-2 Residue Plot of a 1.5-bit/stage Architecture

The digital word obtained contains the combination of values '1', '0' or '-1'. This digital word is to be translated to binary code. Based on our RSD Cyclic algorithm a '1' means a multiply by two and add one which is just a shift to the left and adding a one to the code, a '-1' means multiply by two and subtract a one which means shift to the left and add two's complement of 1 and a '0' means multiply by two which means a shift to the left and adding 0 to the code. This procedure delivers the unsigned binary code. In a signed binary code a binary '1' for the most significant bit means the number is negative and a binary '0' means the number is positive (Atris, 2007).

The residual plot of an ideal 1.5-bit/stage architecture is shown in Figure 4-2. The input dynamic range can be divided into 3 zones, as there are two transition points at $+V_{ref}/4$ and $-V_{ref}/4$. The outputs can be -1, 0 or 1 depending on the set of digital codes obtained from P and Q (00, 01 and 10) respectively.

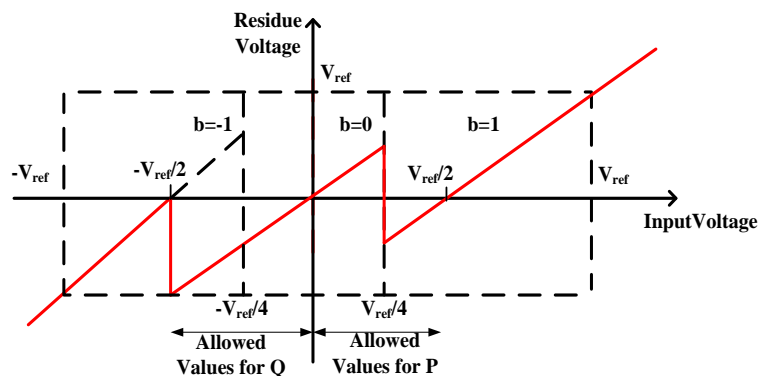


Figure 4-3 Residue Plot with Comparator Offset at $-V_{ref}/2$

One important characteristic of the RSD Cyclic algorithm is that the comparator offsets of $\pm V_{ref}/4$ can be tolerated allowing high levels of noise, offset and even hysteresis. Therefore these offset errors can be corrected by digital correction. This eliminates the use of accurate comparators in the design. The transfer characteristics of 1.5-bit/stage architecture with comparator and loop offset errors are shown in Figure 4-3 and Figure 4-4. In both the cases, the residue voltage is inside the convergence domain and in the range of input dynamic $\pm V_{ref}$. Now, this residue voltage can be successfully resolved by the next cycles to follow, provided the residue still remains in the input dynamic of the following stages.

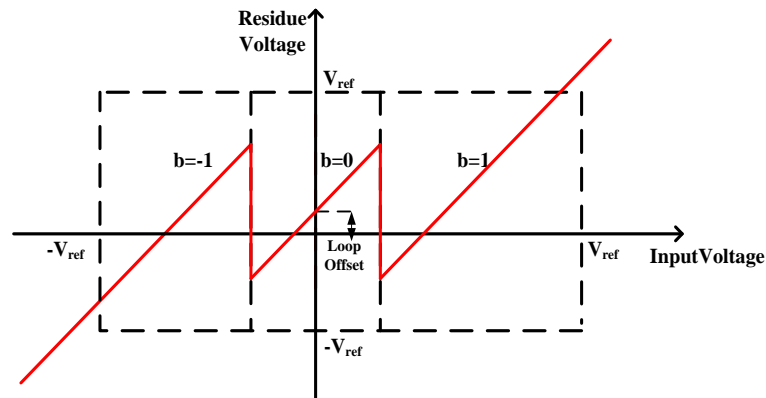


Figure 4-40 Residue Plot of a 1.5-bit/stage Architecture with Loop Offset Error

4.2 TYPICAL IMPLEMENTATION OF RSD CYCLIC ADC

The most popular approach to implement an RSD Cyclic ADC is the Switched Capacitor (SC) implementation. This implementation is suitable to be integrated in a chip and is not dependent on the absolute values of the capacitors but the ratio of the values of the capacitors.

Figure 4-5 shows the implementation of the Cyclic ADC (Single-ended implementation). This ADC has a sample-and-hold (SHA) stage and a second stage called Gain stage. SHA consists of capacitors C_{s_SHA} , C_{f_SHA} and an operational amplifier A1. Gain stage consists of capacitors C_{s_RA} , C_{f_RA} and an operational amplifier A2. The whole ADC operates in two non-overlapping clock phases $\Phi 1$ and $\Phi 2$. During the first sampling phase, Φ_{in} is active and V_{in} is sampled onto C_{s_SHA} . In this design SHA stage has two important tasks to perform. One task is to sample the analog input onto the sampling capacitor and the other task is to sample the residue generated by the gain stage, before sending the sample back to the gain stage. During the first cycle, the input is sampled across C_{s_SHA} . In the next phase $\Phi 2$, the sample is transferred on to the feedback capacitor C_{f_SHA} , where the sample is held. This sample is compared by the comparators to generate the bits P and Q. During the same time, this sample is transferred on to the sampling capacitor C_{s_RA} . At this point, by making use of charge conservation law, we can write,

$$Q = -C_{s_RA} - C_{f_RA} = -V_{out}C_{f_RA} - V_{dac}C_{s_RA} \quad (4.1)$$

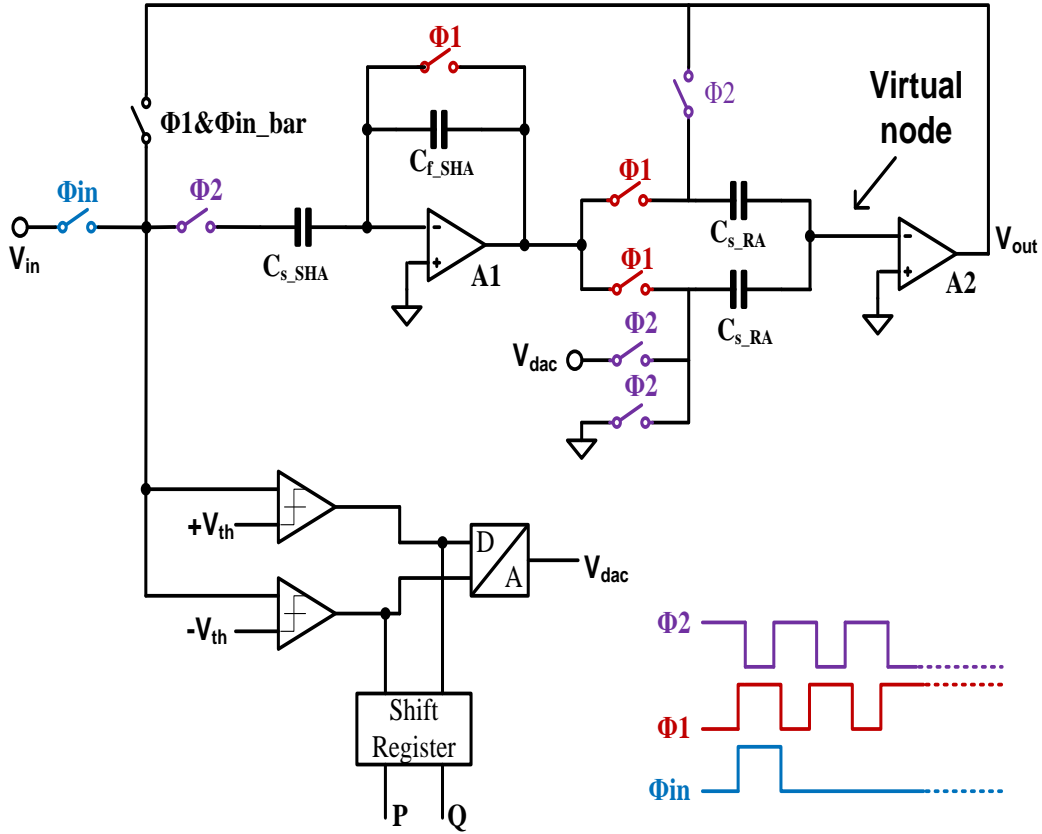


Figure 4-5 Single Ended Implementation of RSD Cyclic ADC

The above charge is at the virtual ground node indicated in Figure 4-5 as 'virtual node'. The charge at the end of phase $\Phi 1$ is $-C_{s_RA} - C_{f_RA}$ and at the end of phase $\Phi 2$ is $-V_{out} C_{f_RA} - V_{dac} C_{s_RA}$.

$$V_{dac} = \begin{cases} V_{refp}; & \text{if } V_{in} > +V_{ref}/4 \\ V_{refm}; & \text{if } V_{in} < -V_{ref}/4 \\ 0; & \text{if } +V_{ref}/4 \leq V_{in} \leq -V_{ref}/4 \end{cases}$$

Solving for V_{out} ,

$$V_{out} = V_{in} \left(1 + \frac{C_{s_RA}}{C_{f_RA}} \right) - V_{dac} \frac{C_{s_RA}}{C_{f_RA}}$$

$$V_{out} = \left(1 + \frac{C_{s_RA}}{C_{f_RA}} \right) \left(V_{in} - \frac{V_{dac} \frac{C_{s_RA}}{C_{f_RA}}}{1 + \frac{C_{s_RA}}{C_{f_RA}}} \right) \quad (4.2)$$

Since, $C_{s_RA} = C_{f_RA}$ we obtain

$$V_{out} = (1 + 1) \left(V_{in} - \frac{V_{dac} \times 1}{1 + 1} \right) = 2 \times V_{in} - 2 \times \frac{V_{dac}}{2}$$

$$V_{out} = 2 \times V_{in} - V_{dac} \quad (4.3)$$

Solving for i^{th} evaluation phase,

$$V_{out}(i+1) = \begin{cases} 2V_{out}(i) - V_{refp}; & \text{if } V_{out}(i) > +V_{ref}/4 \\ 2V_{out}(i); & \text{if } +V_{ref}/4 \leq V_{out}(i) \leq -V_{ref}/4 \\ 2V_{out}(i) - V_{refm}; & \text{if } V_{out}(i) < -V_{ref}/4 \end{cases}$$

The SHA now samples the above residue voltage across C_{s_SHA} . This voltage is held across feedback capacitor in the next phase. The next residue is generated by the gain stage using this held signal and the above process continues until all the bits are generated. Now, the input voltage is again sampled and evaluated until the next digital word is obtained. In the above implementation, to generate n-bits, the ADC requires '2n' clock cycles.

So, the combination of SC structure and 1.5-bit/stage architecture gives better resolution as the comparator offsets up to $\pm V_{ref}/4$ can be tolerated. But still, there are many other non-idealities that affect the performance of ADC. Some of the important errors are discussed in the next section.

4.3 DIFFERENT NON-LINEARITIES

Apart from the comparator inaccuracies and the loop offset errors, there are also other non-ideal errors that largely limit the performance of the RSD Cyclic ADC. Some of the prominent errors in the design are

Capacitor Mismatch Errors

Thermal Noise

Finite gain error of op amps

Analog Switch non-idealities

4.3.1 CAPACITOR MISMATCH ERRORS

The component mismatches arise due to the process variations and pose a serious problem by limiting the achievable resolution of the ADC. The most important of all the mismatches is the capacitor mismatch.

The ratio between the sampling capacitor and feedback capacitor must be equal to 1 which is not true in practical cases. Due to this mismatch large errors are possible and this mismatch can be modeled as,

We know the residue voltage provided by the gain stage,

$$V_{out} = \left(1 + \frac{C_s}{C_f}\right) V_{in} \quad (4.4)$$

Let us assume there is a mismatch of ΔC in both the capacitors, and they can be modeled as $C_s = C \pm \Delta C$ and $C_f = C \mp \Delta C$. Now the residue voltage is given by,

$$V_{out} = \left(1 + \frac{C_s}{C_f}\right)V_{in}$$

$$V_{out} \cong 2 \left(1 \mp \frac{\Delta C}{C}\right)V_{in}$$

Due to this error, there can be discontinuities in the residue plot that give rise to missing codes (Hai, 2011).

We would like this error to be much less than 1 LSB. So, we have

$$\frac{\Delta C}{C} \ll \frac{V_{fs}}{2^n} \quad (4.5)$$

where, V_{fs} is the full-scale range of the input.

The percentage error due to the process variations must be less than the above given error. To minimize the error, capacitor size must be large. But, on the other hand, large capacitor sizes are not always good as they can increase the area significantly.

4.3.2 THERMAL NOISE

Thermal noise is the dominant noise in any SC implementations and this sets the minimum sampling capacitor size. The noise voltage on the sampled capacitor is given by,

$$v_n^2 = \sqrt{\frac{kT}{C}}$$

where k is the Boltzmann's constant, T is the absolute temperature in Kelvin and C is size of the sampling capacitor.

From the above equation we can see that the thermal noise is dependent on sampling capacitor size. The thermal noise is inversely proportional to the capacitor size in the above equation. So, if we set the thermal noise to be much less than (say 10 times) 1 LSB, we have

$$v_n \leq 0.1 \times \frac{V_{fs}}{2^n}$$

Solving the above two equations for C_s ,

We get,

$$C_s \geq \frac{2^{2n}kT}{0.01 \times V_{fs}^2} \quad (4.6)$$

4.3.3 FINITE GAIN ERRORS OF OTAS

Finite gain is the most important parameter that affects the ideal characteristics of the RSD cyclic converter. This error comes into play due to the fact that the DC gain of an op amp is finite. Let A_v be the open loop DC gain of the op amp. Then, the closed loop gain G is given by,

$$G_{actual} = \frac{A_v}{1 + \frac{A_v}{\left(1 + \frac{C_s}{C_f}\right)}}$$

where, $\frac{1}{\left(1 + \frac{C_s}{C_f}\right)}$ is the feed-back factor. ' β '

If $C_s = C_f$, the feed-back factor is,

$$\frac{1}{\beta} = G_{ideal} = 2 \quad (4.7)$$

The above equation also gives the ideal closed loop gain, when open loop DC gain is infinite. So the error due to finite gain can be modeled as,

$$\frac{G_{ideal} - G_{actual}}{G_{ideal}} = \frac{\Delta G}{G} = \frac{1}{1 + A_v \beta}$$

For large gains, $A_v \beta \gg 1$, so the gain error is

$$\frac{\Delta G}{G} \cong \frac{1}{A_v \beta}$$

This error must be less than 1 LSB and 1 LSB is given by

$$1 \text{ LSB} = \frac{V_{fs}}{2^{n-1}}$$

This is because, by the time the multiply-by-two operation is performed, already a digital bit is obtained. So we need to take into account only the next bit resolution and is given by the above equation.

Now we need the gain error to be much less than (say half of the) this bit resolution

$$\frac{\Delta G}{G} \leq 0.5 \times \frac{V_{fs}}{2^{n-1}}$$

$$\frac{1}{A_v \beta} \leq 0.5 \times \frac{V_{fs}}{2^{n-1}}$$

We know $\beta = 1/2$, so

$$A_v \geq \frac{2^{n+1}}{V_{fs}} \quad (4.8)$$

Along with the finite gain error, the op amp has the settling time and Gain-bandwidth product (GBW) requirement. These are also the important parameters that have an influence on the performance of op amp and in-turn on the performance of ADC. (Atris, 2007) The time constant ' τ ' of the dominant pole is computed as

$$\tau = \frac{1}{GBW \times \beta} \quad (4.9)$$

So, the closed-loop bandwidth f_{3-dB} which is the inverse of the time constant is given by,

$$f_{3-dB} = GBW \times \beta$$

The settling time constant of the op amp must be 1 LSB as in the previous case and is given by

$$e^{-t/\tau} \ll \frac{V_{fs}}{2^{n-1}}$$

where $t = \frac{1}{2f_s}$ and f_s is the sampling frequency,

Solving for the equations we get the closed-loop bandwidth and GBW requirements (Atris, 2007) and (Hai, 2011),

$$f_{3-dB} = GBW \times \beta \geq 2 \times f_s (-\ln V_{fs} + (n-1) \ln 2) \quad (4.10)$$

The settling time of an n-bit ADC is given by (Hai, 2011),

$$t_s = \frac{1}{N \times f_s} \quad (4.11)$$

4.3.4 ANALOG SWITCH NON-IDEALITIES

MOS transistors that are used as switches in SC implementations can cause clock-feed through, charge injection and can show some non-linear on-resistance.

Clock-feed through is the gate-to-source overlap capacitance of the MOS transistor. This can lead to the error as the capacitance is couple the clock signal to the signal path. This error is signal independent and is totally proportional to the MOS transistor size. This error can be eliminated by the use of a fully differential configuration.

Charge injection is another source of error and is caused by flow of charge into the source and drain terminals when the switch is turned OFF. This charge injection is signal dependent and is non-linear. Use of transmission gates with dummy configuration can eliminate this problem. Also, use of bottom plate sampling technique makes the charge injection signal dependent and this can be removed easily by employing a differential configuration.

As discussed, MOS transistors can exhibit some non-linear ON resistance and this leads to signal dependent errors. This can be suppressed by use of transmission gates again.

For the ADCs with high resolution clock boot-strapping methods can also be used. However, switching errors do not cause some significant errors and many techniques were adopted to avoid these errors.

4.3.5 CORRELATED LEVEL SHIFT TECHNIQUE

This technique is used to reduce the requirement of finite DC gain of the op amp, thus suppressing the gain error (Gregoire & Moon, 2008). This technique allows the gain of the op amp to be low still producing the same results as of an op amp with high DC gain. This technique is compared to the conventional technique in this thesis.

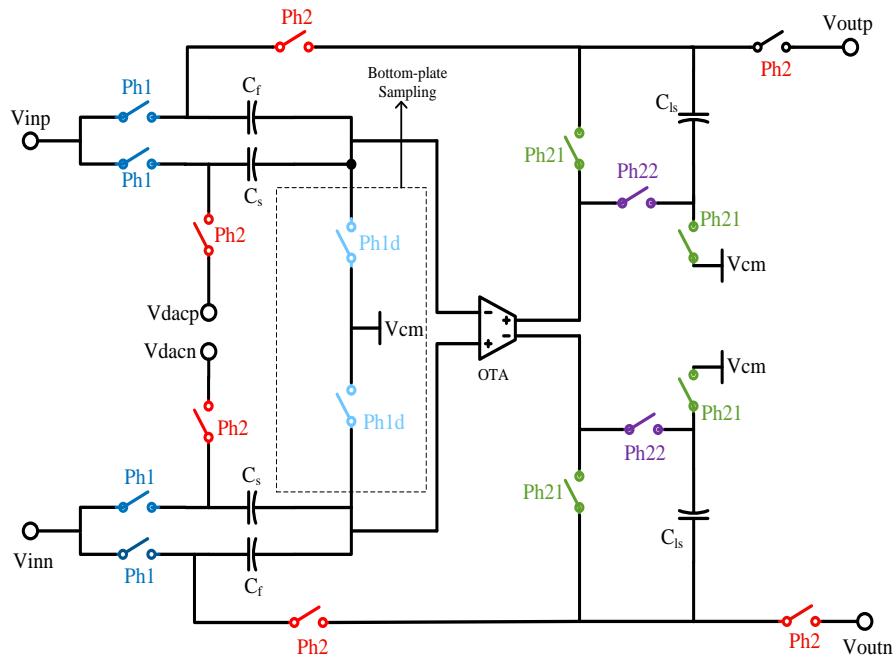


Figure 4-6 Residual Amplifier showing CLS Technique

This technique offers wide swing output by eliminating the gain errors. Figure 4-6 shows the residual Amplifier employing CLS technique. During the sampling phase 'ph1', input is sampled onto the capacitors C_s and C_f . The evaluation/amplification phase is divided into two phases: estimation phase ph21 and level shifting phase ph22. During the estimation phase ph21 the level shifting capacitor C_{Is} samples the estimated output and during the level shifting phase, this capacitor is placed in series with the op amp, bringing back the op amp to common-mode level and thus creating a more accurate virtual ground.

But, during this phase there is also a charge transfer between the level shifting capacitor and load capacitor C_{ld} . The output at the end of ph22 is given by

$$V_o = \left(\frac{C_s + C_f}{C_f} \right) \left(1 - \frac{1 + \delta}{(1 + A_{21}\beta)(1 + A_{22}\beta + \delta)} \right) V_i \quad (4.12)$$

where

$$\beta = \left(\frac{C_s + C_f}{C_f} \right), \delta = \frac{C_{ld}}{C_{ls}}$$

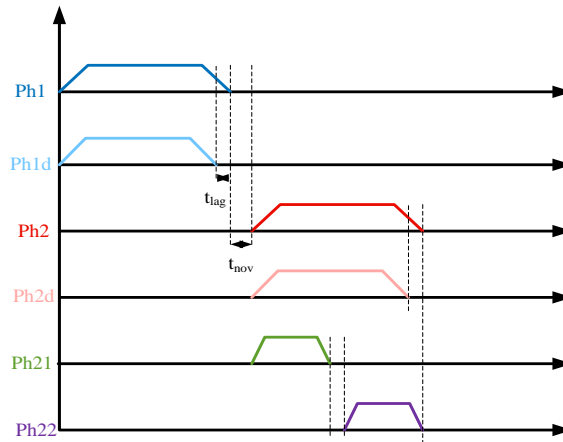


Figure 4-7 Clock Phases Required to Employ CLS Technique

The charge transfer between the level shifting capacitor and the load capacitor degrades the loop gain. This degradation in the loop gain can be avoided by using a two stage op amp. This is due to the fact that the compensation capacitor can provide the charge that is lost by the level shift capacitor during the charge transfer.

There is also a technique proposed in (T & Moon, 2009) to avoid the loop degradation. This technique can be useful in designs employing single stage op amps.

The clock phases used for the CLS technique are shown in Figure 4-7.

4.4 SUMMARY

This chapter summarized the functioning of RSD algorithm and its implementation in Cyclic ADC. The technique's tolerance towards comparator's offsets along with showcasing different non-idealities associated with the design of RSD Cyclic ADC was shown. This chapter primarily concentrated on the mitigation of the offset errors that are caused in the 1-bit/stage architecture. So the technique of RSD algorithm is shown along with the basic operation. The flow chart explains the function of each block and also tells how the ADC resolves the bits in each cycle.

In turn the single ended implementation of the Cyclic ADC was shown and the mathematical functioning is well explained. This implementation is just the basic understanding of the underlying concepts in the ADC. The actual design may differ from this version. This is due the fact that various non-idealities creep up again. So there are some methods discussed to avoid them.

Also, this chapter discussed the requirements on different sizes and parameters of the blocks that must be viewed carefully while designing. These requirements primarily include capacitor sizes so as to lessen the mismatch errors and also to avoid the errors caused due to thermal noise. The gain and GBW required by the op amp is also discussed to avoid the gain errors and other possible non-idealities in the op amp. Apart

from these, there are analog switch non-idealities that can be of a serious problem. There are also methods suggested to mitigate these non-idealities such as use of transmission gates, clock bootstrapping.etc.,

Lastly, the CLS method of implementation that is used to compare with RSD technique is discussed. This method increases hardware and complexity but helps lessen the gain errors and also mitigates the requirements on the op amp. The op amp with a lesser dc gain can be used even while achieving a higher bit resolution.

5 CIRCUIT LEVEL IMPLEMENTATION

This chapter presents the transistor level implementation of the prototype cyclic converter. Design along with the simulation results of different blocks of cyclic converter is discussed. Also, some comparisons were drawn between some new blocks and previously used blocks.

5.1 TWO-PHASE NON-OVERLAPPING CLOCK GENERATOR

The design of non-overlapping clock phase generator is partly influenced by (Delic-Ibukic, 2004). The non-overlapping clock phase generator is shown in Figure 5-1. This design generates a total of six clock phases. The two non overlapping clock phases are generated as ph1 and ph2 with a 180° phase shift from the main clock. All the components in the design must settle within half of the clock period. This is because alternate clock phases are being used for alternate stages.

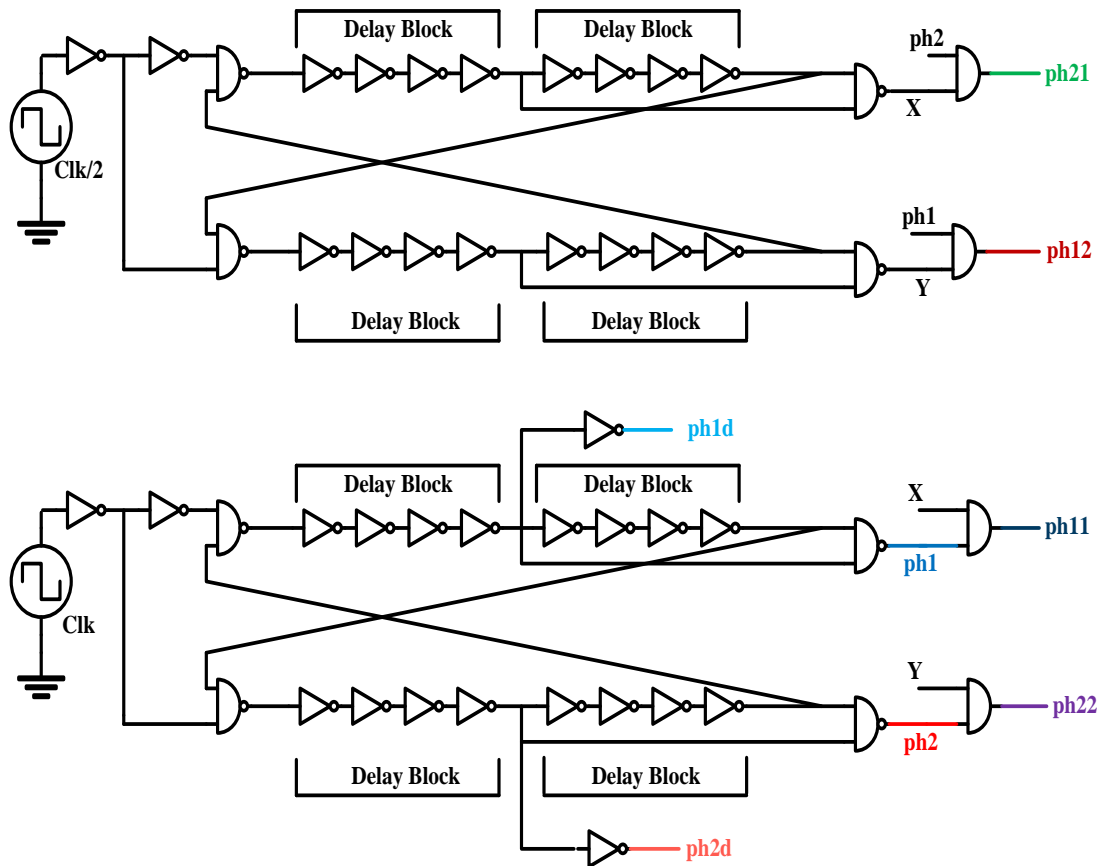


Figure 5-1 Non-Overlapping Clock Phase Generator Design Block

To enable the bottom-plate sampling technique, two more clock phases are required. The delay clock signals ph1d and ph2d are generated also from the main clock. Clock signal ph1d closes before ph1 and in a similar way ph2d closes before ph2.

To enable CLS technique 4 more clock phases are needed to be generated. This is done by making use of a similar clock generator with an input of half the main clock. Using some digital logic phase's ph11, ph12, ph21 and ph22 are generated.

5.1.1 CLOCK GENERATOR DESIGN

The clock generator block is shown in Figure 5-1 and was designed to run at 12 MHz It consists of inverters, 2-input NAND gates, AND gates and delay blocks. The delay block consists of four medium sized inverters. It can be used to adjust the 'on' time of all the clock phases. One additional circuit similar to the main clock generator circuit is made. This is used to generate the clock phases required by the CLS technique. This additional clock generator takes half the time period of main clock as input. So the main clock is at 12MHz and the clock of the additional circuit is at 6 MHz

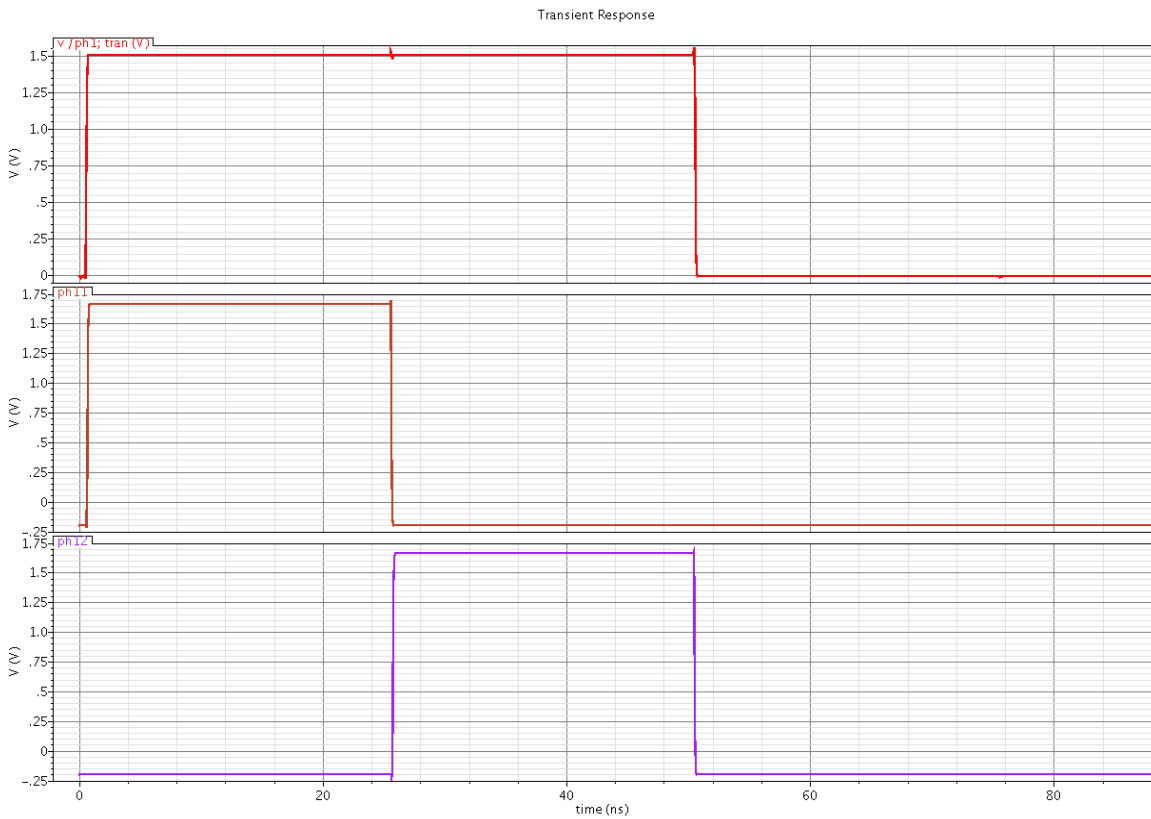


Figure 5-2 Clock phases showing phases used to implement CLS Technique

5.1.2 CLOCK GENERATOR SIMULATION RESULTS

The clock generator is run at 12 MHz in the RSD cyclic ADC. Below figures show the simulation results. Figure 5-2 show the clock phases used for the CLS technique. Ph1 is divided into two phases: estimation phase ph11 and level-shifting phase ph12.

Figure 5-3 shows the delayed phase ph2d along with clock phase ph2. As needed for the bottom-plate sampling technique, ph2d is OFF before ph2.

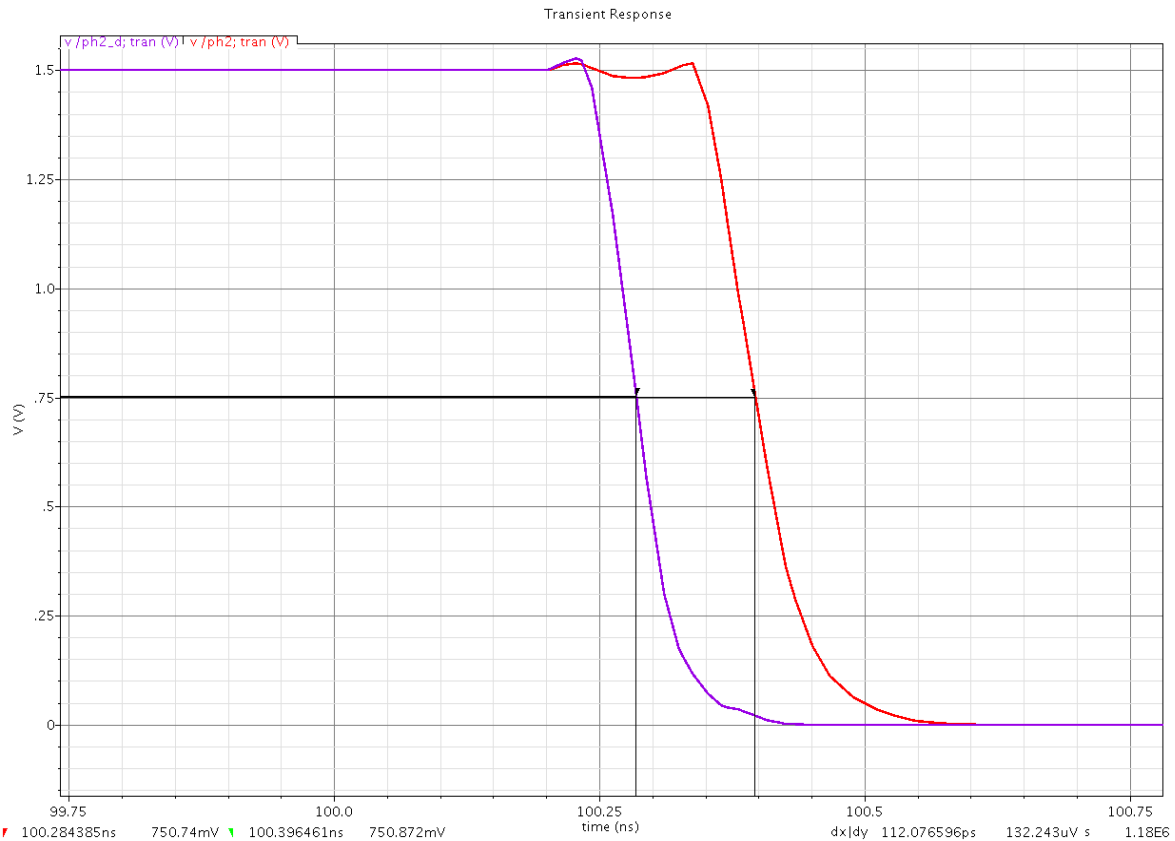


Figure 5-3 Clock Phases showing phase required to implement Bottom-plate Sampling

5.2 SUB-ADC DESIGN

The sub-ADC provides the digital output bits by quantizing the input signal in the first stage and the residual signal in the next stages. The sub-ADC in this design has two differential comparators which provide the threshold voltages $+V_{ref}/4$ and $-V_{ref}/4$. This is because the 1.5-bit/stage architecture requires two threshold voltages and has three possible output states 00, 01 and 11. These output states are converted to output digital bits by a simple combinational logic in the DAC switch. Also these outputs are given to DAC switch in order to calculate the analog outputs. Table 5-1 shows the possible outputs of the sub-ADC based on the differential input given. Next section provides the design of differential comparator.

5.2.1 DIFFERENTIAL COMPARATOR

The differential comparator consists of four capacitors, switches and a voltage comparator. It makes use of the bottom plate sampling technique. The switching circuitry and the capacitors are designed to have the threshold voltages $+V_{ref}/4$ and $-V_{ref}/4$ at each of the inputs. The capacitors at each input side are sized to the ratio of 1:3 to divide the reference voltage by 4. Figure 5-4 shows the possible implementation of the differential comparator.

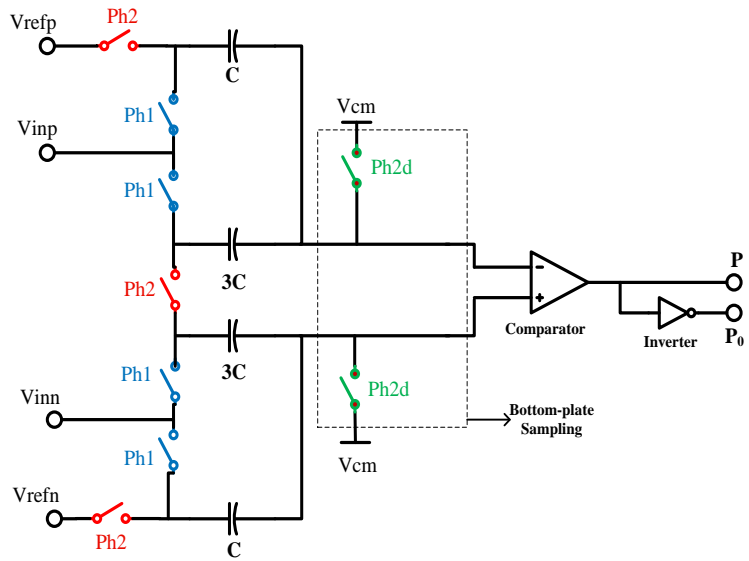


Figure 5-4 Differential Comparator to generate the threshold levels $+V_{ref}/4$ and $-V_{ref}/4$

Table 5-1 shows the possible outcomes when the differential voltages are compared against the threshold voltages. P and Q represent the possible output states for the comparisons. These are sent to DAC switches to calculate the analog voltages. Output state $P=1, Q=1$ is not possible and if it occurs the differential comparator is at error. Apart from this state all the other three states are possible. Next section shows the design of clocked voltage comparator. The inputs of the comparator see the voltages of

Positive side:

$$V_{inp} - \frac{V_{refp} - V_{cm}}{4} \tag{5.1}$$

Negative side:

$$V_{inn} + \frac{V_{refn} - V_{cm}}{4} \tag{5.2}$$

This is accomplished by the switching network and the capacitors.

	$+V_{ref}/4$	$-V_{ref}/4$	P	Q
V_{id}	$>$	$>$	1	1
V_{id}	\leq	\geq	0	1
V_{id}	$<$	$<$	0	0

Table 5-1 Output Calculation in Differential Comparator

5.2.2 VOLTAGE COMPARATOR

The voltage comparator consists of 2 important stages: the pre-amplification stage and the decision-making stage. The bias current is set to 10 μA and the pre-amplifier tail transistor is has 20 μA flowing through it.

Transistors M1 and M2 represents the sensing transistors and they sense the difference between the input voltages. M5, M6, M7 and M8 are simple current mirrors that are activated based on the output from sensing amplifiers. M9 and M10 are diode connected and are used to set the gate voltages for the decision making amplifiers M13 and M14. Based on the output from pre-amplification stage, the decision is made by M13 and M14. M15, M16, M17 and M18 represent the inverter pairs that pull the output high when Latch_Bar is high. They allow M13 and M14 to make the decision by releasing the output when Latch_Bar is low. Transistors M11 and M12 are used to turn the comparator decision making stage OFF during the idle state of comparator. There are other transistors (not shown in the schematic) that pre-charge the output high during comparator's OFF time. The compliment output is obtained by placing an inverter after the comparator's output.

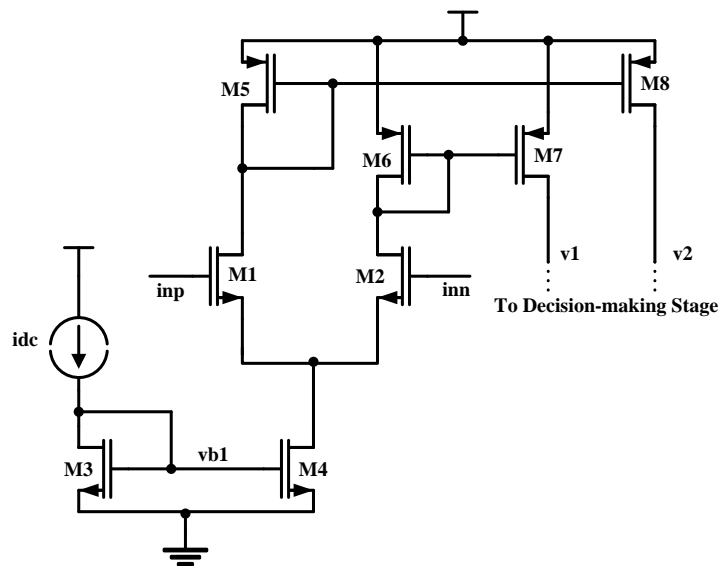


Figure 5-5 Pre-amplification stage of the Voltage Comparator

5.2.3 COMPARATOR SIMULATION RESULTS

Below are the simulation results of the voltage comparator used in the design. Figure 5-7 shows the output of the clocked comparator at a speed of 12 MHz (as the main clock is running at the same speed) and for a swept input of 40 mV at the positive terminal. The input voltage ranges from 725 mV to 765 mV and a reference of 750 mV is applied at the negative terminal. The output is high once the comparator detects the voltage greater than the reference voltage. Latch_Bar decides the output and it is set to ph1. So the output is valid at the end of ph2 while the input is latched on the falling edge of ph1. After the output is obtained, it is pre charged again to erase any previous comparison results.

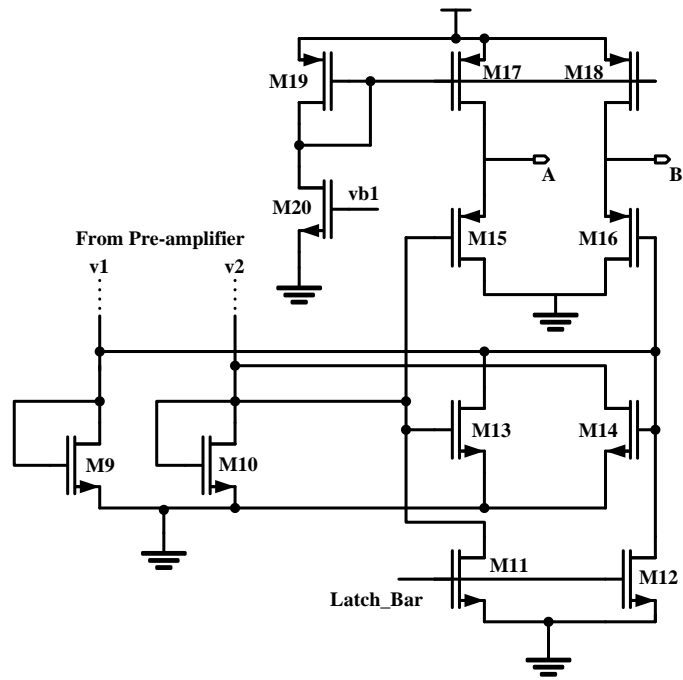


Figure 5-6 Decision-making Stage of the Voltage Comparator

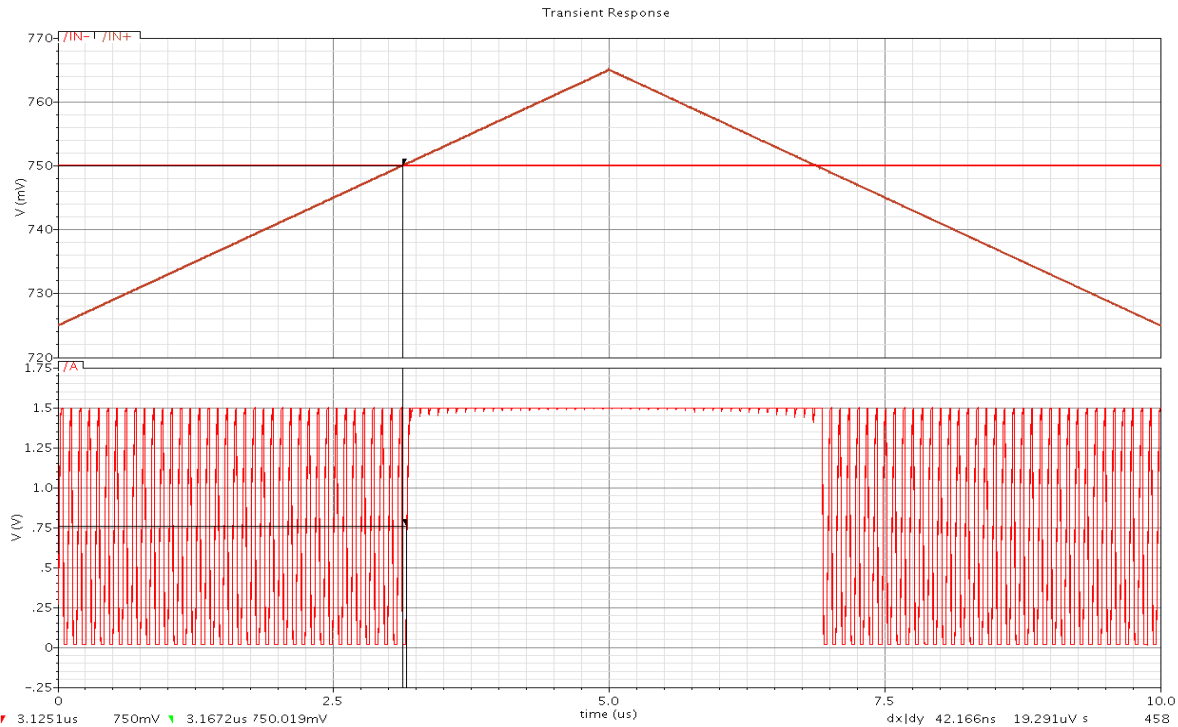


Figure 5-7 Voltage Comparator Simulation Results

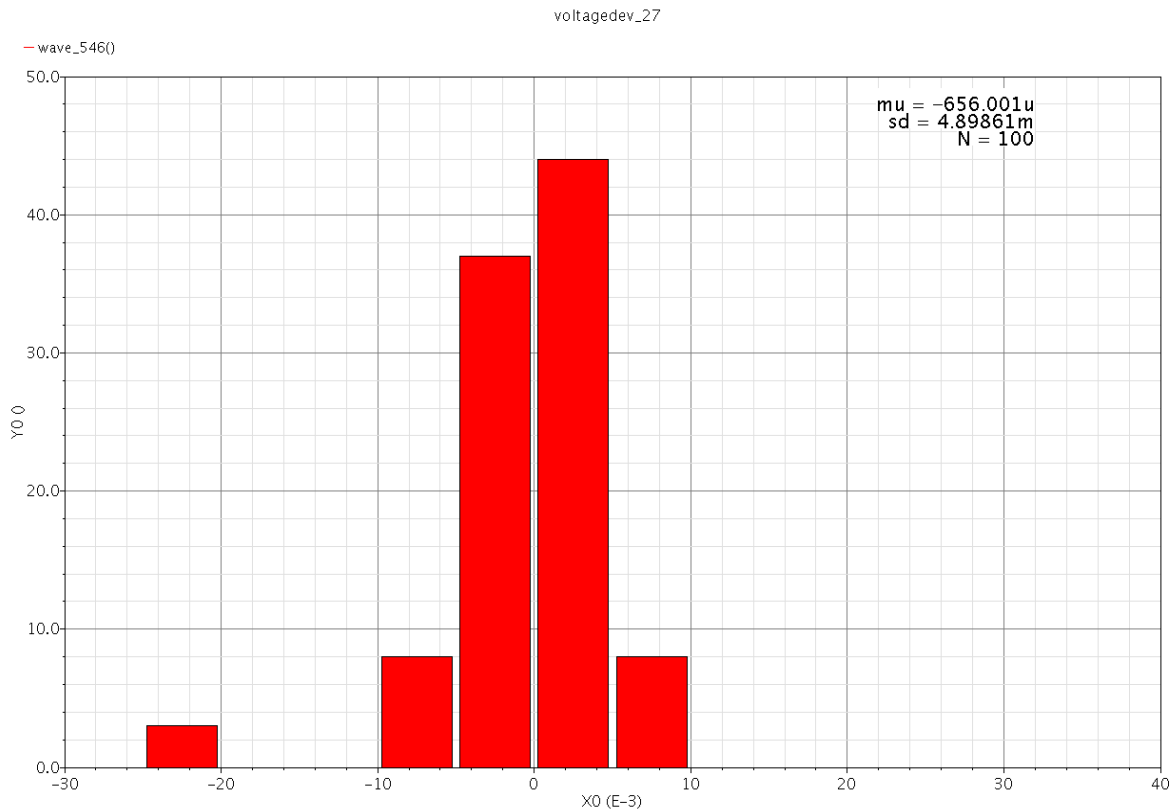


Figure 5-8 Offset Voltage Simulation to find Standard Deviation of the voltage comparator

Figure 5-8 shows the Monte Carlo analysis of the clocked comparator to calculate the input offset voltage. From the histogram it is evident that the standard deviation of the input voltage is around 4.89 mV. This compared with the comparator from the earlier project and proved to be better. The other comparator had an offset of approximately 10 mV. Even the 3σ of the clocked voltage comparator is 14.67 mV which is more than required.

5.3 DAC SWITCH

The design of DAC switch was partly influenced by (Delic-Ibukic, 2004). Some modifications were made to original circuit to meet the needs of ADC. Figure 5-9 shows the NMOS switches and combinational logic that is implemented. The inputs to the DAC switch are the outputs (P and Q) from differential comparators. The compliments of the comparator outputs (P_0 and Q_0) are obtained by the inverters. MSB (d1) and LSB (d0) are the intermediate signals generated from the combinational logic and are sent to shift registers to form the digital word after N cycles. The outputs of the DAC switch are the analog voltages V_{dacp} and V_{dacn} that are the inputs to Residual amplifier. These analog outputs are subtracted from the signal multiplied by a gain of two to generate the residue.

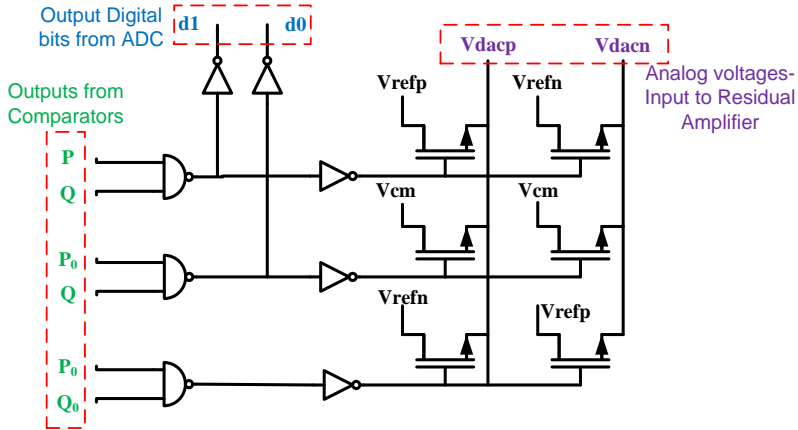


Figure 5-9 DAC switch to Calculate the Analog Voltages for the Residual Amplifier

Table 5-2 shows the possible outcomes of the analog voltages and the digital bits from the DAC switch

P	P ₀	Q	Q ₀	d ₁	d ₀	V _{dacp}	V _{dacn}
0	1	0	1	0	0	V _{refn}	V _{refp}
0	1	1	0	0	1	V _{cm}	V _{cm}
1	0	0	1	x	x	x	x
1	0	1	0	1	0	V _{refp}	V _{refn}

Table 5-2 Operation of DAC Switch

5.4 SAMPLE-AND-HOLD STAGE

SHA stage is inevitable in RSD cyclic ADC design. The design of SHA is taken from (R, M, & O, 2003). The SHA stage employs charge redistribution architecture to perform the sample-and-hold operation. This is done in two clock phases: sampling phase and evaluation phase. During the sampling phase the input is sample onto the sampling capacitor and during the evaluation phase this charge is transferred onto the feed-back capacitor where it is held for that clock period. Thus, the voltage gain is determined by the ratio of C_s and C_f and is usually unity for ADCs.

In this design bottom-plate sampling is used to combat errors like charge injection due to sampling switches. Bottom-plate sampling is carried out by switches with the new clock phases ph1d and ph2d. In Figure 5-10 ph2d clock phase is used for bottom-plate sampling. It is ensured that ph2d closes before ph2, so as to see that a floating node is created at the bottom plate of C_s. In this way the charge injection from sampling switch onto C_s is avoided.

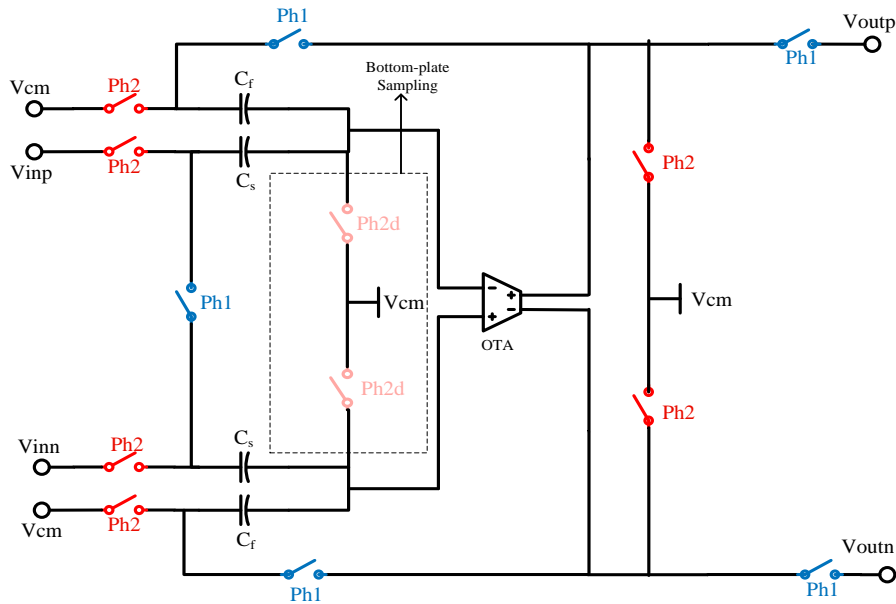


Figure 5-10 Schematic of SHA without using CLS Technique

During sampling phase the output of the op amp is tied to common mode. This is due to the fact that op amp under open loop can stack the output voltages near the positive or negative supply rails. If this happens the op amp takes longer time than normal to recover and come back to the normal operation. To avoid this phenomenon, the output of op amp is connected to common mode voltage during the sampling phase.

SHA stage is also designed with CLS technique shown in Figure 5-11 and the operation is similar to the charge redistribution scheme. But, the stage has the level shifting capacitors and some additional switches that implement CLS technique. This allows having low gain op amp and thus reduces the finite gain error. This technique, may again suffer from the charge transfer drawback and there is a need to employ a two stage op amp to combat the drawback. The capacitance C_{IS} at the output adds up as the load capacitance and proper care must be taken while designing the op amp.

5.4.1 OPERATIONAL AMPLIFIER

The design of a folded-cascode op amp with class A and class AB output stage is discussed. The folded cascode with class A stage is adapted with some modifications from (Allen & Holberg, 2002).

Figure 5-13 shows the two-stage folded-cascode op amp where the second stage is class A with Miller compensation. Use of folded-cascode architecture enables us to have a wide output swing. Class A stage is used as the gain boosting stage of the op amp.

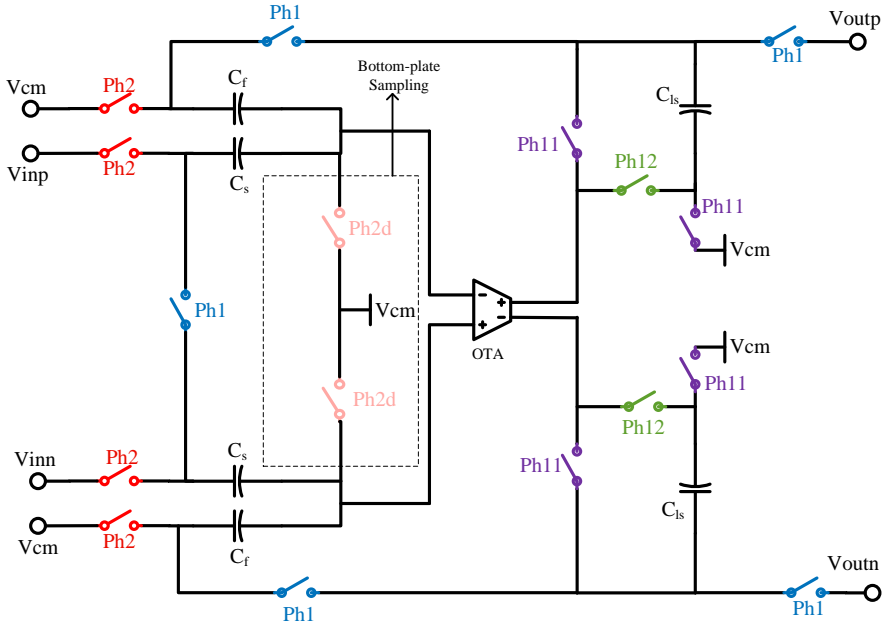


Figure 5-11 Schematic of SHA using CLS technique

The bias circuit shown in Figure 5-12 is different from the original one described in the book. It is a high-swing cascade current source and uses resistor dividers. The bias current is set as 10 μA . The widths and lengths of all the transistors in the bias circuit are adjusted to have different biasing voltages at their gates. The lengths of the PMOS transistor near to positive rail must be high. The resistors ensure the same current of 10 μA flows through the other branch.

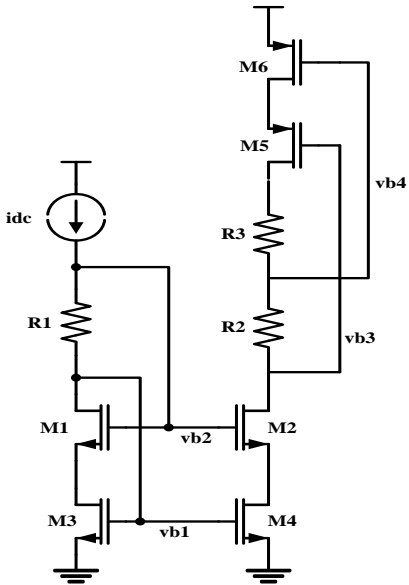


Figure 5-12 Biasing circuit of the Folded-cascode op-amp with class A output stage

The tail transistor in the folded-cascode has a width 3 times that of the NMOS bias transistor M3, to make sure that 30 μA current flow through it. But the length of the tail

transistor is increased to make more current flow for better gain and GBW. The current in the differential pair (M7 and M8) is kept equal to the current flowing in the folded-cascode branch transistors (M12, M13, M14 and M15). But as the current in the tail transistor is increased there is approximately $20\mu\text{A}$ current flowing in the differential pair. The transistors in folded-branch have approximately $15\mu\text{A}$ current flowing through them. The folded-cascode stage provides a gain of 49 dB without the output stage. To increase the gain suitable for the operation of the ADC, class A stage is added as the output stage. A current of $100\mu\text{A}$ is given to the output stage to ensure high gain and bandwidth. Miller compensation is added to the output stage to make the op amp stable. All the transistors in the op-amp operate in medium inversion region.

To ensure stable common-mode voltages during the operation, a common-mode feedback circuit is employed. The CMFB circuit adjusts the common mode output current to stabilize common-mode voltages. There are different architectures that can be used as CMFB circuits like:

Switched-capacitor realization,

Differential difference amplifier realization and

Resistor averaged CMFB circuits.

The function of any CMFB circuit is the same. The two differential output voltages are averaged and compared to the common-mode reference voltage. Now, the differential voltage is converted to the common-mode output current to adjust the common-mode differential output voltage (Luh, Choma, & Draper, 1998).

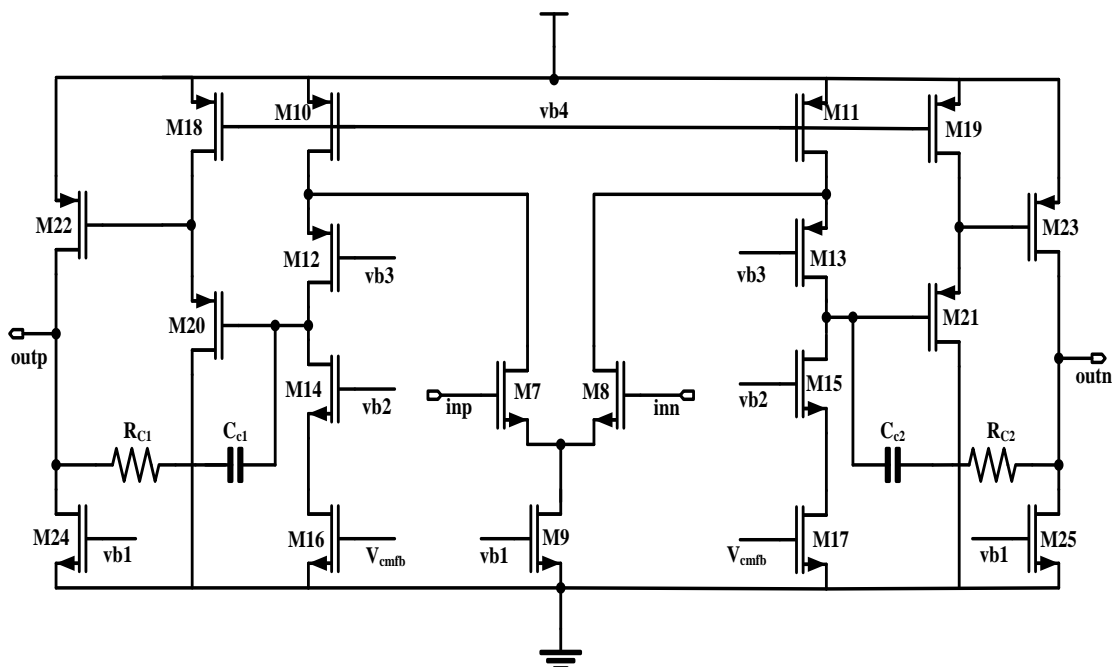


Figure 5-13 Folded-Cascode op amp with Class A Output Stage

The design is adapted from (Johns & Martin, 1997) Figure 5-16 shows the resistor averaged continuous time common-mode feedback circuit used in the design. This circuit used resistors to average the differential outputs and compares the result with common-mode voltage using a differential pair. This technique reduces the voltage error caused by the non-linearity of the differential pair. This allows having more voltage swing without a significant offset.

The folded-cascode op-amp with class AB output stage is taken partly from (Ge). It is similar to the previous op-amp except the output stage is Class AB. This variation is also tried due to the fact that class AB with push-pull output stage has a better trade-off in the rail-to-rail operation compared to class A output stage. Another advantage of class AB output stage is, it has a lesser power consumption and distortion. Also, it can drive the resistive loads which a simple folded-cascode cannot do. The circuit of folded-cascode with class AB output stage is shown in Figure 5-14. It has transistors M18, M19, M20 and M21 that form floating current source to bias the class AB stage. Due to the stability issues there is always a compensation required and that is provided by the Miller compensation.

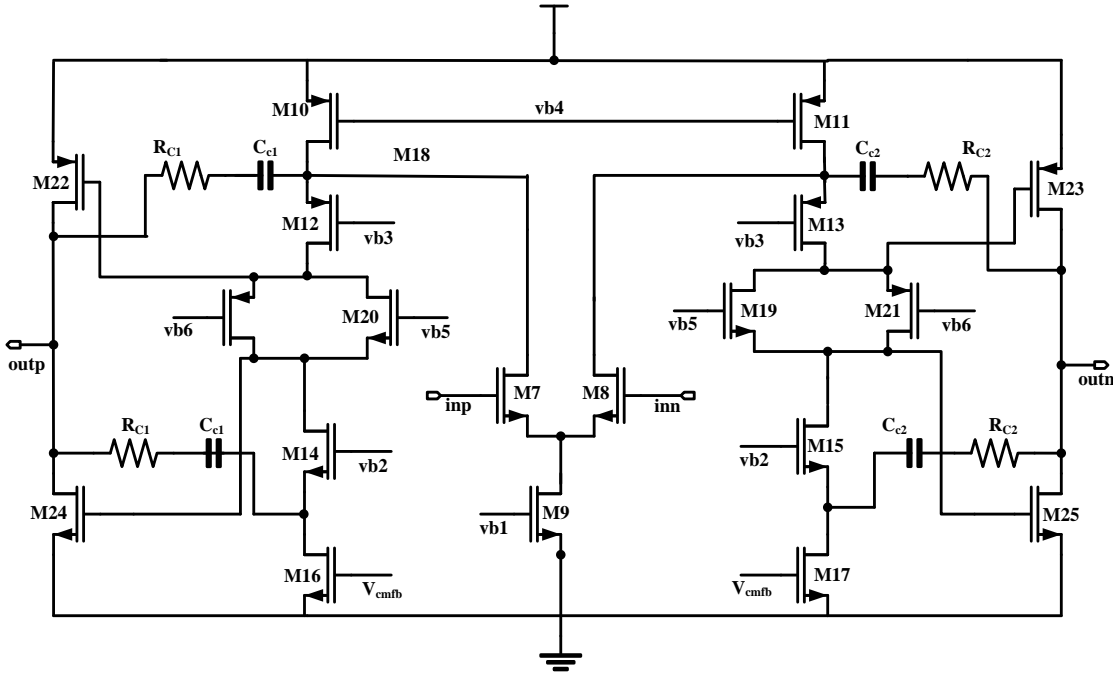


Figure 5-14 Folded-cascode op-amp with Class AB output stage

Little changes were made to the bias circuit from the previous one and are shown in.

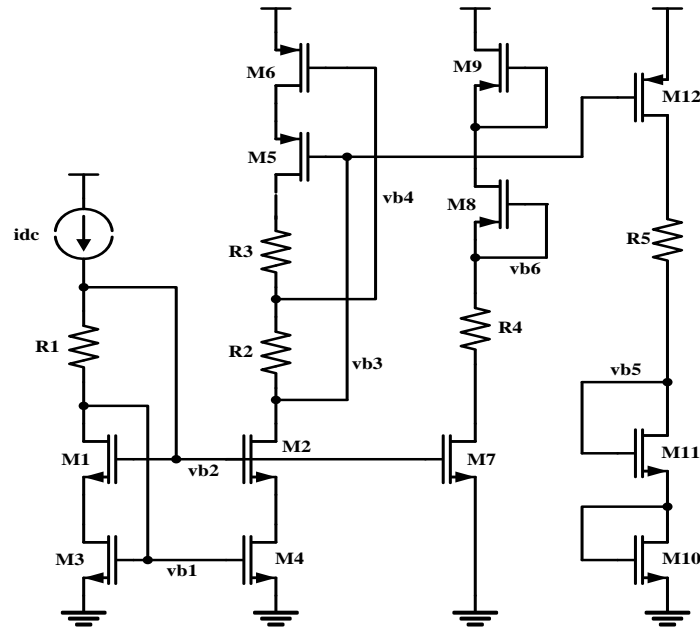


Figure 5-15 Biasing Circuit of the Folded-cascode op-amp with Class AB output stage

The CMFB circuit used in the above discussed op-amp is the same as the previous one.

5.4.2 OP AMP SIMULATION RESULTS

The two-stage folded-cascode op amp with Class-A output stage is simulated in open-loop configuration. The DC open-loop gain of the op amp is found out to be 75.97 dB. The unity-gain frequency is at 54.9 MHz with a phase margin around 63°.

The GBW product of the op-amp is 54.66 MHz and the dominant pole is at 8.1 kHz. The current consumed by the op amp is 421.1 μA . The power consumption of the op-amp is 631.6 μW at 1.5 V power supply.

The 1% settling time of the op amp is found out to be 54 ns. Slew rate is 28.1 V/ μs .

Also the CMRR and PSRR of the op amp were calculated and the op amp seems to be performing well. The graphs Figure 5-17 show the gain and phase plots and Figure 5-19 show the Settling time and Slew rate of the two stage folded-cascode op amp.

Figure 5-22 shows the corner simulation (in 6 corners) of the designed op amp. The worst case corner is the slow-low-gain corner (125°C and 1.42V), where the gain of the op.amp drops to 69 dB (requires 74 dB for a 12-bit ADC). All the other cases are fine providing 74 dB or more gain. The other parameters like phase margin and UGF are not affected by the corners.

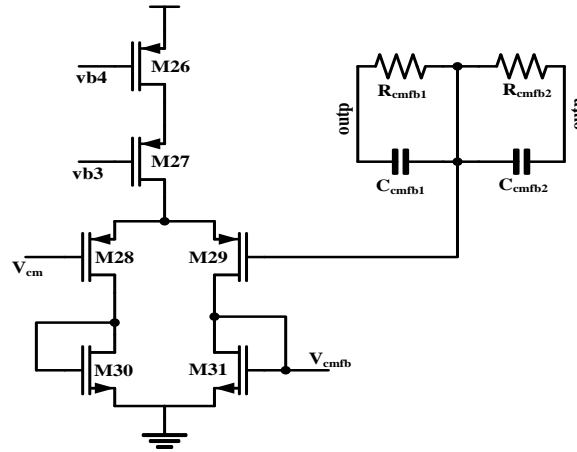


Figure 5-16 Continuous-time CMFB Circuit

The two-stage folded-cascode op amp with Class-AB output stage is simulated in open-loop configuration. The DC open-loop gain of the op amp is found out to be 78.1 dB. The unity-gain frequency is at 64.59 MHz with a phase margin around 64.58°.

The GBW product of the op-amp is 55.75 MHz and the dominant pole is at 6.89 kHz. The current consumed by the op amp is 325.3 μ A. The power consumption of the op-amp is 488 μ W at 1.5 V power supply.

The 1% settling time of the op amp is found out to be 45 ns. Op amp slew rate is 36 V/ μ s.

Parameters	Folded-Cascode op-amp with Class A output stage	Folded-Cascode op-amp with Class AB output stage
Power Supply (V_{DD})	1.5 V	1.5 V
Open-loop DC Gain	75.97 dB	78.15 dB
Unity Gain Frequency	54.99 MHz	64.51 MHz
Phase Margin	63.05°	64.58°
Gain-bandwidth (GBW)	54.66 MHz	55.75 MHz
CMRR	103 dB	-
Positive PSRR	122 dB	-
Negative PSRR	97 dB	-
Current Consumption	421.1 μ A	325.3 μ A
Power Consumption	631.6 μ W	488 μ W
Slew rate	28.1 V/ μ s	36 V/ μ s
Settling time (1%)	54 ns	45 ns

Table 5-3 Simulated Op amp Parameters

The worst case corner is the slow fast corner, where the gain of the op.amp drops to 66 dB (requires 72 dB for a 12-bit ADC). All the other cases are fine providing 72 dB or more gain. The other parameters like phase margin and UGF are not affected by the corners.

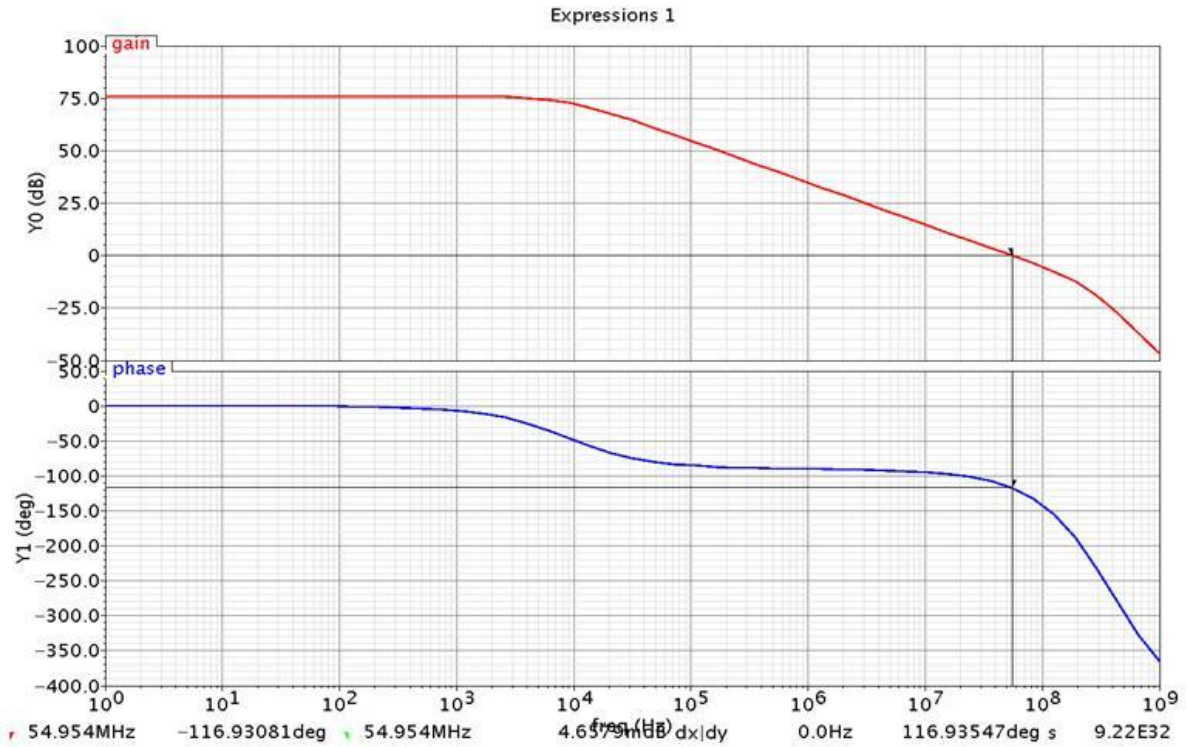


Figure 5-17 Gain and Phase Plots of Folded-cascode op amp with class A output stage

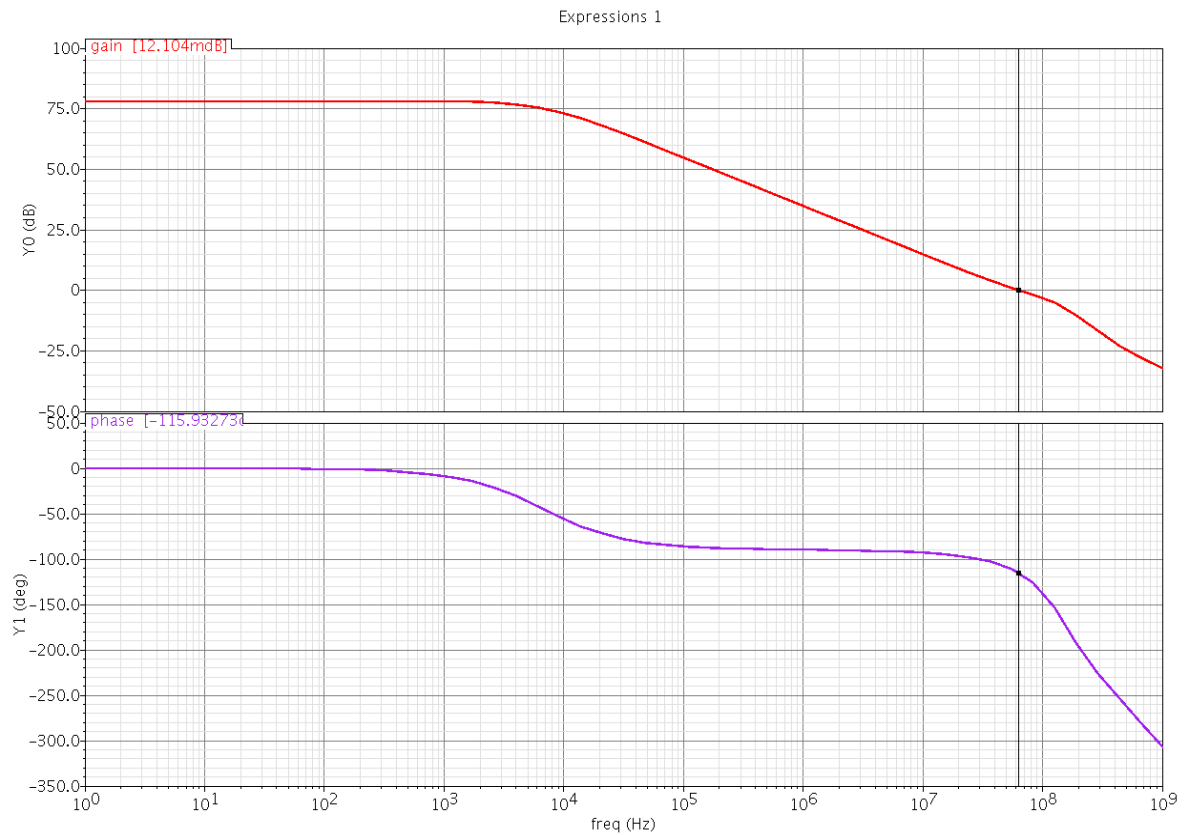


Figure 5-18 Gain and Phase Plots of Folded-cascode op amp with class AB output stage

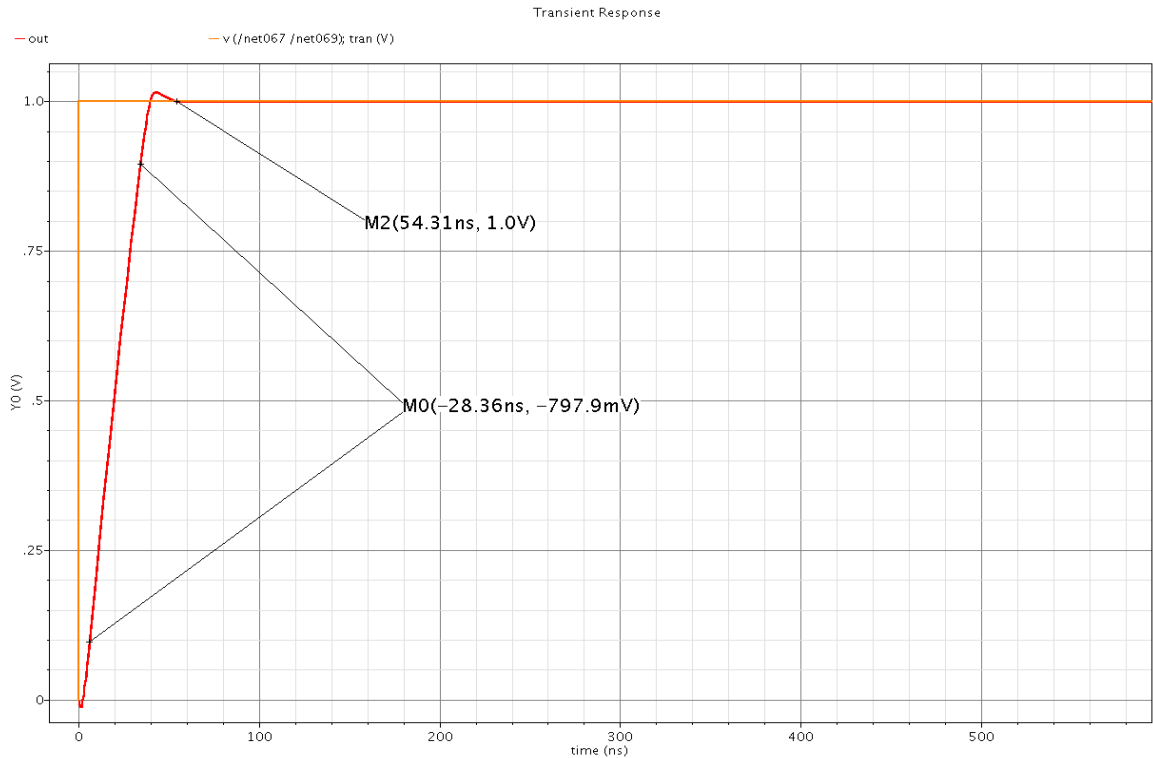


Figure 5-19 Graph showing Slew rate and Settling time of Folded-cascode op amp with class A output stage

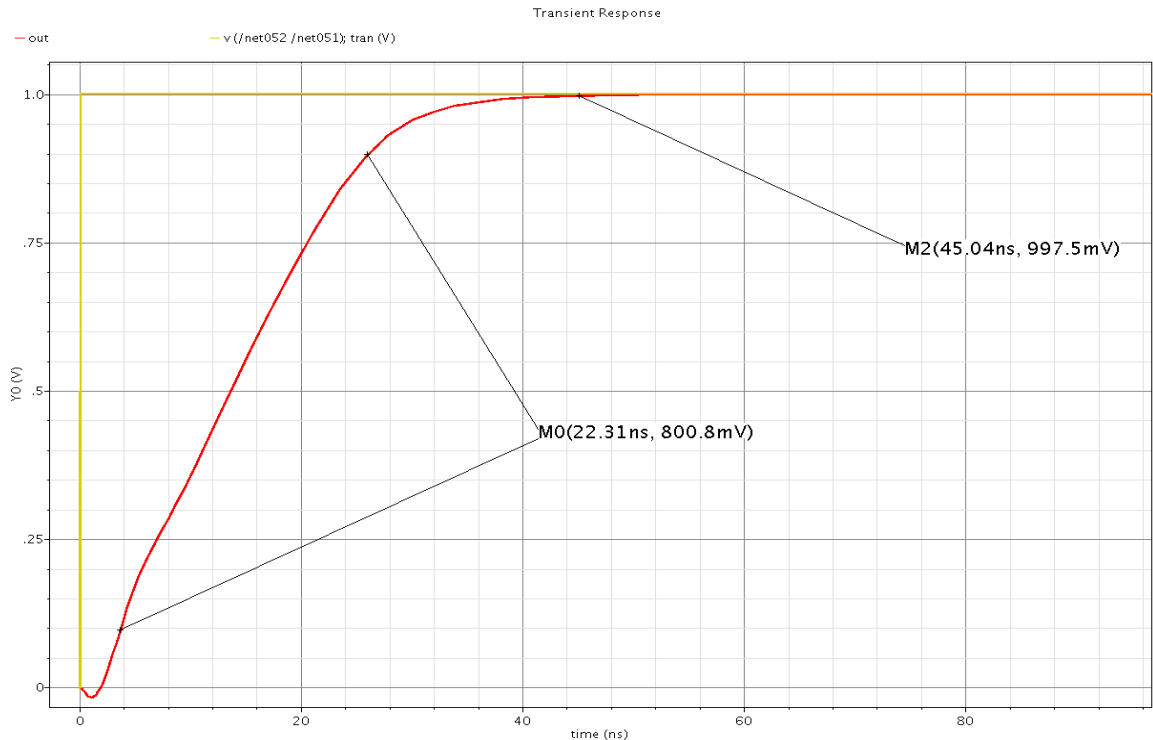


Figure 5-20 Graph showing Slew rate and Settling time of Folded-cascode op amp with class AB output stage

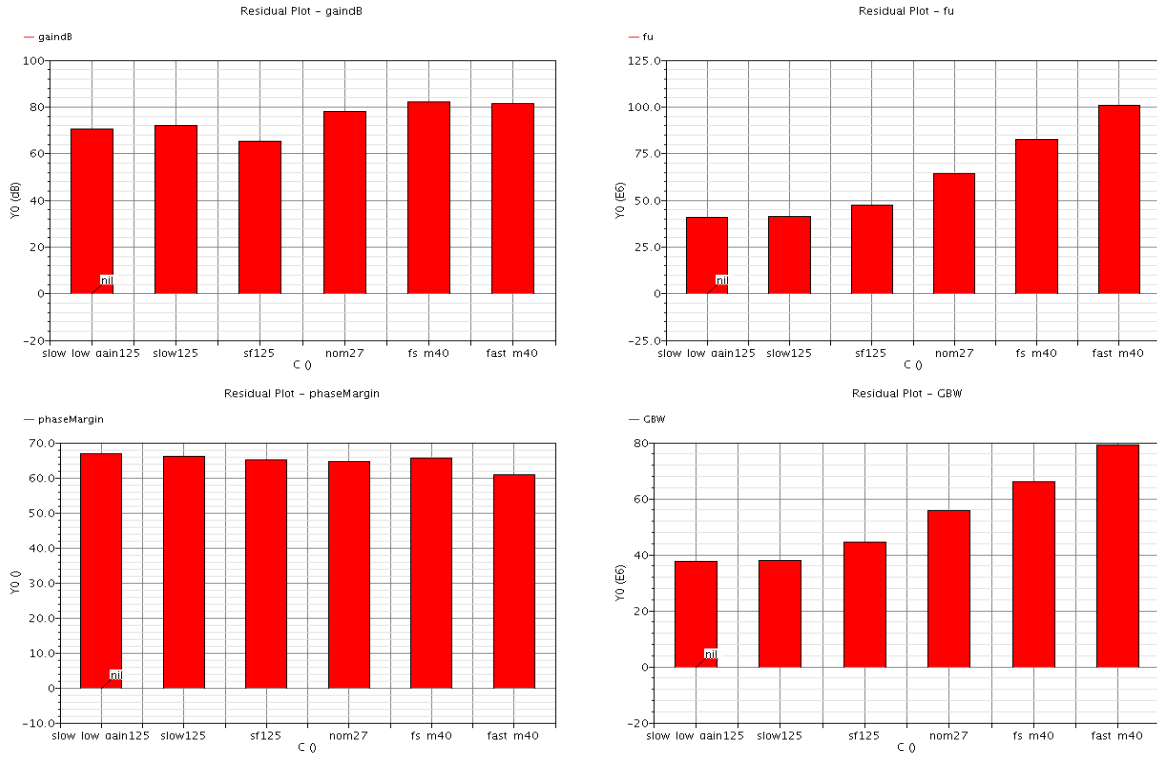


Figure 5-21 Two stage Folded-cascode op-amp with class AB output stage simulation results at the corners

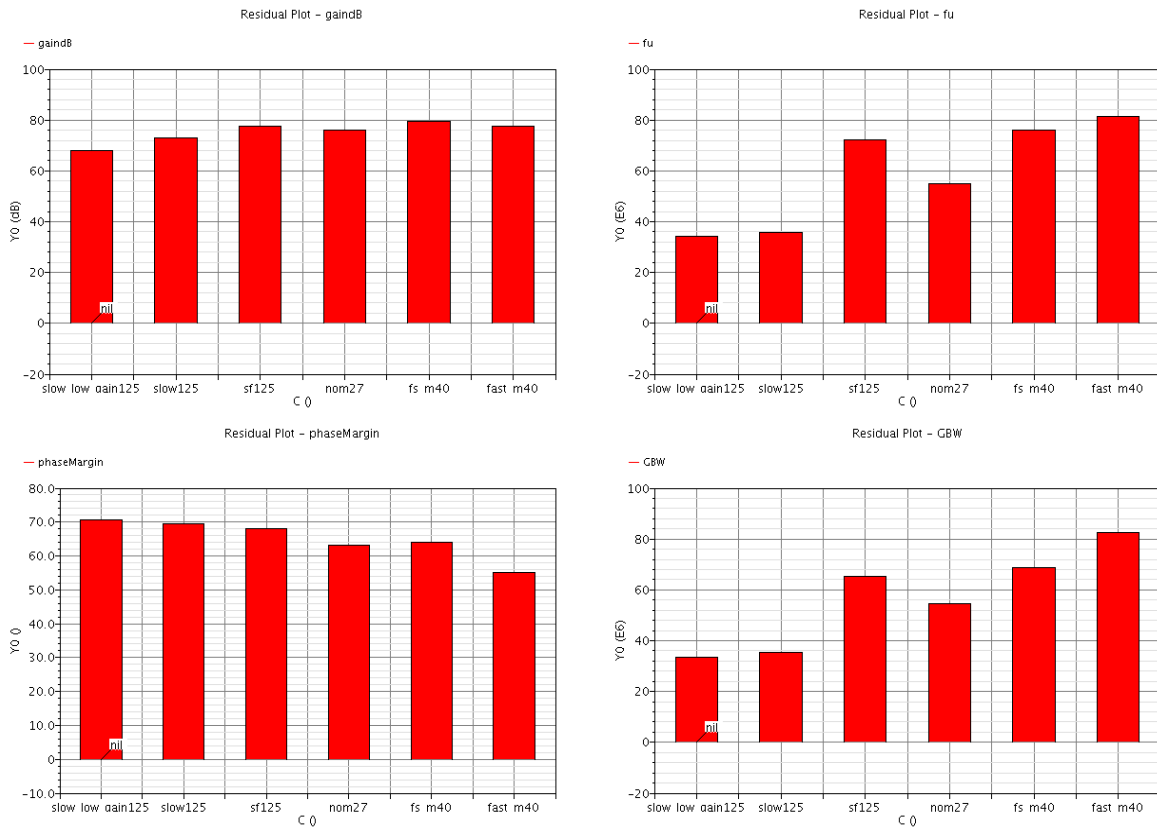


Figure 5-22 Two stage Folded-cascode op-amp with class A output stage simulation results at the corners

5.5 RESIDUAL AMPLIFIER/GAIN STAGE

Residual Amplifier is the last stage of the design. This stage generates the residue signal required as the input to the next stage. This stage again similar to a SHA stage consists of a simple sample-and-hold circuit followed by the op amp. The op amp is the similar design used in the SHA stage with no changes. For op amp design refer to Operational Amplifier. The SHA stage consists of sampling and feedback capacitors along with the switches to perform SHA operation. In addition the analog inputs come from the DAC switch. They are connected to C_{s_RA} but in evaluation phase. The input from the SHA stage is sampled onto the sampling and feed-back capacitors at the same instant and during the evaluation phase the difference of input signal from SHA and signal from DAC are transferred onto feed-back capacitor. This operation performs the multiplication-by-two and generates the residue.

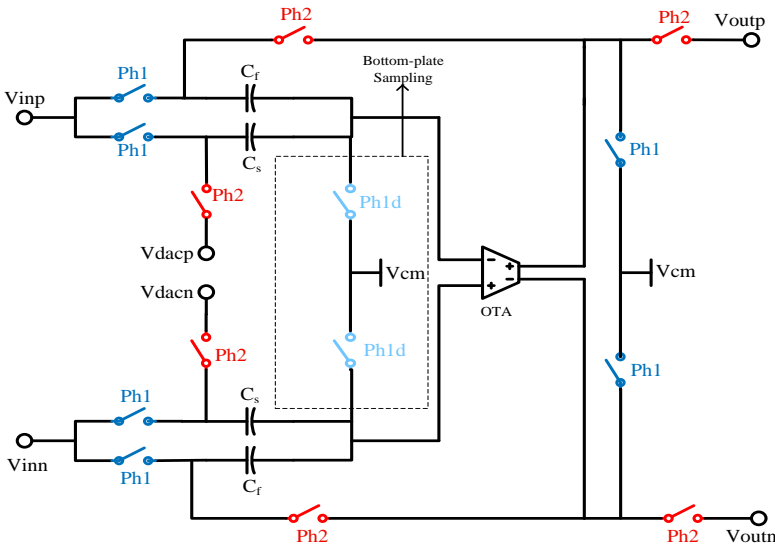


Figure 5-23 Schematic of Residual Amplifier without using CLS Technique

In this design Residual Amplifier with and without CLS technique was made similar to SHA. They are discussed in the following sections. For the schematic and working of this technique refer to 4.3.5.

Also, the Residual Amplifier without the CLS technique is designed. The working is similar to the CLS technique but with no extra clock phases and capacitors. It works in two phases: sampling phase ph1 and evaluation phase ph2. During the sampling phase input is sampled onto both the capacitors C_s and C_f . And, during the evaluation phase analog voltage from the DAC switch is sample onto C_s . At the same time the charge on C_s is transferred onto C_f . At the end of evaluation phase the effective charge at the output (if $C_s=C_f$) is

$$V_{out} = 2V_{in} - V_{dac}$$

(5.3)

In this way the Residual Amplifier calculates the residue voltage. This voltage is transferred as the input to the next stage and consequently for the output bit calculation. The performance comparison of both the methods and designs is shown in Circuit Performance.

5.6 SUMMARY

This chapter discussed the design of various blocks at transistor level that are involved in the design of ADC. Design of Non-overlapping clock phase generator along with its simulation results was shown. This Non-overlapping clock phase generator is used for dual purpose. It generates 6 different phases of clocks that are required by both RSD architecture and also CLS RSD architecture. The clock generator design is little tricky as it involves the generation of many different phases.

Also, the design of Residue Amplifiers for both RSD method and CLS method were shown. The design of the Residue amplifier for CLS method is little more complicated as it involves some more capacitors and switches to operate them and extra clock phases to control the switches.

Design of Folded-cascode op-amp with Class-A and Class-AB output stages along with the simulation results were discussed. Results showed that the op-amp with class-AB output stage is better compared to the op-amp with class-A output stage. Both the output stages have their own advantages and disadvantages.

Also, the design of a low-power voltage comparator was discussed. This comparator was used in the sub ADC block of the design. The results of the comparator showed good performance with a low offset (though offset is not a problem in this architecture). Also, this comparator was compared with the comparator from the previous version. The results of the comparisons were also shown.

Apart from these design implementations of various blocks like Differential comparator, DAC switch and SHA were shown. The differential comparator is a switched-capacitor implementation. This architecture was chosen for a better accuracy. DAC switch comprises of simple transistors and this design did not pose any serious problems. SHA implementation comprises of a charge redistribution scheme. Also, the SHA was developed for the CLS method.

6 CIRCUIT PERFORMANCE

This chapter shows various simulation results of the conventional RSD converters and also the RSD converters employing CLS technique.

The graph below shows the converter result of RSD cyclic ADC for an input of -100mV and a sampling frequency of 100 Ksps. The plots of residues from SHA and Residue amplifier can also be seen.

In the residue plot of SHA the green lines are marked at +250 mV and -250 mV which are the threshold voltages of the two differential comparators. When the residue is out of the comparison range, the comparators bring them back into the convergence domain.

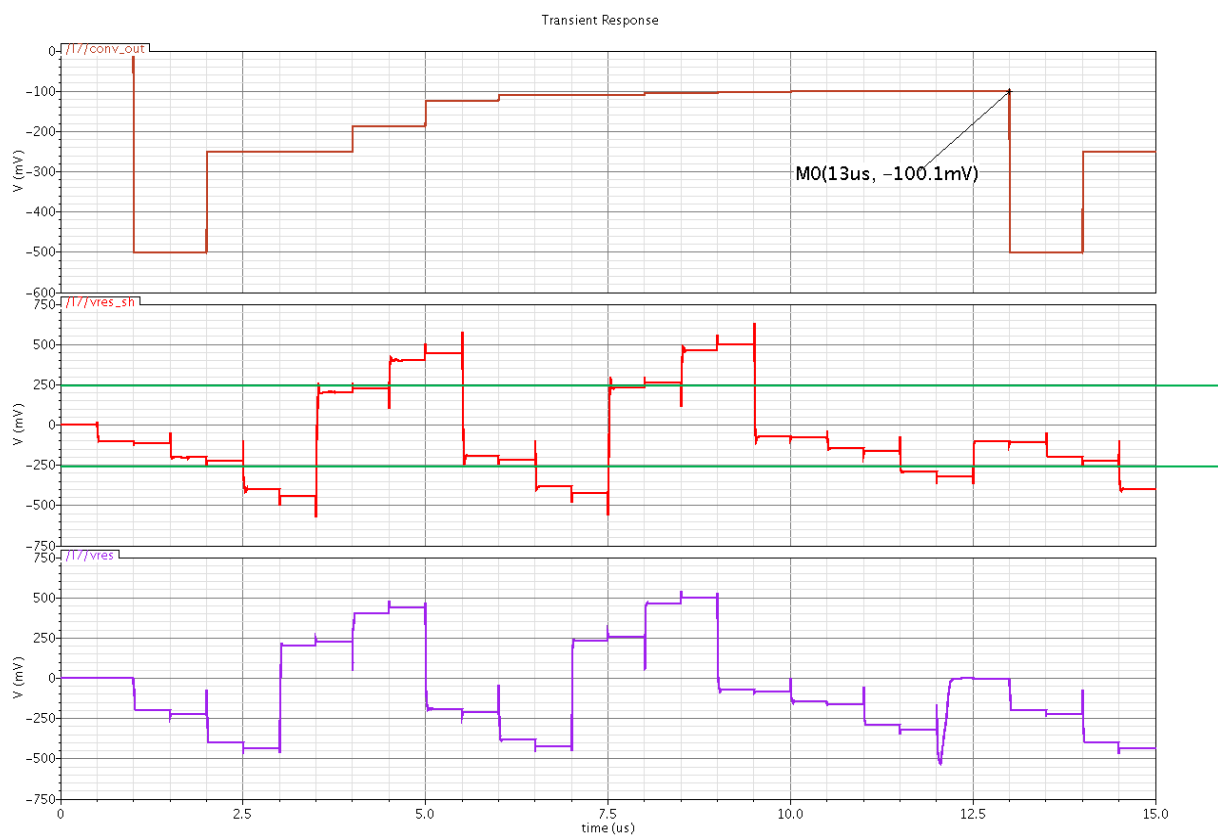


Figure 6-1 Simulation Result (From Top: Conversion Result, SHA Residue, RA Residue) –of RSD cyclic ADC with an input of 100 mV@100 Ksps without CLS Technique

Below figures (Figure 6-2 to Figure 6-5) compare the CLS technique and the conventional RSD technique at lower (100 Ksps) and higher (1 Msps) sampling rates and for different voltages.

The CLS technique at higher sampling rates shows an error of more than 1 LSB and is evident from the output voltage detected by the converter.

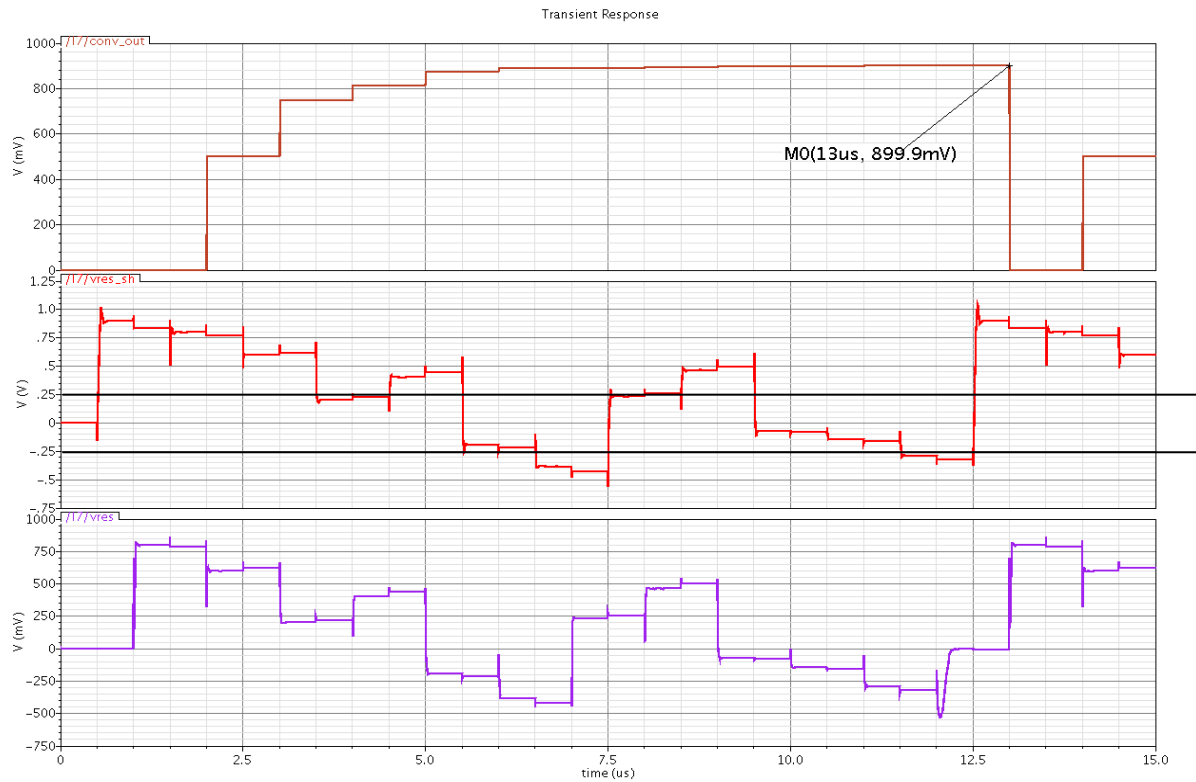


Figure 6-2 Simulation Result of Cyclic ADC with an input of 900 mV@100 Ksps without CLS Technique

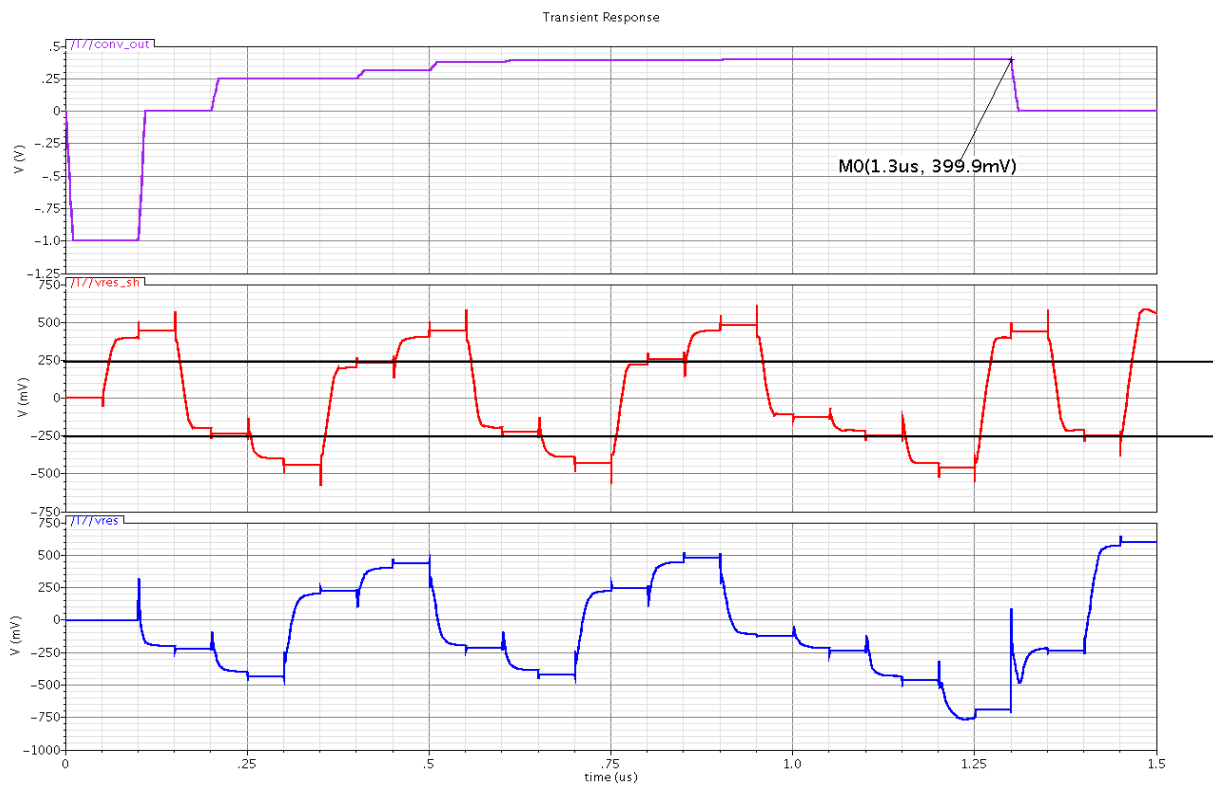


Figure 6-3 Simulation Result of RSD cyclic ADC with an input of 400 mV@1 MspS without CLS Technique

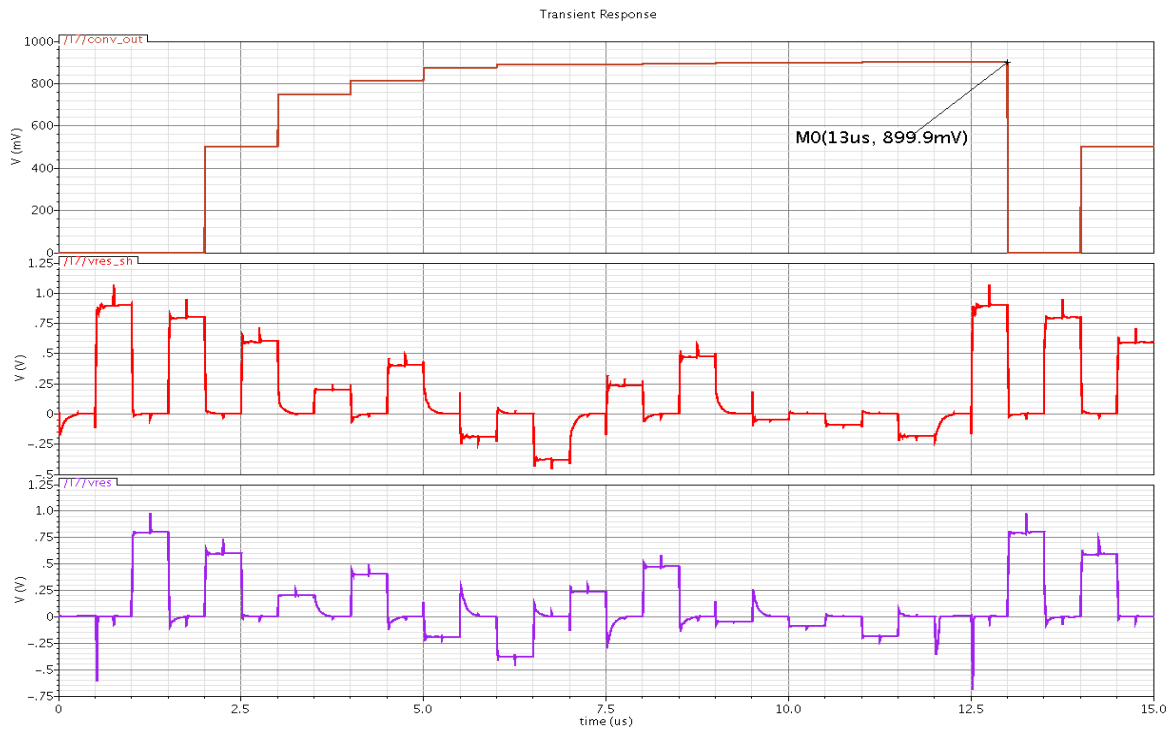


Figure 6-4 Simulation Result of RSD cyclic ADC with an input of 900 mV@100 Ksps with CLS Technique

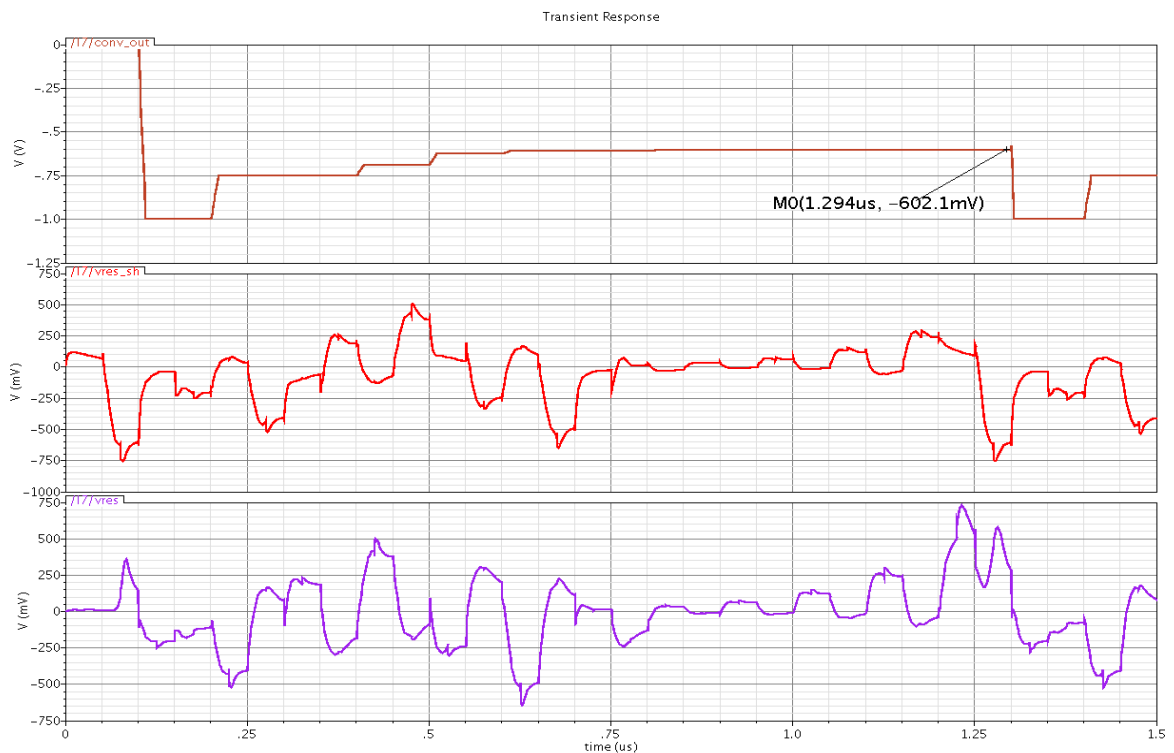


Figure 6-5 Simulation Result of RSD cyclic ADC with an input of -600 mV@1 Msp with CLS Technique

Below figures Figure 6-6 to Figure 6-8 show the corners simulations of the conventional RSD cyclic ADC at 100 mV input voltage and a speed of 100 Ksps. It is tested over six corners and it seems the ADC is fine in all the corners.

Figure 6-7 shows the corners simulation for the RSD cyclic ADC for 100 mV input at 100 Ksps speed. There seems to be an error of more than 1 LSB in two corner cases (1.58 V, -40°C and 1.58 V, 125°C).

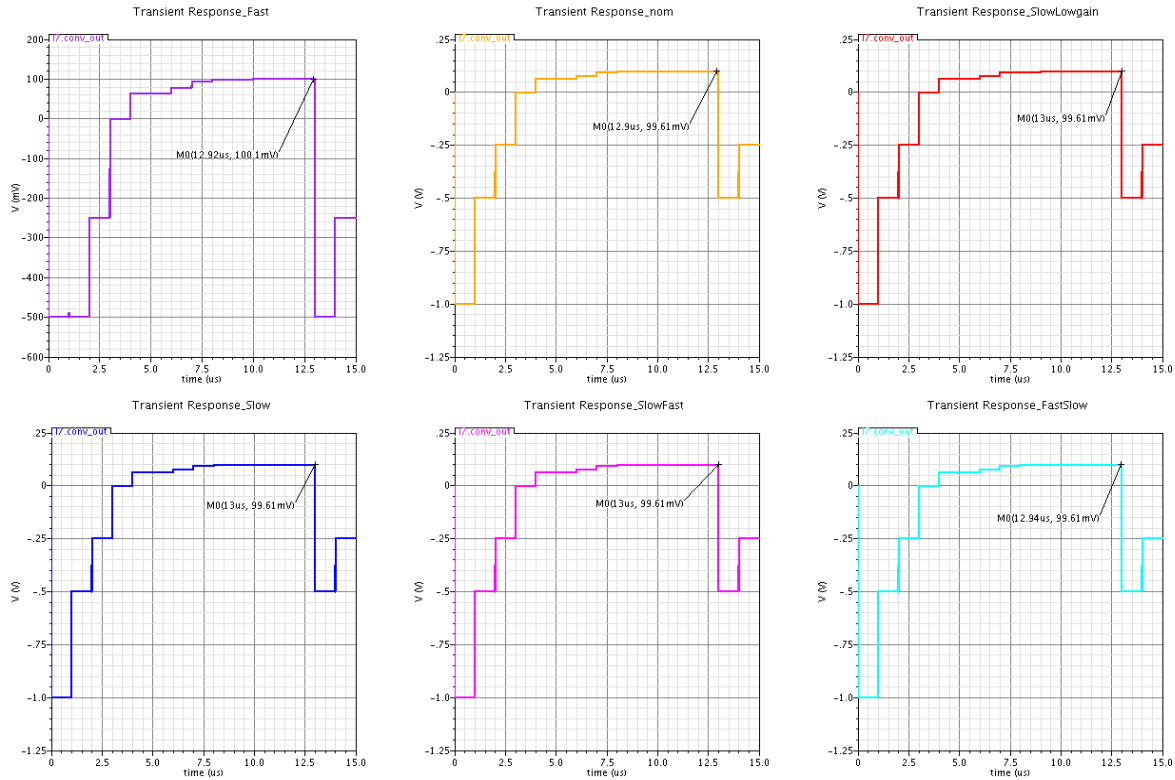


Figure 6-6 Corners Simulation Result of RSD cyclic ADC with an input of 100 mV@100 Ksps without CLS Technique

Figure 6-8 shows the corners simulation for conventional RSD cyclic ADC of 100 mV input and 1 Msps sampling frequency. This case also works well for all the corners except one corner (125°C, 1.42 V). The error is greater than 1 LSB at this corner.

Table 6-1 shows the table of expected results and simulated results. It also compares the parameters of conventional and CLS RSD cyclic ADCs. CLS RSD cyclic ADC consumes less power than the conventional technique due to the fact that it requires an op amp with low gain. The op amp used in the CLS technique has a DC open-loop gain of 46 dB where as the op amp in conventional RSD cyclic ADC has a gain of 76 dB approximately.

Also, the performance of conventional RSD cyclic ADC is better than that of CLS RSD cyclic ADC at higher speeds of operation. Another drawback of CLS method is that it cannot work with a high gain op amp. Due to the increased number of capacitors in CLS method there can be mismatches between them limiting the performance of ADC.

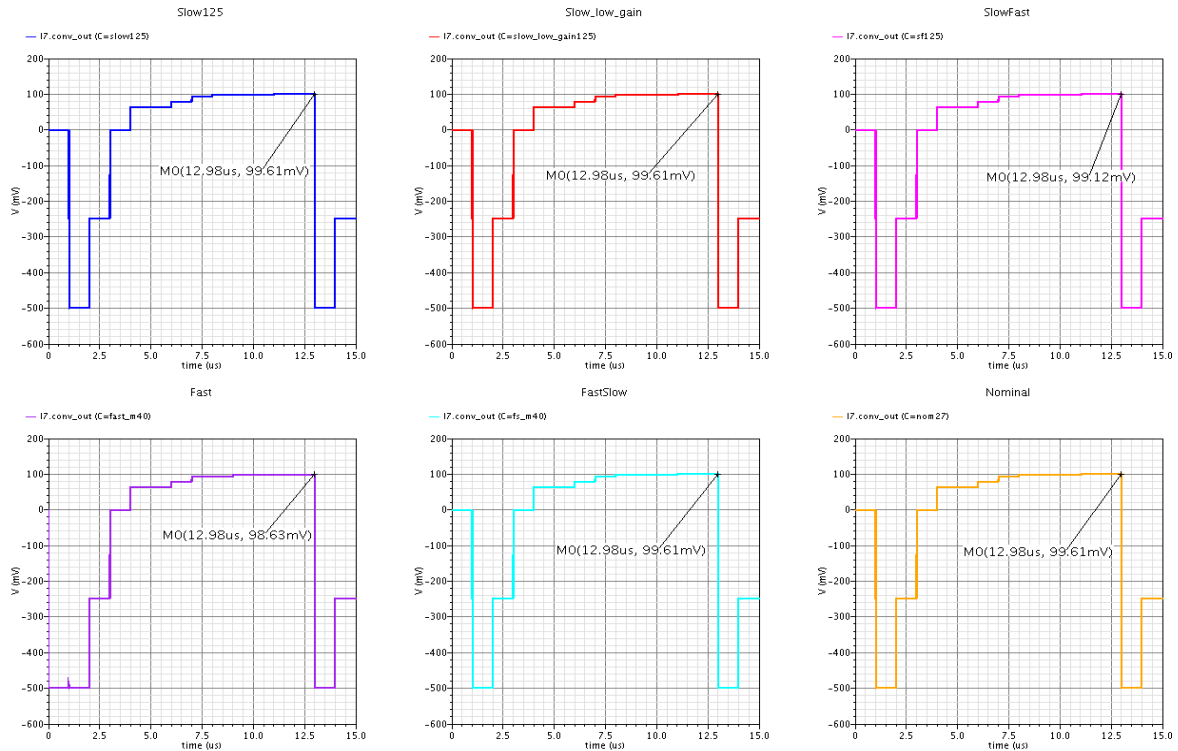


Figure 6-7 Corners Simulation Result of RSD cyclic ADC with an input of 100 mV@100 Ksps with CLS Technique

6.1 SUMMARY

This chapter showed the simulation results of the Cyclic ADC block. The simulation results of RSD cyclic ADC and CLS cyclic ADC are also compared. The corners simulations for the RSD cyclic ADC were also shown.

The simulated results of the prototype ADCs were shown in the tabular column. This performance comparison shows that the RSD cyclic ADC is better compared to the CLS. This is because of the performance of the op-amp and this op-amp is accurate in the case of RSD ADC compared to the op-amp in CLS ADC. So an improved op-amp must be replaced with the existing one that is used for the CLS method.

This ADC was simulated for the DC inputs and so the INL and DNL performances were not known. The designed ADC was checked for the minimum frequency and maximum frequency inputs. The ADC with the CLS method is also verified in the similar fashion.

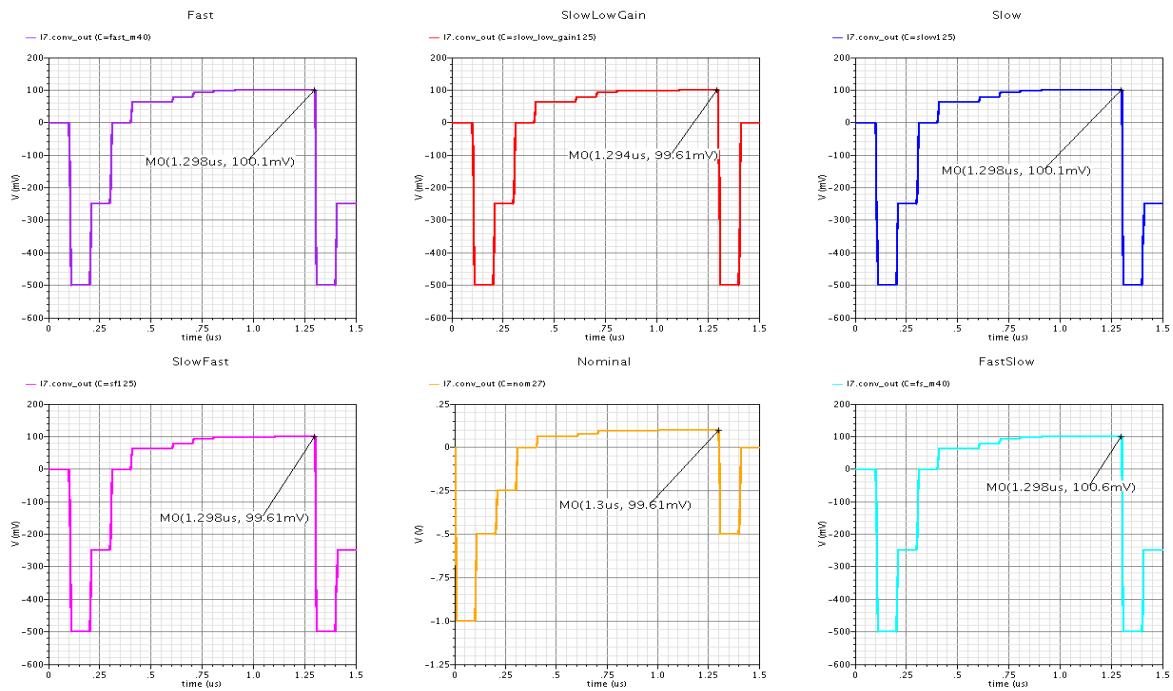


Figure 6-8 Corners Simulation Result of RSD cyclic ADC with an input of 100 mV@1 Mps without CLS Technique

	Expected	Simulated with Conventional RSD cyclic ADC	Simulated with CLS RSD cyclic ADC
Process Technology	130 nm	130 nm	130 nm
Resolution	12-bits	12-bits	12-bits
Conversion Rate	Up to 1 Mps	Up to 1 Mps	Up to 1 Mps
Input Frequency	Up to 450 kHz	Up to 450 kHz	Up to 450 kHz
Power Supply	1.5 V	1.5 V	1.5 V
Reference Voltage	1 V	1 V	1 V
Power Consumption	1 mW @1 Mps	1.24 mW@1 Mps	870 μ W@1 Mps
Input Range	-1 V to +1 V	-1 V to +1 V	-1 V to +1 V (output with errors greater than 1 LSB)

Table 6-1 Table showing the Simulation Results comparison between conventional and RSD cyclic ADCs

7 CONCLUSION AND FUTURE WORK

This chapter presents the summary of the whole Thesis work. The contributions to the design and the possible future work involved are described briefly.

7.1 CONCLUSION

Cyclic analog-to-digital converters (ADCs) are mostly found in portable devices, sensing and biomedical applications where medium to high resolutions are required at medium conversion speeds with minimum die area costs involved and having lower power consumption. The cyclic ADC architecture is in close resemblance with the pipelined ADC architecture. Unlike pipelined ADCs where the residue voltage is propagated through successive stages, an N-bit cyclic ADC utilizes the same hardware N-times to obtain the N-bit digital word. Due to the hardware reuse cyclic ADCs have minimum die area and hardware complexity. However, in terms of power dissipation, compared to that of pipelined ADCs, traditional cyclic ADCs are not comparable. Pipelined ADCs have greatly benefited from many low power methods implemented in between the stages, which is not directly applicable to cyclic ADCs.

In this thesis, two low-power techniques to implement a cyclic ADC are discussed. These are conventional RSD method and CLS method. In the conventional RSD method the power consumption of the ADC is 1.24 mW for a resolution of 12-bits and a speed of 1 Msps in 130 nm CMOS process.

Apart from the RSD method, there is CLS technique that was also used to implement the cyclic ADC. This technique uses the level shifting capacitors and three non-overlapping clock phases to implement the ADC. This method had stringent requirements on the settling times and slew rates of the op-amp and so could not be fully developed. But this technique is more power efficient at the lower sampling rates compared to the traditional RSD method.

In this thesis, two op-amps were also designed. One is the two-stage Folded-cascode op-amp with class A output stage and the other is with class AB output stage. Both op-amps were tested within the conventional RSD cyclic ADC as they were designed to fit into RSD cyclic ADC. Both the op-amps showed promising results with class AB output stage op-amp gaining the upper hand. This is due to the fact that the class AB output stage is flexible for rail-to-rail operation. Also, class AB output stage consumes less power and has less distortion compared to the class A output stage. The folded cascode op-amp with class A stage consumes 630 μ W power with a gain of 75.97 dB and a phase margin of 63° and GBW of 54.6 MHz. Whereas, op-amp with class AB output stage consumes only 480 μ W with a gain of 78.1 dB and a phase margin of 64.5° and GBW of 55.75 MHz.

7.2 FUTURE WORK

There are many future possibilities concerning the improvement of the design. Apart from the improvements, there is some work left to be done in the design.

- The design of the Cyclic ADC has been verified by a DC input signal until now. All the simulations were done using a DC input. Though this test gives us the rough

approximation of what is happening with the ADC, the Cyclic ADC has to be verified in other terms. That is, the static and dynamic characteristics of the ADC have to be evaluated. These characteristics include SNDR, ENOB, THD, INL, DNL, etc., FFT (Fast Fourier Transform) analysis has to be carried out using coherent sampling phenomenon given by

$$\frac{f_{in}}{f_s} = \frac{N_{cycles}}{M_{samples}} \quad (7.1)$$

The samples after the simulation have to be collected using a file writer and is processed in MATLAB using simple programs to find out different characteristics associated with the performance of the ADC.

- After the evaluation of the above parameters, the schematic has to be laid out. The Layout of the ADC involves the design of all the new blocks starting from Analog Switch, Comparator to Op-amp design. Also the Layout has to be done for the clock generator. After the layout is completed, parasitic extraction is to be done and once again the ADC's performance has to be verified against all the parameters listed above.
- The performance of folded-cascode op-amp with class-A output stage is not up to the mark in all the corners simulations. Though all the parameters like phase margin and GBW are looking good, the gain of the op-amp drops less than the required in slow-low-gain corner. This problem still has no effect on the Cyclic ADC's performance yet. But, it can prove problematic at the later stages of the design, may be after the post-layout simulations.

The future work that can be carried out in terms of improvement of this design may include

- **Op-amp Reuse technique:** This is one suggested method to decrease the power consumption of the Cyclic ADC as the op-amp is the most power hungry block in the design consuming more than 80% of the total power. In this method, the op-amp can be shared between the SHA and the Residue amplifier. This is possible only when both of them operate in different clock phases. So that, a single op-amp can be reused eliminating the need of having another one. But care has to be taken while designing this technique as there may be other factors that can diminish the performance of the ADC.
- **Two-stage Cyclic ADC:** The conversion speeds of the ADC can be improved using a two-stage design as this requires only half the number of clock cycles ($N/2$) to obtain an N-bit conversion. Another advantage of this technique is that the SHA can be eliminated from the design. This is due to the fact that the Residue Amplifier in the first stage can act as the SHA for the succeeding stage Residue Amplifier and vice versa. Using two residue amplifiers to sample and hold the signal instead of SHAs can help reduce the power consumption too.

These improvements discussed above can be implemented on the design to obtain robust, flexible and even low power consuming results.

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