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A Silicon-Organic Hybrid Voltage Equalizer for Supercapacitor Balancing

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***Abstract*—Cell voltage equalizers are an important part in electric energy storage systems comprising series-connected cells, for example, supercapacitors. Hybrid electronics with silicon chips and printed devices enables electronic systems with moderate performance and low cost. This paper presents a silicon-organic hybrid voltage equalizer to balance and protect series-connected supercapacitor cells during charging. Printed organic electrochemical transistors with conducting polymer poly(3,4-ethylenedioxythiophene): poly(styrene sulfonate) (PEDOT:PSS) are utilized to bypass excess current when the supercapacitor cells are fully charged to desired voltages. In this study, low-cost silicon microcontrollers (ATtiny85) are programmed to sense voltages across the supercapacitor cells and control the organic electrochemical transistors to bypass charging current when the voltages exceed 1 V. Experimental results show that the hybrid equalizer with the organic electrochemical transistors works in dual-mode, switched-transistor mode or constant-resistor mode, depending on the charging current applied (0.3 mA to 100 mA). With the voltage equalizer, capacitors are charged equally regardless of their capacitances. This work demonstrates a low-cost hybrid solution for supercapacitor balancing modules at large-scale packs.**

***Index Terms*—Hybrid electronics, organic electrochemical transistors, printed electronics, supercapacitor balancing, voltage equalizer**

I. Introduction

PRINTED and organic electronics [1, 2] offers a route to a low-cost manufacture platform that enables electronic systems with the ability for wide distribution of, for instance, devices for internet of things (IoT). However, printed components, [3] especially with organic/polymer functional materials, suffer from low speed and large device variations due to the relatively low mobility and instability to ambient environment. On the contrary, conventional silicon chips are excellent in terms of speed and stability. The trade-off between the two technologies, printed electronics and conventional silicon chips, enables hybrid electronic systems with both performance/stability and low cost.

Supercapacitors (SCs, also referred to as ultracapacitors, electric-double layer capacitors, etc.), combining moderate capacity (~Farads) and fast charging (1~10 s), are very promising for electric energy storage, where high power density is needed [4]. In order to lower the cost of SC manufacturing, a number of works have been reported on printed SCs [5-7]. For instance, [7] presents environmentally friendly SCs with ionic liquid electrolytes on paper, showing a specific energy of 7 Wh/kg (40% higher than commercially available non-printed SCs). The potential of electrochemical storage cells is limited by the electrochemical window of all components in the cell, electrolytes as well as electrode materials, to low number of volts. As many applications require higher tension, electrochemical storage cells are often connected in series. When serially connected cells are to undergo a large number of charge-discharge cycles, circuits to protect the cells from over- or undervoltage as well as to balance the charge levels are required [8]. The control and balancing circuits can contribute more than 50% of the cost of the entire module of SC packs. To further lower the cost, an all-printed, integrated SC energy storage system including the control and balancing circuits is preferable. However, as stated above, all-printed organic circuits have difficulties in providing fast, accurate, and reliable signal processing ability. Here, we have explored the combined use of printed electronics and surface mounted components, herein termed hybrid solutions, to enable new schemes for integrating electrochemical storage cells with circuits for protection and balancing.

In this work, we propose a silicon-organic hybrid voltage equalizer for supercapacitor balancing, twinning the accuracy/stability of low-cost silicon chips (ATtiny85 microcontrollers) and the large current of printed organic electrochemical transistors (OECTs). Unlike organic field effect transistors, the channel current in OECTs is modulated by electrochemical doping/de-doping via a redox reaction mediated by ions from an electrolyte layer [9, 10]. Thanks to the electrochemical doping, OECTs usually control high current (e.g., up to 1A [11]) at low-voltage, while they also have extremely good printability on non-conventional substrates (e.g., paper or plastic). Therefore, printed OECTs are used as bypassing transistors here, indicating the possibility to fully integrate OECTs and SCs on the same substrate and in the same production line, since conducting polymers

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(PEDOT:PSS), electrolytes and graphite can possibly serve as the active materials in both OECTs and SCs. The built-in analog-to-digital converters (ADCs) in the microcontrollers provide more accurate voltage sensing with much faster speed, compared to organic circuits. Aiming at balancing printed SCs with water-based electrolytes, the microcontrollers in this work are programmed to bypass the charging current when the charging cell voltage is over 1 V and thereby protect the cells against overcharging. By combining a microcontroller with OECTs, we have shown that the hybrid voltage equalizer is able to charge an imbalanced pair of capacitors (6.8 µF and 15 µF) equally. Moreover, the hybrid equalizer was demonstrated to charge a pair of SC cells equally, through constant current charging (100mA). This study combines the accuracy and speed of silicon microcontrollers and the large-current capability of OECTs for SC balancing, paving a road towards low-cost SC-based energy storage systems through hybrid electronics.

This paper is organized as follows. The main components, OECTs and microcontrollers, as well as the compatibility of OECTs and the microcontrollers, are presented in Section II. We present the voltage equalizers implemented with a microcontroller either associated with silicon NMOS transistors (for comparison) or OECTs in Section III. Section IV contains the summary of the silicon-organic hybrid voltage equalizer and concluding remarks.

II. OECTs and Microcontrollers

This section describes the printed organic electrochemical transistors and the ATtiny85 microcontrollers that are used in the experiments as well as their compatibility with the OECTs.

A. OECTs

The OECTs manufactured at Acreo Swedish ICT AB [10] include PEDOT:PSS (poly(3,4-ethylenedioxythiophene): poly(styrene sulfonate)), which acts as the active material in the transistor channel and is patterned by screen printing on a transparent polyethylene terephthalate (PET) film (see Fig. 1a). Carbon, originating from a graphite ink, and silver conductors and contact pads are both screen printed with the purpose of minimizing the overall resistance of the OECT. A water-based electrolyte is then deposited to ensure the ionic connectivity between gate and channel, and the OECT device is finally completed by depositing a PEDOT:PSS-based gate electrode on top of the electrolyte.

The transistor characterization was carried out in controlled environment at a temperature of 20 °C and a relative humidity of 40%RH. An HP/Agilent 4155B semiconductor parameter analyzer and two Keithley 2400 Source Meter units were used for the measurements [10].

Fig. 1b presents the output characteristics of a typical printed OECT. The source electrode was connected to ground and seven different gate-source voltages (V_{GS}) ranging from 0 to 1.5 V (with 0.25 V intervals) were applied to the gate. In each step,

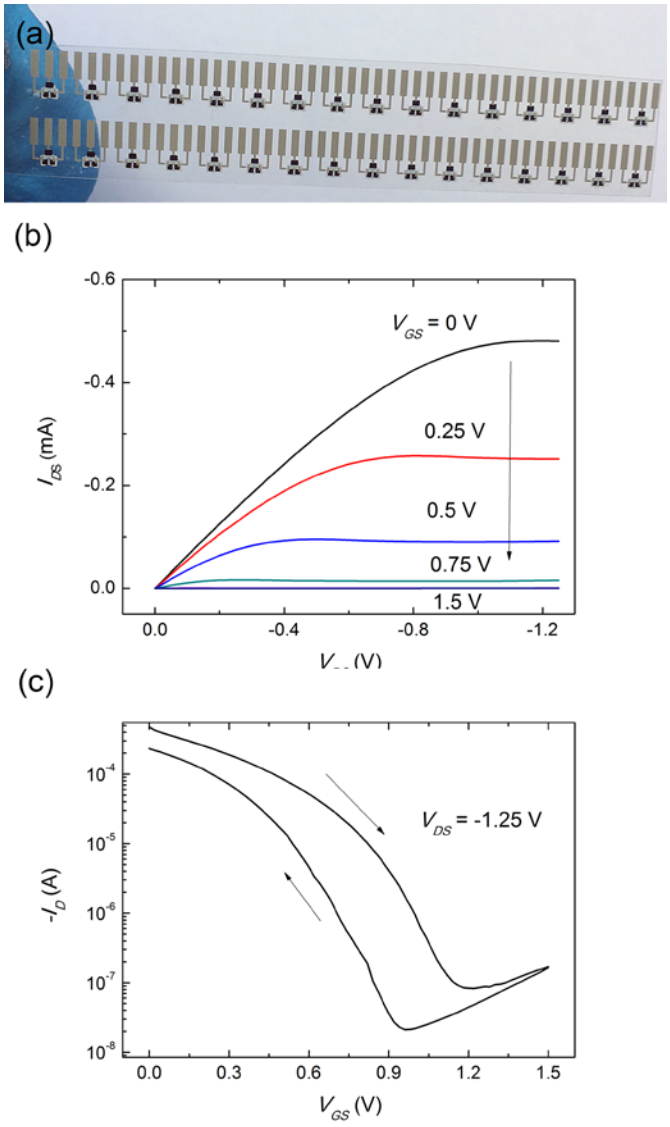

Fig. 1. (a) Printed OECTs on a plastic (PET) substrate. Output (b) and (c) characteristics of a typical printed OECT.

the drain-source current (I_{DS}) was continuously measured while the voltage between the drain and source (V_{DS}) was swept from 0 to -1.25 V. Negative V_{GS} was not applied to avoid over oxidation that may lead to an irreversible damage to the OECTs. Applying a positive V_{GS} drives cations (M^+) from the electrolyte into the channel and in combination with electrons from the drain and source electrodes reduce the PEDOT as follows:

$$PEDOT^+PSS^- + M^+ + e^- \leftarrow\rightarrow PEDOT^0 + M^+PSS^- \quad Eq.\ (1)$$

where e^- are electrons. The reduced $PEDOT^0$ has much lower conductivity than the oxidized $PEDOT^+$, hence the drain-source current (I_{DS}) is modulated by V_{GS}. Normal saturation behaviors in I_{DS} can be seen from the output curves and the current saturation is interpreted as a depletion of the ion-concentration near the electrolyte/channel-interface.

Fig. 1c illustrates the transfer characteristics of the OECT. As shown, when V_{GS} = 0 V, the transistor conducts the maximum current, amounting to approximately 0.5 mA, indicating the OECTs are operated in depletion mode. Increasing the gate-source voltage (V_{GS}) reduces the channel current via the reduction of PEDOT. In this measurement, the drain-source voltage was fixed at V_{DS} = -1.25 V and the V_{GS} was swept from 0 to 1.5 V and back from 1.5 to 0 V, measuring the drain-source current (I_{DS}). The hysteresis that can be clearly seen between the forward and backward sweeps is due to the ion penetration into the bulk of the PEDOT:PSS channel material. The hysteresis reflects the electrochemical kinetic in the OECT operations and depends on the sweep rate of the voltages.

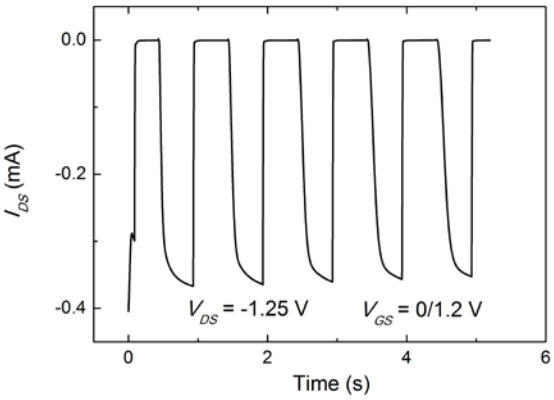

Fig. 2. Switching characteristics of a typical OECT.

The switching speed that defines how fast transistors respond to the gate voltage is an important parameter in logic circuits. Fig. 2 shows the switching characteristics of the OECT, where a pulse between 0 and 1.2 V was applied to the gate of the OECT and the drain-source current (I_{DS}) was measured. The drain-source voltage was fixed at V_{DS} = -1.25 V. It can be seen from the figure that the OFF switching is much faster than the ON switching. This non-symmetric switching is caused by that a reduction front [10] propagates within the PEDOT:PSS film. The reduction front [10] is often beyond the coverage of the electrolyte and residual cations in the reduction front are slow to diffuse back into the electrolyte, when the OECT voltage supply is turned off (V_{DS} = V_{GS} = 0 V). This effect also contributes to the hysteresis shown in Fig. 1(c). The use of carbon-paste as the source and drain electrodes can partly eliminate this non-symmetric switching [10]. It is also noted that the ON-state current in Fig. 2 becomes slightly reduced as a function of time. This is explained by the reduction front that is propagating inside the conducting polymer material and it is a temporary reduction of the current level caused by the continuous voltage supply. The yield of the printed OECTs was quite high (close to 100% in our experiments) and they survived in a 325 h endurance test (over 3400 switching cycles) without significant degradation.

B. ATtiny85 Microcontrollers

The ATtiny85 microcontroller from Atmel is used to program the conditions for balancing (see Fig. 3 for pin configuration). There are five input/output pins: three input pins that are used as analog inputs and two output pins that can be configured either as digital outputs that deliver either *HIGH* (+5 V) or *LOW* (0 V) signals or as analog outputs. The built-in ADCs at the analog input pins offer fast and accurate voltage sensing. The *RESET* pin is used for programming the microcontroller and the *Vdd* pin is the power supply of +5 V.

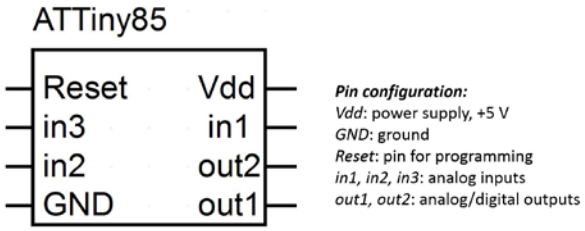

Fig. 3. Pin configuration of ATtiny85 microcontrollers (Amtel Corp., San Jose, CA).

C. Compatibility of OECTs and Microcontrollers

The desired voltage (V_{GS}) for operating the OECTs is 1 V, whereas the digital output voltage of the microcontroller generates *HIGH* (+5 V) or *LOW* (0 V) signals. High V_{GS} will accelerate the degradation of OECTs and may cause permanent damage to the devices. Subsequently, the gap in the operating voltage has to be resolved to make the microcontroller compatible with the OECTs.

Ideally, analog outputs at desired voltages (e.g., 1 V) from microcontrollers could solve this issue. However, the analog outputs of the ATtiny85 microcontrollers are width-modulated pulse (0/5 V). Another explicit solution is to use a voltage divider with two resistors to lower the voltage applied to the OECT gate. *R1* and *R2* in Fig. 4a form the voltage divider. By assigning correct resistor values (e.g., *R1* = 470 kΩ, *R2* = 120 kΩ), the 5 V pulse from the microcontroller can be lowered down to a pulse between 0 and 1 V. In order to demonstrate the successful control of the OECTs through the voltage divider, a source follower with a single OECT and a resistor, *R3* = 120 kΩ, was driven by an ATtiny85 microcontroller through the voltage divider (Fig. 4a). The drain was connected to a -1 V voltage source and the voltage divider was used to control the gate. The voltage at the source (V_S) was measured using an oscilloscope (PicoScope 2000, Pico Technology, United Kingdom). Fig. 4b shows that the output of the microcontroller (V_{out2}, blue dash), a 5 to 0 V pulse, was converted to a 1 to 0 V pulse at the gate (V_G, black line) and the OECT (V_S, red line) was controlled by the voltage divider.

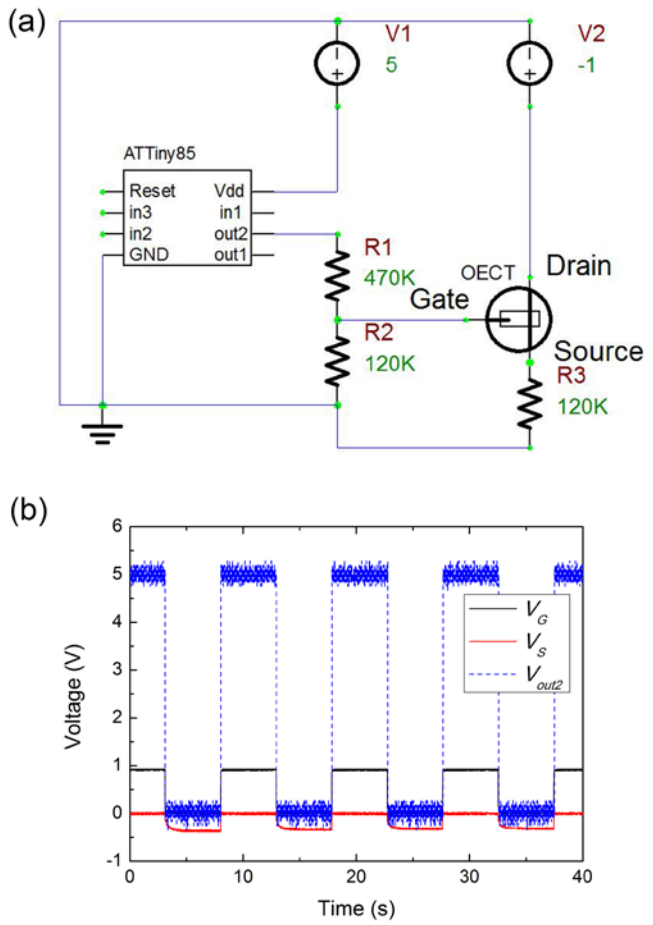

Fig. 4. (a) Circuit schematics of an ATtiny85 driving an OECT through a voltage divider. (b) The measured waveforms of V_G and V_S of the OECT in Fig. 4(a) when the OECT was switched by a pulse given by the *out2* pin of the ATtiny85 in Fig. 4(a).

III. Voltage Equalizers

Voltage equalizers are usually used to eliminate cell voltage imbalance for series-connected energy storage cells (e.g. lithium-ion batteries or SCs) [12, 13]. This section describes two voltage equalizers with ATtiny85 microcontrollers and transistors for passive balancing of the voltage across the SC cells. The voltage equalizer, with the microcontroller and NMOS transistors, was implemented to verify the circuit design and the functionality of the programmed microcontroller. The proposed hybrid voltage equalizer, using the OECTs instead of the NMOS transistors, was developed and its capability to equally charge imbalanced capacitors/SCs was demonstrated.

A. Microcontroller and NMOS transistors

Fig. 5 presents the voltage equalizer comprising of the microcontroller, two silicon NMOS transistors (*M1* and *M2*, e.g., 2N7000 (DioTec Semiconductor, Germany) or BSP295 (Infineon Technology, Germany) depending on the bypassing current), and a two-cell supercapacitor (940 mF of each cell for a total capacity of 470 mF, Murata Electronics, Japan). All the components are surface-mounted through anisotropic conductive paste on a flexible plastic substrate and all the interconnects consist of aluminum patterned by dry etching.

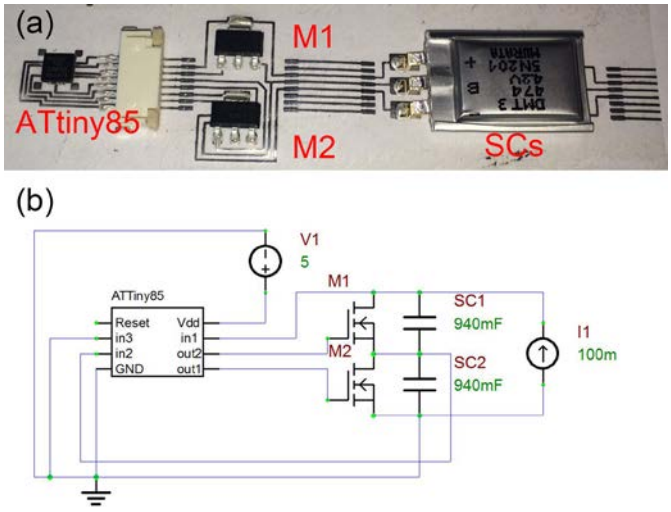

Fig. 5. (a) A voltage equalizer for two-cell SCs on plastic substrate, implemented with a microcontroller and two NMOS transistors. (b) The circuit schematics of the voltage equalizer in Fig. 5(a) charged with a constant current source.

As we can see in Fig. 5b, the voltages across supercapacitor cells *SC1* and *SC2* are connected to three analog inputs of the microcontroller (*in1*, *in2* and *in3*). Depending on the voltages accumulated on the *SC1* and *SC2*, the bypassing transistors *M1* and *M2* are either switched ON or OFF by the microcontroller to keep the cell voltages at the desired level. The microcontroller is powered by +5 V and a constant current source is used to charge the supercapacitor cells.

The flow chart in Fig. 6 illustrates the workflow of how the microcontroller is programmed to behave in the voltage equalizer. The first step, called initialization, is about assigning each parameter to a pin. Then the three analog inputs read the voltages across the SC cells. Next, if the voltage across the first SC cell is greater than 1 V, the *out2* pin is set to *HIGH*, thereby turning ON the transistor *M1* and bypassing the charging current. Otherwise, *M1* stays OFF and the voltage across the second SC cell is checked, and the current will be bypassed through the transistor *M2* if the voltage across the second cell exceeds 1 V. Then next cycle begins with the reading of the three analog pins again. The microcontroller runs the loop every millisecond.

The two-cell SC with the voltage equalizer in Fig. 5 was charged with a variety of constant currents (Keithley 2200 Power Supply, Tektronix, Uinted States) to verify the circuit function. Fig. 7 shows the measured waveforms of cell voltages during charging/discharging and the charge time depending on the charging current. All the waveforms were measured with an oscilloscope (PicoScope 2000, Pico Technology, United Kingdom) while all the charging was done via a Keithley 2200 Power Supply in a constant current mode.

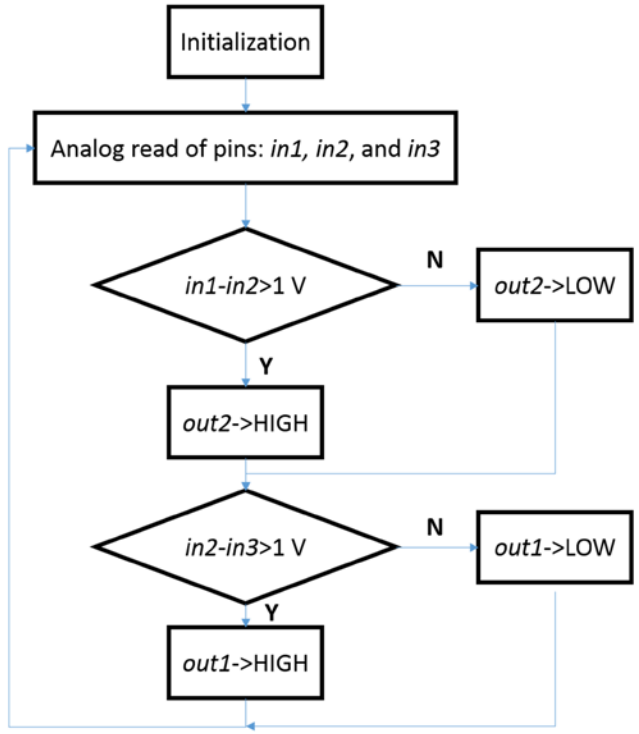

Fig. 6. The programming flow chart of the ATtiny85 microcontrollers for the voltage equalizer in Fig. 5.

The black, red and blue curves in Fig. 7a-b are the voltage across *SC2*, the sum of voltages of both SC cells, and the voltage difference of the cells, respectively. In Fig. 7a (time axis unevenly scaled), the two SC cells were charged by a 50 mA constant current source. When the cell voltage reached 1 V, charging was stopped via bypass of the charging current through *M1* or *M2*. The two cells reached 1 V almost simultaneously at time *T1* and the voltages were kept at 1 V by the voltage equalizer. When the current source was turned OFF at time *T2*, the cell voltage dropped due to self-discharging. The dentate lines of the voltages between *T1* and *T2* are due to the frequent switching of the transistors *M1* and *M2*, caused by the self-discharging voltage drop. Applying a load of 220 Ω resistor at time *T3*, the cells discharged in ~300 s. In order to investigate the maximum current that can be bypassed by this voltage equalizer, Fig. 7b shows the voltage waveforms of the SC cell when charged by a constant charging current of 500 mA that exceeds the maximum current the transistors can pass. In Fig. 7b, when V_{SC2} reaches 1 V, both transistors *M1* and *M2* switched ON at time *T1*. However, the charging current is too large for the transistors, so the *SC1* was continuously charged until the compliance voltage (2.5 V) was reached at time *T2*, while the *SC2* was kept at the desired 1 V. Turning OFF the current source at time *T3*, the *SC1* was balanced to the desired 1 V and both cells were kept at 1 V constantly. The results shows that the SC cells could not be equally charged if the charging current exceeded the maximum that the transistors could pass. It is noted that there are frequent current pulses in the measured waveforms and this is due to the frequent ON/OFF switching of the transistors, caused by the leakage current of the SC cells. To reduce the current pulses, we can either enlarge the voltage margin during the programming of the microcontrollers or lower the leakage current of the SC cells.

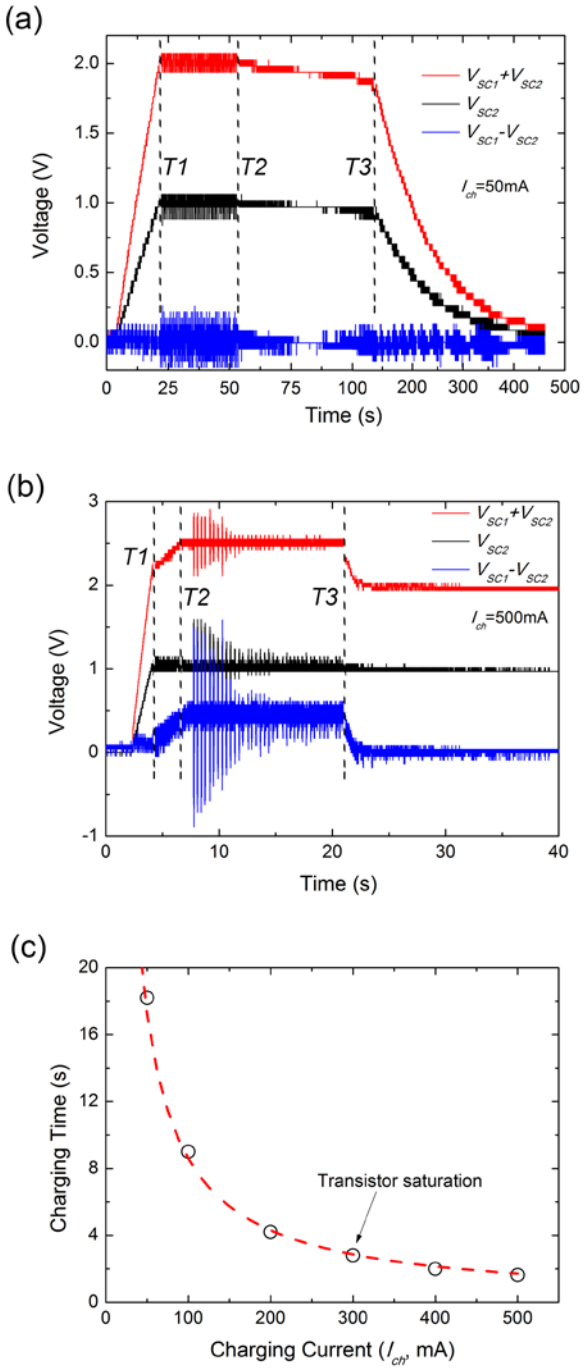

Fig. 7. Charging the SCs in Fig. 5 using constant current source of (a) 50 mA and (b) 500 mA. (c) The charging time dependent on the charging currents.

To find out the maximum charging current where the voltage equalizer works correctly (in this case, the transistors were 2N7000), the charging current was varied from 50 to 500 mA. Fig. 7c shows that the transistors were saturated at ~300 mA. Moreover, the charging time of the SCs versus the charging currents is illustrated in Fig. 7c. The dotted red line is the theoretical curve for the time it takes to charge a 940 mF SC

cell to 1 V. Given the following is true,

$Q = C \cdot V$ and $Q = I \cdot t$, *Eq. (2)*

where Q is the charge, C is the capacitance, V is the voltage, and I is the current, the charging time is calculated as follows:

$t = (C \cdot V)/I$. *Eq. (3)*

The black circles represent the measurement data. The results exhibit good matching between the theoretical and experimental data.

B. *Microcontroller and OECTs*

After verifying that the voltage equalizer functions correctly with the microcontroller and silicon NMOS transistors, we used the printed OECTs as bypass transistors instead of the silicon NMOS transistors. The hybrid voltage equalizer is designed to bypass the charging current when the voltage across the SC cells is exceeding 1 V, which is the same behavior as in the inorganic voltage equalizer discussed above. In the circuit configuration shown in Fig. 8a, there are three main differences: first, two voltage dividers offering different output voltages were used to convert the digital outputs of the microcontroller and then to obtain the desired V_{GS} = 1 V; second, a pair of deliberately imbalanced capacitors (*C1* = 6.8 µF and *C2* = 15 µF) were used to explore the balancing capability of the hybrid voltage equalizer; third, the microcontroller was programmed slightly different since the OECTs are operated in depletion mode. For the voltage dividers, different resistances were chosen accordingly, as each OECT needs a different gate voltage to switch OFF due to the different source voltages. For instance, the source terminal of *OECT2* parallel to *C2* is charged to 1 V, so 2 V is required at the gate to turn OFF *OECT2*. While the potential over *C1* is the sum of the voltage across two capacitors and it will be 2 V when both cells are fully charged to 1 V, so 3 V is required on the gate of *OECT1* parallel to *C1*. Here, the resistors are *R1* = 220 kΩ, *R2* = 330 kΩ, *R3* = 330 kΩ, and *R4* = 220 kΩ, respectively. For the microcontroller, when the *in1* - *in2* > 1 V or *in2* - *in3* > 1 V (Fig. 6), the output pin *out2* or *out1* will be set to *LOW* instead of *HIGH* to turn ON the OECTs, otherwise the OECTs are kept OFF to charge the cells by *HIGH* outputs of the *out2*/*out1*.

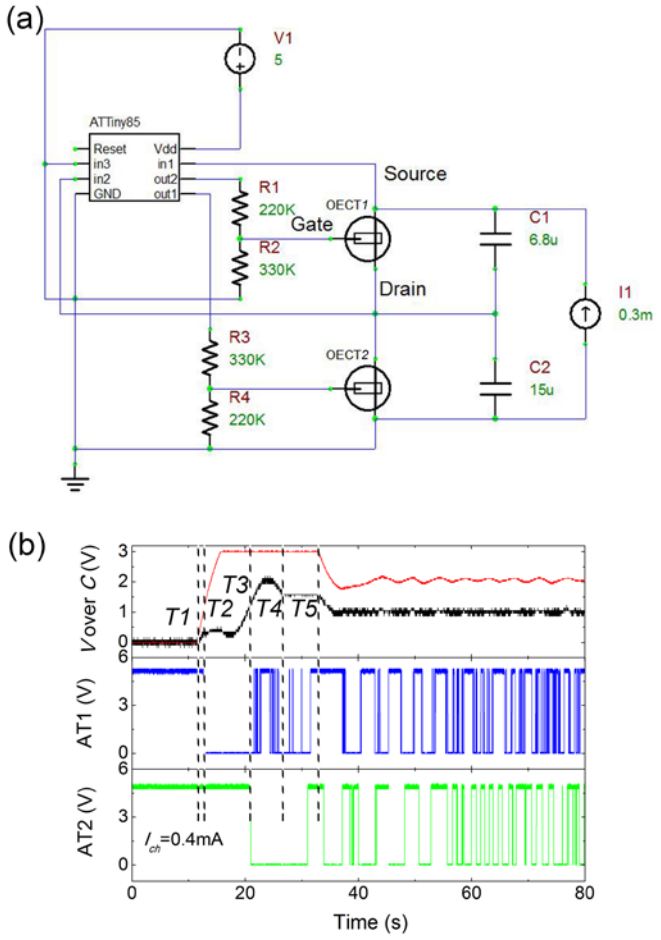

Fig. 8. (a) Circuit schematics of the hybrid voltage equalizer to balance an imbalanced pair of capacitors (*C1* = 6.8 µF and *C2* = 15 µF). Two voltage dividers provide different voltages to drive the OECTs. (b) The voltage waveforms at the capacitors and the digital outputs of the ATtiny85 microcontrollers.

Fig. 8b shows the voltage waveforms of the hybrid voltage equalizer in Fig. 8a when the capacitors were charged with a current source of 0.4 mA. The black and red curves (*V* over *C*) are the respective charging curves of the capacitor *C2* and the sum of the voltages of two capacitors (*C1*+*C2*). The blue (*AT1*) and green (*AT2*) square waves are the respective outputs (*out2*, *out1*) of the microcontroller.

Initially, both transistors were set to OFF-state. At time *T1*, the current source was turned *ON* and both capacitors started being charged. When the voltage of *C1* (smaller capacitor) reached 1 V at time *T2*, the *OECT1* was switched ON, and bypassed the current. However, this involved a delay, leading to charging to the compliance voltage of 3 V. The main reason for the delay is that it took a few seconds for the OECTs to turn ON due to the slow turning ON of the OECTs discussed above. So, the charging did not stop immediately after the OECT switched ON. Meanwhile, *C2* was still charging, and when its voltage reached 1 V at time *T3*, *OECT2* was switched ON and bypassed the current. The slow switching of the OECTs is partly due to the low humidity. Generally, PEDOT:PSS OECTs are sensitive to humidity and they show slower response below a humidity level of 25%RH (with the current choice of electrolyte). The humidity dependency can be circumvented by encapsulation, even though this adds complexity to the manufacturing process. In the stage between *T4* and *T5*, both capacitors were equally charged to 1.5 V. At time *T5*, the current source was turned OFF, and both cell voltages dropped down and re-balanced to the desired 1 V. The fluctuations seen at the end of the curves are due to the ON/OFF switching of the OECTs to keep the voltage at 1 V.

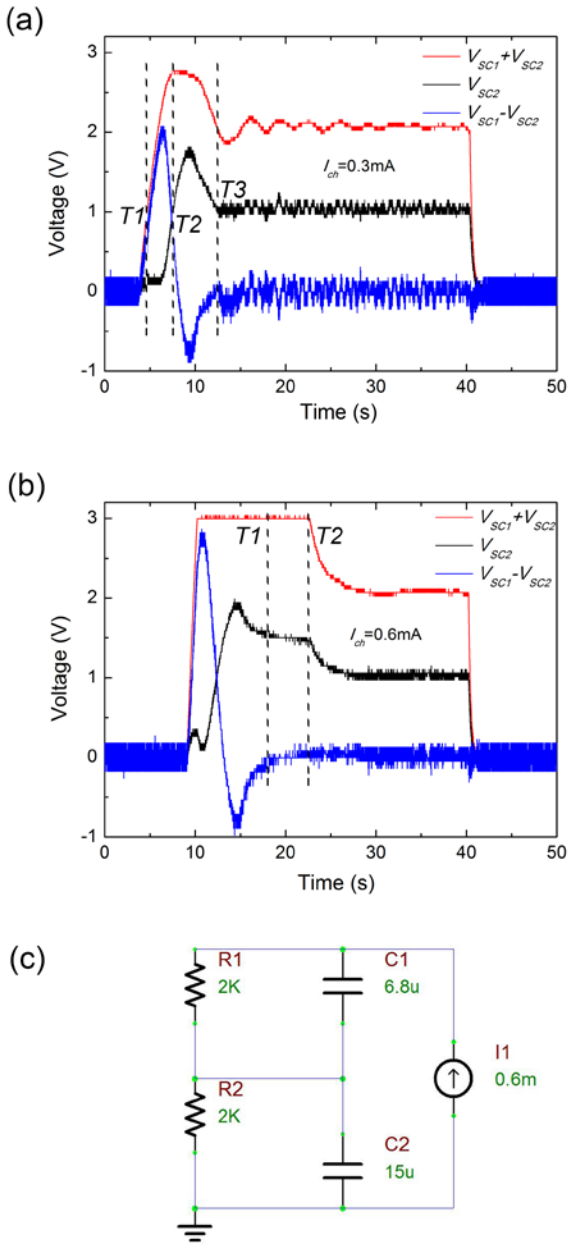

Fig. 9. (a) The voltage waveforms of the capacitors in Fig. 8(a) with charging currents (a) 0.3 mA and (b) 0.6 mA. (c) The equivalent circuit of Fig. 8(a) when the charging current is greater than 0.3 mA.

In order not to hit the compliance voltage during the charging, the charging current was lowered to 0.3 mA (Fig. 9a). Similarly, the *OECT1* and *OECT2* were switched ON at time *T1* and *T2*, respectively, to bypass the charging current. Although the overshooting of the cell voltages (red and black curves), due to the slow switching of the OECTs, and the voltage difference (blue curve) between the two capacitors could be observed in the beginning of measurement, the two largely imbalanced capacitors reached the desired 1 V simultaneously in ~7.5 s (*T1* to *T3*). At t = 40 s, the charging was stopped and the capacitors were discharged through a 220 Ω resistor.

The charging current was then increased to investigate the maximum current that the hybrid voltage equalizer can bypass. Fig. 9b shows the voltage waveforms of the two capacitors when charged with 0.6 mA current. In the interval when both OECTs were ON in order to bypass the current (*T1* and *T2*, as well as *T4* and *T5* in Fig. 8b), the compliance voltage of 3 V was divided equally between the two cells. This means that both cells charged to the same voltage despite the difference in capacitance, and hence were balanced. On the contrary, the voltage equalizer with silicon NMOS transistors was not able to charge the two cells equally, if the charging current exceeded the maximum current that the transistors could pass (Fig. 7b). Due to the 2 kΩ internal resistance (ON-state) of the OECTs, the hybrid voltage equalizer works in constant-resistor mode (the equivalent circuit is shown in Fig. 9c) when the charging current exceeds the maximum current that the OECTs can pass. These results indicate a dual-mode operation for the hybrid voltage equalizer. Expressly, the equalizer works in either switch-transistor mode at low charging currents or in constant-resistor mode at high charging currents. When the current source was turned OFF at *T2*, the two capacitors were re-balanced to the desired 1 V from the equally-divided 1.5 V. At t=40 s, the capacitors were discharged through a 220 Ω resistor.

The charging time versus the charging currents of the hybrid voltage equalizer is shown in Fig. 10. The dotted red line is the theoretical curve of the time needed to charge a 6.8 μF capacitor to 3 V with a constant current source (from 0.3 to 2 mA), and, the black circles stand for the measured data of the hybrid voltage equalizer. As we can see from the figure, it takes up to 2.8 s to charge the capacitor with the hybrid voltage equalizer with a charging current of 0.3 mA, which is much slower than the theoretical value. Compared with Fig. 7c, where silicon transistors were used with good matching between the theoretical and the experimental data, this discrepancy can be explained by the slow speed of the OECTs in turning ON and OFF and the leakage current going into the OECTs.

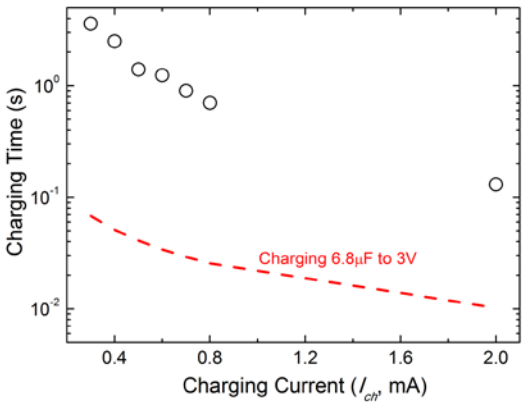

Fig. 10. The charging time dependent on the charging currents of the hybrid voltage equalizer in Fig. 8(a).

The same two-cell SC (940 mF each, 470 mF in total) in Fig. 5b was used to replace the pair of capacitors in Fig. 8a in order to show the ability of the hybrid voltage equalizer for SC

balancing during charging. As shown in Fig.11 (time is unevenly scaled), at *T1*, a current source of 100 mA was turned ON, resulting in both cells starting being charged. When the current source reached the compliance voltage of 3 V at *T2*, the charging stopped and both cells were charged equally to 1.5 V. The hybrid voltage equalizer worked in a constant-resistor mode as shown in Fig. 9c. The voltage of the two cells was maintained at 1.5 V until the current source was turned OFF at *T3*. The cell voltages dropped slightly due to self-discharging between *T3* and *T4*. Finally, the SC was discharged through a 220 Ω resistor. The voltage difference (blue curve in Fig. 11) is only 2.9 mV between intervals of *T2* and *T3*.

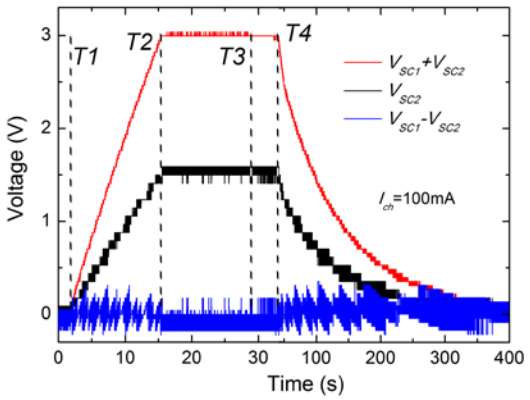

Fig. 11. The voltage waveforms of the two-cell SC charged with 100 mA current through the hybrid voltage equalizer that worked in the constant-resistor mode shown in Fig. 9(c).

The equal charging of the two largely different capacitors (6.8 μF and 15 μF) and the two-cell SCs, shows that the hybrid voltage equalizer is able to balance series-connected energy storage cells operating in either switched-transistor mode or constant-resistor mode. In order to minimize the current limitation in the switched-transistor mode, the OECTs can be designed to deliver higher current by enlarging the channel width or by using PEDOT:PSS with higher conductivity. In the constant-resistor mode, the equalizer has no maximum limit for the charging current. Also, in a practical device, a built-in switch to stop the charging, which is currently being provided by the voltage compliance of the measuring instrument, is needed.

IV. Conclusion

A silicon-organic hybrid voltage equalizer, consisting of a microcontroller and printed OECTs, has been demonstrated in order to balance and protect two-cell SCs during charging. Printed OECTs with an ON-conductance of 0.5 mS were used to bypass excess current while the SCs were fully charged to the desired voltage. The microcontroller was used to sense the voltages of the SC cells and switch the OECTs for bypassing charging current when needed. With the hybrid voltage equalizer, a pair of imbalanced capacitors (6.8 μF and 15 μF) were charged equally. Depending on the charging current, the hybrid voltage equalizer worked either in switched-transistor mode or constant-resistor mode, thanks to the 2 kΩ ON-resistance of the OECTs. Despite the superior performance of an all-silicon reference equalizer, it only worked in switched-transistor mode. The main challenge for the hybrid voltage equalizer is the long turn-ON time (up to seconds, depending on the humidity) of the OECTs, which limits its response speed to overcharging. The switching speed of the printed OECTs can be improved through materials and device structure [10, 14]. The hybrid voltage equalizer, as a good example of hybrid electronics, paves a road towards low-cost fully-integrated energy storage systems with printed SCs.

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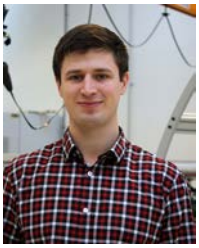

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