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Design and Analysis of Battery-Integrated Modular Multilevel Converters for Automotive Powertrain Applications

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Abstract

The automotive industry has grown considerably over the last century consequently increasing greenhouse gas emissions and thus contributing towards increase in the average global temperature. It is thus of paramount importance to increase the use of alternative energy sources. Electric vehicles have gained popularity over the last decade. However, a major concern with electric vehicles is their range. The range of an electric vehicle is limited by the battery pack, in particular, the weakest cell of the pack. One method of increasing the available energy from the battery pack is by introducing more electronics. Modular multilevel converters, with their modular concept, could be a viable solution. The concept of battery-integrated modular multilevel converters (BI-MMC) for automotive applications is explored. In particular, the impact of the number of cascaded cells per submodule is investigated, considering battery losses, DC-link capacitor losses, and the converter losses. Furthermore, an optimization of the DC-link capacitors and the selection of MOSFET switching frequency is presented in order to minimize the total losses.

Keywords

≪DC-AC converters≫, ≪Modular Multilevel Converters (MMC)≫, ≪Power converters for EV≫. ≪Electric vehicle≫, ≪Hybrid Electric Vehicle (HEV)≫,

Introduction

The average global temperature has risen considerably because of greenhouse gas emissions [1]. Although the energy sector holds the major share of greenhouse gas emissions, the automotive industry accounts for about 15% of the CO_2 emissions [2]. Therefore, it is of paramount importance to increase the utilization of alternative energy carriers that can replace fossil fuels in both the automotive and energy industries. Automotive battery packs are typically made up of modules. Each module contains several parallel and/or series-connected cells [3]. However, the energy and power are determined not only by the cell type and size but to a large extent also by the configuration and battery management system (BMS) [4, 5]. By restructuring the cell interconnections and introducing more electronics in the pack, more precise control and thus better utilization of the energy in the individual modules can increase the energy and provide more benefits such as improved battery life and increased usable capacity of the battery pack [6, 7].

Presently, EV powertrains typically use a conventional 2-level voltage source inverter with a large battery pack [8]. The battery pack typically contains low-voltage battery cells (e.g. 2–4 V) that are connected in series (strings) providing high-voltage (e.g. 300 – 1000 V) [9]. These strings are then connected in parallel to achieve the required power rating. Because of differences in leakage currents and cell in-homogeneities, individual cell voltage and state-of-charge (SOC) distribution among the cells are non-homogeneous. As a result, some cells discharge faster than other cells, thus limiting the total energy that can be delivered by the pack. In order to mitigate this problem, cell balancers are employed as part of the battery management systems (BMS) [4]. In order to maximize the energy delivered by the battery pack, individual cell control is often preferred.

Modular multilevel converters (MMCs), have gained interest and high popularity over the last several years in the power distribution sector especially in HV and MV applications where it has been proven to give several advantages; such as low THD, modularity, and scalability [10, 11]. Over last few years, battery-integrated MMCs (BI-MMC) have gained popularity especially for battery energy storage systems (BESS) [12–14]. Several pieces of research indicate that there is a great benefit in increasing the controllability of the cells in terms of battery life-time and battery utilization [15, 16]. The slightest increase in the battery lifetime and battery utilization typically results in monumental benefits [17]. BI-MMCs are thus particularly interesting for EV powertrains because of their high efficiency, greater cell-level control, and provide better battery fault isolation [18–22]. A comparative assessment between half-bridge and full-bridge MMCs, and cascaded H-bridge inverters was performed for BESS [23]. The study reported that cascaded H-bridge inverters had higher efficiency. Although the shown interesting effort in literature, these articles do not investigate the impact of the number of battery cells per submodule, DC-link capacitor design, and MOSFET switching frequency on the efficiency of BI-MMCs.

This paper develops and presents the principle optimization of DC-link capacitor and MOSFET switching frequency for a wide range of BI-MMC topologies with different number of cascaded cells per submodule for hybrid and electric vehicles. Furthermore a comparison between five different 400 kW 3-phase MMC topologies and a 3 phase 2-level voltage source is presented for a 40 ton commercial vehicle. Although the evaluation is performed considering automotive applications, the procedure is generic and can also be applied to BESS.

Topology review

A 3-phase BI-MMC topology consists of either one or two arms per phase (N_{arms}) and each arm is made up of number of cascaded stages of DC/AC converters and are commonly referred to as submodules (SM). The DC side of a submodule contains a battery pack and are configured with $N_{s(cells)}$ series and $N_{p(cells)}$ parallel cells. The submodules can be broadly classified into half-bridge (HB) and full-bridge (FB) SMs, as seen in Fig. 1. The HB-SM is shown in Fig. 1(a) and the FB-SM is shown in Fig. 1(b). Here the DC-link capacitor is modeled as an RLC series network as seen in Fig. 1. The RMS output voltage of the HB-SM ($U_{sm(hb)}$), and FB-SM ($U_{sm(fb)}$) can be written as follows:

$$U_{sm(hb)} = M\frac{U_s}{2}, \qquad U_{sm(fb)} = M\,U_s, \tag{1}$$

where M is the maximum modulation index.

Fig. 2 presents several BI-MMC topologies. These topologies include the double-star half-bridge (DSHB), double-star full-bridge (DSFB), single-star half-bridge (SSHB), single-star full-bridge (SSFB, also known as cascaded H-bridge), and single-delta full-bridge (SDFB). In this paper the DSFB topology analyzed is a parallel combination of two SSFB topologies. Furthermore, all presented topologies belongs to the set *Top*.

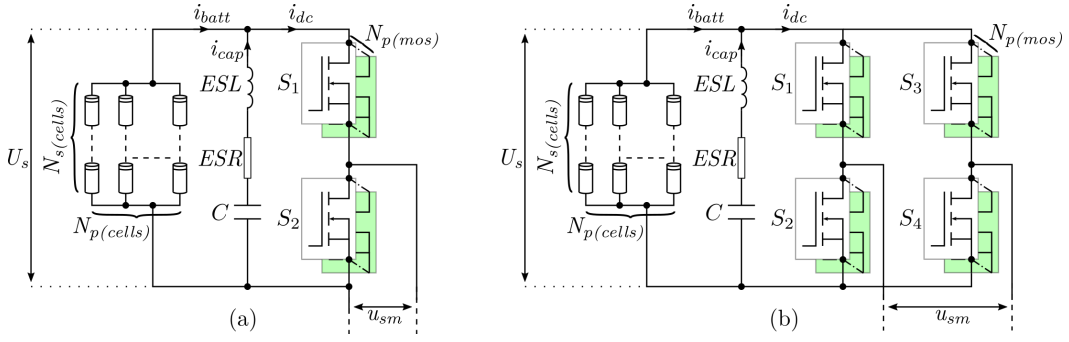

Fig. 1: Battery Integrated MMC submodules, (a) half-bridge, and (b) full-bridge submodules.

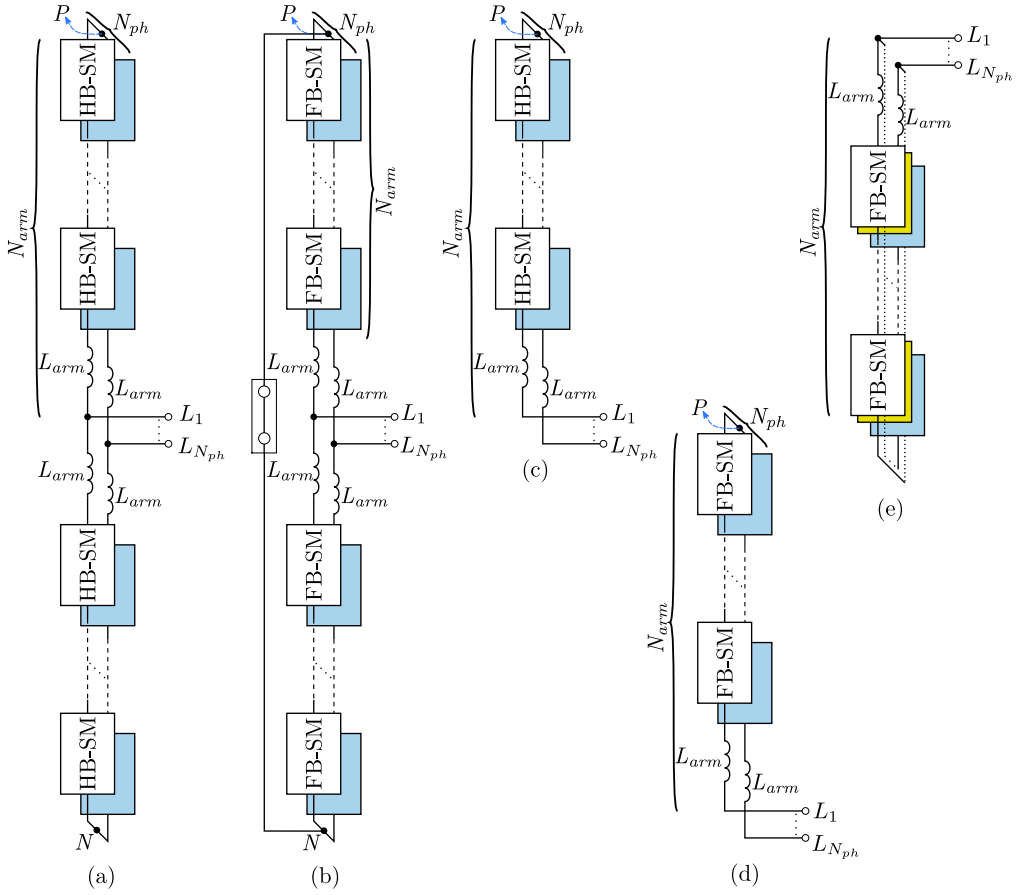

Fig. 2: Schematic of battery integrated MMC topologies for N_{ph}-phase system. (a) Double-star half-bridge, (b) double-star full-bridge, (c) single-star half-bridge, (d) single-star full-bridge, and (e) single-delta full-bridge topologies.

Battery-Integrated Modular Multilevel Converter: Modeling and Design

This section presents the battery model, converter losses and number of parallel MOSFETs calculation, DC-side SM current harmonics calculation, SM DC-link capacitor impedance, DC-link capacitor and battery current calculations, and the resonance between the battery and DC-link capacitor. This section also presents an example of losses vs the energy stored in the DC-link capacitor and MOSFET switching frequency. In particular, the influence of the resonance on the losses is discussed. Furthermore, the DC-link capacitor design optimization for all the topologies is also presented.

Battery Modeling

Fig. 3 presents the electrochemical impedance spectroscopy (EIS) performed on a 24 Ah Li-ion NMC battery cell. The EIS shows the battery impedance (Z_{batt}) from 0.025 Hz to 100 kHz. It is worth mentioning that, for the sake of simplicity, the battery loss model incorporated in the paper does not include the reversible battery losses. This is because the entropic coefficient is a highly non-linear function of current, and battery state-of-charge [24].

Semiconductor losses and thermal rating

A SM contains 2 or 4 switches (for HB and FB SMs, respectively) each defined with $N_{p,mos}$ parallel MOSFETs related to thermal design conditions. Every MOSFET has an on-state resistance of $R^{max}_{ds(on)}$. The conduction loss for a switch, $P_{c,sw}$, is determined by the RMS current through the switch corresponding to $1/\sqrt{2}$ of the RMS arm current. The switching loss for a switch, $P_{s,sw}$, is determining as the product of energy dissipated during average switching transients and the switching frequency. The conduction losses ($P^{max}_{c,sw}$) and switching losses ($P^{max}_{s,sw}$) of a switch at rated power are written as follows:

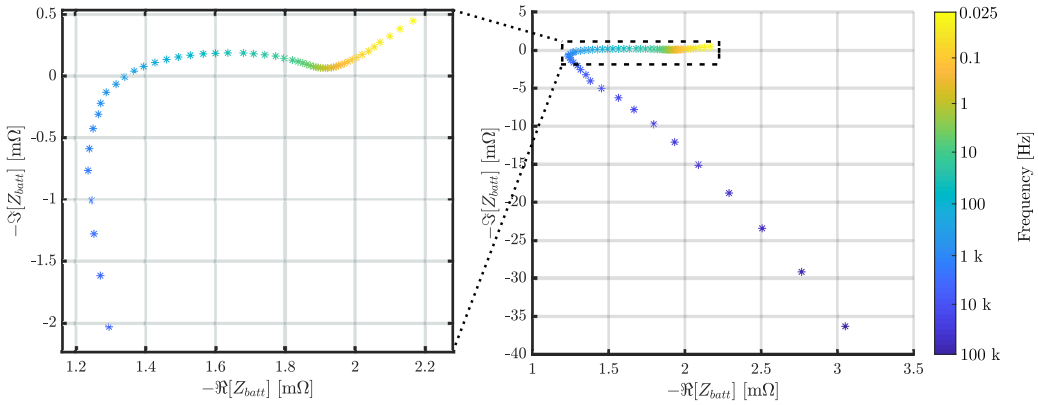

Fig. 3: Electochemical impedance spectroscopy for Samsung 24 Ah NMC Li-ion prismatic cell.

$$P_{c,sw}^{max} = \frac{1}{2}\,(I_{arm}^{max})^2\,\frac{R_{ds(on)}^{max}}{N_{p,mos}}, \qquad P_{s,sw}^{max} = \frac{2\sqrt{2}}{\pi}\,U_s\,I_{arm}^{max}\,t_{sw(tran)}\,f_{sw}, \tag{2}$$

where $t_{sw(tran)}$ is the combined switching transient time corresponding to the sum of current rise and voltage fall time at turn-on and the voltage rise and current fall time at a turn-off, i.e, $t_{sw(tran)} = t_{ri} + t_{fi} + t_{rv} + t_{fv}$, and f_{sw} is the switching frequency. I_{arm}^{max} represents the RMS arm current in the BI-MMC at rated power, considering sinusoidal fundamental frequency current wave shape, where the absolute average is given by the factor $2\sqrt{2}/\pi$. The rise and fall times for the voltage and current are calculated considering a constant dv/dt and di/dt, respectively. di/dt is a rather critical design parameter as it determines MOSFET drain-source voltage ripple. di/dt is calculated using:

$$\frac{di}{dt} \approx \left[\frac{1}{L_{cap}}\left(\Delta U_{ds}^{def} - R_{cap}\,\sqrt{2}\,I_{arm}^{max}\right)\right]_{\left.\frac{di}{dt}\right|_{min}}^{\left.\frac{di}{dt}\right|_{max}}, \tag{3}$$

where L_{cap} is the parasitic inductance between the DC-link capacitor and the MOSFET drain terminals, ΔU_{ds}^{def} is the maximum allowable drain-source voltage ripple, I_{arm}^{max} is the maximum arm current, and $di/dt|_{min}$ and $di/dt|_{max}$ are the minimum and maximum di/dt, respectively. $di/dt|_{min}$ and $di/dt|_{max}$ are determined by the choice of MOSFETs. It is assumed that the voltage drop due to C_{cap} is negligible.

In automotive applications, the thermal management is critical parameter that has to be considered for the converter design. The cooling principle considered is based on cooling collectors underneath the converter PCB, where micro-vias conduct heat from the MOSFETs. The thermal resistance of the active cooling area per MOSFET, $R_{\theta pad}$ is determined by the thermal resistance of the micro-via contacts below the MOSFETs. The crucial temperature conditions of MOSFETs are the junction and the case temperatures, where for this design case temperature has been found to be limiting. The case-to-ambient temperature rise (ΔT_{ca}) can be written as follows:

$$\Delta T_{ca} = T_c - T_a = N_{sw}\,(P_{c,sw} + P_{s,sw})\,\frac{R_{\theta pad}}{N_{p,mos}\,N_{sw}} = \left(\frac{1}{2}\left(\frac{I_{arm}^{max}}{N_{p,mos}}\right)^2 R_{ds(on)}^{max} + \frac{P_{s,sw}}{N_{p,mos}}\right) R_{\theta pad}, \tag{4}$$

where T_c is the case temperature, T_a is the ambient temperature, and N_{sw} gives the number of switches per submodule.

In order to limit the MOSFET case to ambient temperature rise, $N_{p,mos}$ is determined from (4) using:

$$N_{p,mos} = \left[\frac{2\,I_{arm}^{max2}\,R_{ds(on)}^{max}}{\sqrt{P_{s,sw}^{max2} + \frac{2\,\Delta T_{ca}^{max}\,I_{arm}^{max2}\,R_{ds(on)}^{max}}{R_{\theta pad}}} - P_{s,sw}^{max}}\right]_{N_{p,mos}^{min}}^{N_{p,mos}^{max}}, \tag{5}$$

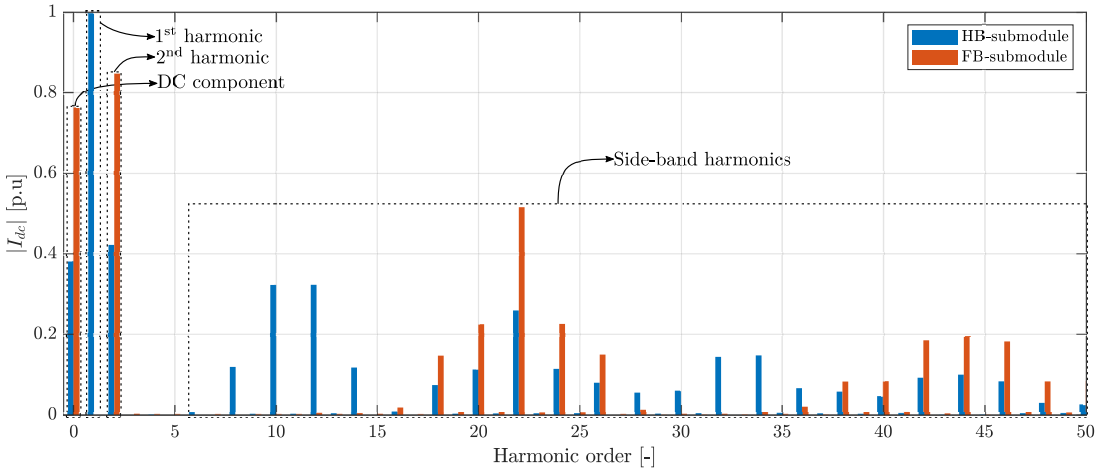

Fig. 4: The DC-side currents for HB and FB submodules considering $f_{sw} = 11\, f_1$ and $\cos(\phi) = 0.8$.

where ΔT_{ca}^{max} is the maximum case-to-ambient temperature rise, $N_{p,mos}^{max}$ and $N_{p,mos}^{min}$ are maximum and minimum $N_{p,mos}$, respectively.

Submodule DC-side currents and loss calculation

The instantaneous DC-side SM current ($i_{dc}\ (t)$) is calculated as follows:

$$i_{dc}(t) = \mathcal{S}_{conv}(t)\ i_{arm}(t), \tag{6}$$

where $i_{arm}(t)$ represents the instantaneous arm current of the BI-MMC, and $\mathcal{S}_{conv}(t)$ is the converter/SM switching function. For simplicity, this paper considers a phase-shifted carrier based modulation. Fig. 4 shows the DC-side currents for the HB and FB submodules with a switching frequency, $f_{sw} = 11\, f_1$, where f_1 is the fundamental frequency. From the figure it is clear that the DC-side currents for the HB-submodule contains DC, 1st, 2nd, and all the side-band harmonic components. However, the DC-side currents for the FB-submodule consists of DC, 2nd, and only the even carrier multiples as the side-band harmonic components.

DC-link capacitor impedance calculations

The DC-link capacitor capacitance (C_{cap}) is defined based on the total energy stored in the capacitor ($E_{cap(tot)}$). In the example in Fig. 5, the capacitor effective ESR (R_{cap}) is calculated based on the dissipation factor ($\tan\delta$). C_{cap}, R_{cap} and the capacitor impedance (Z_{cap}) are calculated as follows:

$$C_{cap} = \frac{2\, E_{cap(tot)}}{{U_s}^2\, N_{sm(tot)}}, \qquad R_{cap} = \frac{\tan\delta}{2\pi\, f_{sw}\, C_{cap}}, \qquad Z_{cap} = R_{cap} + \frac{1}{j\,2\pi\, f\, C_{cap}}, \tag{7}$$

where $N_{sm(tot)}$ represents the total number of submodules.

Battery and DC-link capacitor losses and resonance

Using the battery and the capacitor impedances, the battery and capacitor RMS currents (I_{batt} and I_{cap}, respectively) (see Fig. 1), are calculated using the following:

$$I_{batt} = I_{dc}\, \frac{Z_{cap}}{Z_{cap} + Z_{batt}}, \qquad I_{cap} = I_{dc}\, \frac{Z_{batt}}{Z_{cap} + Z_{batt}}, \tag{8}$$

where I_{dc} is the DC-side RMS current.

The battery (P_{batt}) and capacitor (P_{cap}) losses are calculated using the following relation:

$$P_{batt} = \sum_{k=0}^{\infty} {I_{batt}}^2(2\pi\, k\, f_1)\ \Re\left[Z_{batt}(2\pi\, k\, f_1)\right], \qquad P_{cap} = \sum_{k=0}^{\infty} {I_{cap}}^2(2\pi\, k\, f_1)\ R_{cap}. \tag{9}$$

There exists a resonance, at f_{res}, between the battery and the DC-link capacitor given as follows:

$$f_{res} = \frac{1}{2\pi\sqrt{L_{\mathcal{B}}\, C_{cap}}}, \qquad L_{\mathcal{B}} = L_s \frac{N_{s(cells)}}{N_{p(cells)}} + L_{\mathcal{C}}, \tag{10}$$

where L_s is the inductance of the battery cell and $L_{\mathcal{C}}$ is the parasitic inductance between the terminals of the battery and the converter. It is assumed that the ESL of the unit capacitor is negligible since it is considerably lower than the L_s and $L_{\mathcal{C}}$. Also, the battery double-layer capacitance and Warburg impedances are neglected since they are significantly larger than C_{cap}.

Loss variation with capacitor size and switching frequency

Two key parameters driving the loss distribution between battery, DC-link capacitor, and converter are the capacitor energy rating and the converter switching frequency. As discussed above, a resonance is obtained between battery inductance and DC-link capacitance which defines the allocation of harmonics between the battery and the DC-link capacitor. An example of a 3-phase DSFB with 5 series battery cells per converter sub-module is presented to illustrate these principles. Fig. 5 shows the total battery losses ($P^{max}_{batt(tot)}$), total capacitor losses ($P^{max}_{cap(tot)}$), total semiconductor losses ($P^{max}_{sc(tot)}$), and total losses (P^{max}_{tot}) as a function of total energy stored in the DC-link capacitors, and MOSFET switching frequency f_{sw} for the converter operating at rated power (P^{max}_{tot}) for a 3-phase, 5 $N_{s(cells)}$, DSFB BI-MMC topology. Fig. 5(a) shows the total battery losses at rated power. The figure consists of several regions and these regions are described as follows:

Region (i): In this region, $f_{sw} < f_{res}$, as a result, the switching harmonic components of I_{dc} flows through the battery, thereby increasing $P^{max}_{batt(tot)}$. $P^{max}_{cap(tot)}$ shown in Fig. 5(b) is also high since $E_{cap(tot)}$ is low and R_{cap} is high, i.e, inversely proportional to $E_{cap(tot)}$ (see (7)).

Region (ii): In this region, $f_{sw} \approx f_{res}$, i.e, a series resonance resulting in low impedance in the loop

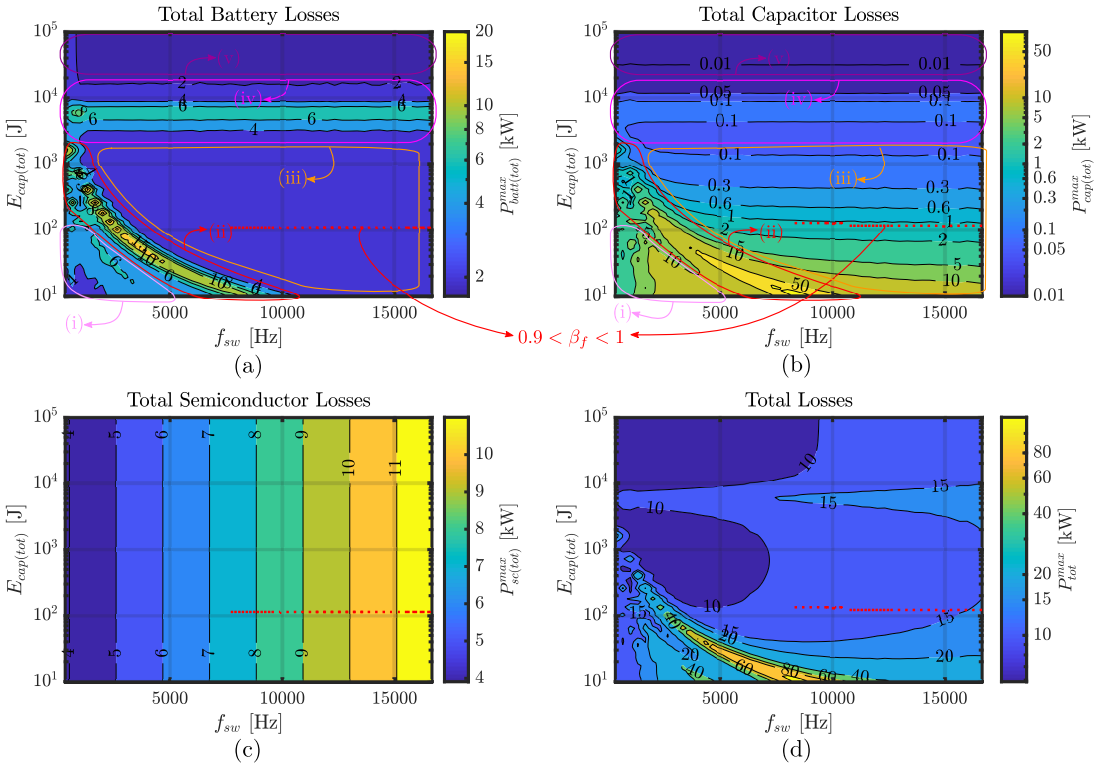

Fig. 5: Power losses as a function of total energy stored in the capacitors ($E_{cap(tot)}$), and MOSFET switching frequency (f_{sw}) for 3-phase 5-$N_{s(cells)}$ DSFB BI-MMC topology at rated power (P^{max}_{tot}). (a) Total battery losses ($P^{max}_{batt(tot)}$), (b) total capacitor losses ($P^{max}_{cap(tot)}$), (c) total semiconductor losses ($P^{max}_{sc(tot)}$), (d) total losses (P^{max}_{tot}).

between $L_{\mathcal{B}}$ and C_{cap} resulting in high circulating currents. Therefore, we observe large $P^{max}_{cap(tot)}$ and $P^{max}_{batt(tot)}$.

Region (iii): In this region, $f_{sw} > f_{res}$. Here, I_{batt} only consists of the DC-component and the 2nd harmonic (1st harmonic also for HB-SM). As a result, we observe low battery losses. Although I_{cap} consists of all the switching frequency components, $E_{cap(tot)}$ is high, thus low $P^{max}_{cap(tot)}$.

Region (iv): In this region, $f_{res} \approx 2\ f_1$, i.e, there exists a resonance close to the 2nd harmonic component. As a result, we observe increase in $P^{max}_{batt(tot)}$. However, since $E_{cap(tot)}$ is about 10^4 J, we observe little to no increase in $P^{max}_{cap(tot)}$. It is important to mention that there will exist an addition peak in this region for HB-SMs due to the presence of the fundamental component in the DC-side currents.

Region (v): In this region, $f_{res} > 2\ f_1$ ($f_{res} > f_1$ for HB-SMs), I_{batt} only consists of the DC-component. Therefore, $P^{max}_{batt(tot)}$ is minimum in this region. Although I_{cap} consists of 2nd harmonic (also, 1st harmonic for HB-SMs) components and also the switching frequency components, $E_{cap(tot)}$ is large resulting in very low capacitor losses.

Fig. 5(b) presents the $P^{max}_{cap(tot)}$ and from the figure, $P^{max}_{cap(tot)}$ can be considered to be independent of f_{sw} (when $f_{sw} > f_{res}$). Fig. 5(c) gives the total semiconductor losses. From Fig. 5(c) we observe that $P^{max}_{sc(tot)}$ is proportional to f_{sw} and is independent of the $E_{cap(tot)}$.

DC-link capacitor selection and current rating factor

The total DC-link capacitor is defined based on the total DC-link capacitor energy rating ($E_{cap(tot)}$), defined as a number of parallel units ($N_{p(cap)}$) corresponding to voltage class required for the SM DC-voltage. These capacitor units are chosen such that they have low ESR and high ripple current capability. The DC-link capacitor ripple current factor (β_f) is defined as the ratio of the capacitor RMS current (I_{cap}) to the rated capacitor RMS ripple current (I^{def}_{cap}). The effective DC-link capacitor ESR (R_{cap}) is now re-calculated based on $N_{p(cap)}$. Therefore, $N_{p(cap)}$, β_f and R_{cap} are calculated using:

$$N_{p(cap)} = \frac{C_{cap}}{C^{def}_{cap}}, \qquad \beta_f = \frac{I_{cap}}{I^{def}_{cap}}, \qquad R_{cap} = \frac{R^{def}_{cap}}{N_{p(cap)}}, \tag{11}$$

where C^{def}_{cap} is the capacitance of the unit capacitor, and R^{def}_{cap} is the ESR of the unit capacitor.

Optimization of DC-link capacitor energy and MOSFET switching frequency

As discussed in previous sections, there exists two degrees of freedom for the design of the converter system. Therefore, an optimization is set up that is defined as follows:

$$\begin{aligned} \text{objective} &: P^{opt}_{tot}\left(Top, N_{s(cells)}\right) = \min\left\{\ P^{max}_{tot}\left(E_{cap(tot)}, f_{sw} \middle| Top, N_{s(cells)}\right)\right\}, \\ \text{optimize} &: E_{cap(tot)},\ f_{sw}, \\ \text{constraints} &: 0.9 \leq \beta_f \leq 1,\ f_{sw} > f_{res}, \end{aligned} \tag{12}$$

where P^{opt}_{tot} is the minimum total loss for a given topology (Top) with $N_{s(cells)}$ as the number of series cells per submodule constraining $E_{cap(tot)}$ and f_{sw} such that $\beta_f \in [0.9,\ 1]$ and the switching frequency is above the resonance ($f_{sw} > f_{res}$) defined by (10). The narrow region (shown in red) in Fig. 5, gives the region where the constraints are satisfied. $E^{opt}_{cap(tot)}$ and f^{opt}_{sw} are the optimal total energy stored in the DC-link capacitor and optimal switching frequency, respectively.

Comparative Assessment

Based on the optimization of the converter switching frequency and DC-link capacitor size, as described in previous section, the points of minimum total losses for a minimum DC-link capacitor size related to ripple current capability are compared for 5 different topologies. The design parameters are presented in Table I. The average power consumption (P^{avg}_{tot}) for a 40 ton trunk is considered to be about 100 kW. The maximum power rating (P^{max}_{tot}) the converter is designed for is 400 kW. The total number of submodules are determined considered a maximum modulation index of 0.85. A 40 pole PMSM with nominal speed

Table I: Design parameters considering a 40 ton battery electric truck with a battery pack of 1 MWh.

Parameters	Nomenclature	Value
Average power rating	P_{tot}^{avg}	100 kW
Maximum power rating	P_{tot}^{max}	400 kW
Nominal converter frequency	f_1	333.33 Hz
Load power factor	$\cos(\phi)$	0.9
Parasitic inductance between capacitor and MOSFET	L_{cap}	2 nH
Parasitic inductance between battery terminals and PCB	L_C	200 nH
Maximum ambient temperature	T_a^{max}	40 °C
Maximum case temperature	T_c^{max}	80 °C
Maximum di/dt	$\frac{di}{dt}\Big\vert_{max}$	2000 A/μs
Minimum di/dt	$\frac{di}{dt}\Big\vert_{min}$	200 A/μs
Minimum number of parallel MOSFETs	$N_{p,mos}^{min}$	4
Maximum number of parallel MOSFETs	$N_{p,mos}^{max}$	20

of 1000 rpm is considered as the traction motor. The battery cells considered here are 24 Ah Samsung NMC Li-ion cells with a nominal cell voltage of 3.7 V. The total energy of the battery pack in the truck is about 1 MWh with a depth-of-discharge of 65%. The capacitors and MOSFETs considered for different $N_{s(cells)}$ are presented in Appendix A.

The comparative assessment also includes a 2-level inverter as a reference case. The 2-level inverter utilizes CAB450M12XM3 SiC MOSFET HB modules. The 2-level inverter has DC-link voltage of 800 V. $R_{ds(on)}$ and $R_{\theta jc}$ are determined using the MOSFET data-sheet. The case-to-ambient thermal resistance is considered to be 0.01 K/W. The 2-level inverter MOSFET switching frequency is 7000 Hz. The total energy stored in the DC-link capacitor is 992 J and 620 μF B25690A2627K201 film capacitors are considered. R_{cap}^{def}, L_{cap}, and I_{cap}^{def} are determined from the capacitor data-sheet.

Hereafter, for simplicity, DSFB, SSFB, and SDFB topologies will be referred to as FB topologies, and DSHB and SSHB topologies will be referred as HB topologies.

Fig. 6 shows the optimized total energy stored in the DC-link capacitor ($E_{cap(tot)}^{opt}$), optimized MOSFET switching frequency (f_{sw}^{opt}), number of parallel MOSFETs ($N_{p,mos}$), and total number of submodules ($N_{sm(tot)}$) for all topologies and $N_{s(cells)}$ at P_{tot}^{avg}. From Fig. 6(a) it is evident that the HB-topologies require higher $E_{cap(tot)}$ than the FB-topologies. This is due to the fact that I_{dc} of the HB-topologies have more harmonics (all carrier side-bands) when compared to FB-topologies (only even carrier side-bands). In addition, we also observe that $E_{cap(tot)}$ for all the FB-topologies are similar. The same behavior is also observed for all HB-topologies. Due to the change in voltage class of the DC-link capacitors utilized for different $N_{s(cells)}$, we observe change in slopes at 3, 6, and 9 $N_{s(cells)}$. From Fig. 6(b) it is seen that f_{sw} increases with to $N_{s(cells)}$ for all topologies due to increase in f_{res}. f_{sw} for HB-topologies is generally greater than FB-topolgies. The DSHB topology has higher f_{sw} than all other topologies. This is due to the fact that the arm current in DSHB contains both all the switching frequency side-bands. From Fig. 6(c), we observe that at higher $N_{s(cells)}$, SSHB and SSFB topologies need more number of parallel MOSFETs. This is because these topologies have only one arm per phase and therefore higher current. From Fig. 6(d), it is clear that $N_{sm(tot)}$ is inversely proportional to $N_{s(cells)}$ for all topologies. The DSHB topology has the highest $N_{sm(tot)}$ while SSFB has the least $N_{sm(tot)}$.

Fig. 7 shows the losses for all the topologies under consideration as a function of $N_{s(cells)}$ at P_{tot}^{avg}. Fig. 7(a) presents the total battery losses ($P_{batt(tot)}^{avg}$) for all topologies as a function of $N_{s(cells)}$. From the figure it is clear that $P_{batt(tot)}^{avg}$ is fairly independent of $N_{s(cells)}$. Furthermore, it is clear that all the FB topologies have similar $P_{batt(tot)}^{avg}$ and the similar behaviour is observed for all the HB topologies. However, $P_{batt(tot)}^{avg}$ for the HB topologies are significantly greater than FB topologies. This is because I_{batt} in HB topologies consists of DC, fundamental, and 2$^{\text{nd}}$ harmonic components. On the other hand, I_{batt} in FB-SMs comprises of only DC, and 2$^{\text{nd}}$ harmonic components. In the 2-level inverter, I_{batt} consists of the DC component and

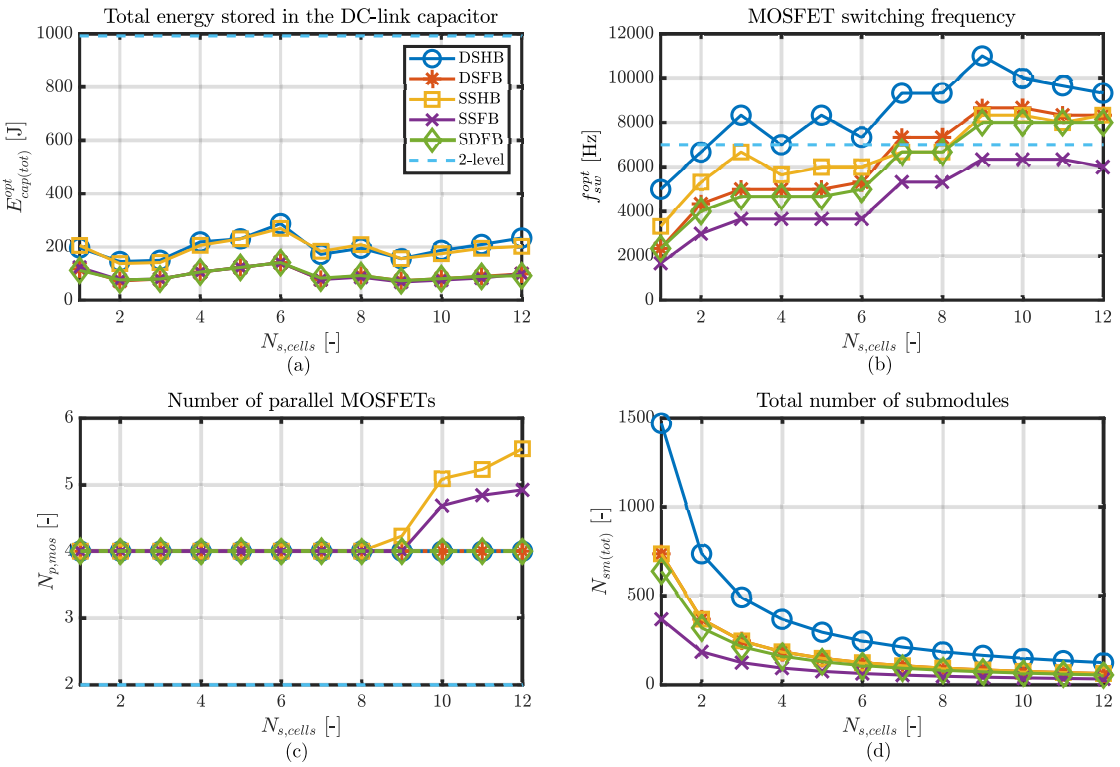

Fig. 6: Optimized design variables for all topologies and $N_{s(cells)}$ at the average power (P^{avg}_{tot}). (a) Optimized total energy stored in the DC-link capacitor ($E^{opt}_{cap(tot)}$), (b) Optimized MOSFET switching frequency (f^{opt}_{sw}), (c) Number of parallel MOSFETs per switch ($N_{p,mos}$), and (d) Total number of submodules ($N_{sm(tot)}$).

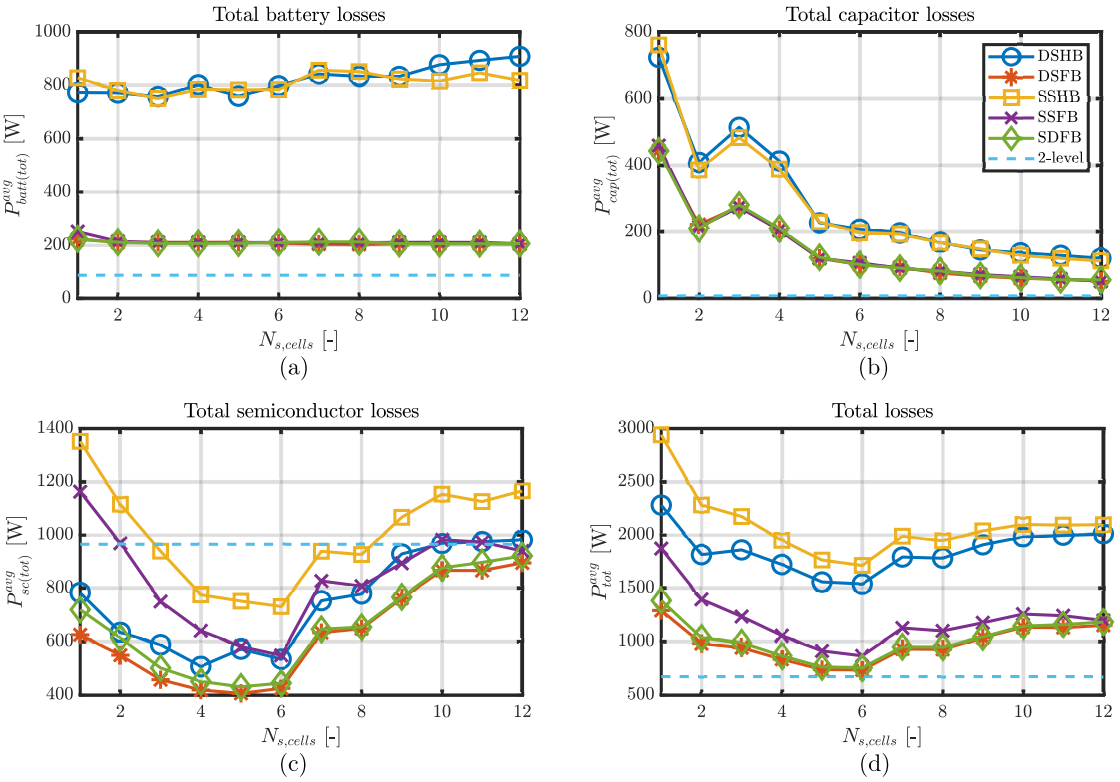

Fig. 7: Total losses for all topologies and $N_{s(cells)}$ at average power (P^{avg}_{tot}). (a) battery losses ($P^{avg}_{batt(tot)}$), (b) capacitor losses ($P^{avg}_{cap(tot)}$), (c) semiconductor losses ($P^{avg}_{sc(tot)}$), and (d) total losses (P^{avg}_{tot}).

negligible switching frequency components. As a result, we observe minimum $P^{avg}_{batt(tot)}$ for the 2-level inverter. Fig. 7(b) presents the total capacitor losses ($P^{avg}_{cap(tot)}$) as a function of $N_{s(cells)}$. From the figure it is clear that $P^{avg}_{cap(tot)}$ is relatively large for HB topologies. This is because I_{cap} for HB topologies consists of all the switching frequency components, i.e, $p \cdot f$, $2\,p \cdot f$, $3p \cdot f$, etc... However, for the FB-SMs I_{cap} consists of only the even harmonic components, i.e, $2\,p \cdot f$, $4\,p \cdot f$, etc... Moreover, from the figure it is evident that $P^{avg}_{cap(tot)}$ is inversely proportional to $N_{s(cells)}$ since $N_{sm(tot)}$ is also inversely proportional to $N_{s(cells)}$ (see Fig. 6(d)). It is important to mention that the ESR of the capacitors used for $N_{s(cells)} \geq 3$ is about 3 times that of the capacitors used for $N_{s(cells)} < 3$, due to the change in voltage class of the capacitors. As a result, we observe momentary spike in $P^{avg}_{cap(tot)}$ at 3 $N_{s(cells)}$. The 2-level inverter has the least $P^{avg}_{cap(tot)}$ since ESR of film capacitors are significantly lower than the polymer capacitors considered for BI-MMC. Fig. 7(c) presents the total semiconductor losses ($P^{avg}_{sc(tot)}$) as a function of $N_{s(cells)}$. From the figure, it is clear that the DSFB and SDFB have the least losses. This is because the DSFB has 2 arms per phase, thereby reducing the current. In the SDFB, the current through the MOSFETs is reduced due to the delta connected phase arms. The DSHB has higher losses since it has the largest $N_{sm(tot)}$ and f^{opt}_{sw}. The SSFB, despite having least $N_{sm(tot)}$ and f^{opt}_{sw}, has higher losses because it has only one arm per submodule. The SSHB also have higher losses because of high MOSFET switching frequency, high $N_{sm(tot)}$ and contains only one arm per phase. $P^{avg}_{sc(tot)}$ increases with $N_{s(cells)} > 6$, since both the MOSFET $R_{ds(on)}$ and also the switching frequency increases. Also, $P^{avg}_{sc(tot)}$ increases with $N_{s(cells)} < 3$, since the total number of submodules increases proportionally with decrease in $N_{s(cells)}$ but however, this is not compensated by the MOSFET $R_{ds(on)}$, as it does not reduce in the same proportion with lower with $N_{s(cells)}$. Most BI-MMC topologies with more than 2 cells per sub-module give lower converter losses compared to the 2-level inverter.

Discussion

The performance of BI-MMCs depend heavily on the semiconductor area and the rating of the DC-link capacitor. Increasing both semiconductor area and over-rating capacitors could lower losses for BI-MMCs. Topologies with low $N_{s(cells)}$ have a higher degree of cell control but however, they encounter relatively higher losses. In order to achieve low losses for BI-MMCs with 1 or 2 $N_{s(cells)}$, the number of parallel MOSFETs can be increased. The improved controllability of the cells could compensate for the challenges, such as improving the battery lifetime, that arise when the batteries are subjected to large second-harmonic components (fundamental components also in HB topologies). Although the DSHB topology has significant higher loses, the benefit of providing simultaneous DC-link voltage for DC-charging and feeding auxiliary loads, and AC for the traction motor makes it an attractive candidate for automotive applications.

Conclusion

Several battery-integrated MMC (BI-MMC) based inverter topologies are investigated in this paper. The evaluations also includes a reference case which is the conventional 3-phase 2-level voltage source inverter (2-level). All the investigated topologies considered a maximum power rating of 400 kW. The topologies are evaluated for number of cascaded cells per submodule and then a compared for battery losses, DC-link capacitor losses, semiconductor losses, and total losses.

The evaluation of topologies for $N_{s(cells)}$ shows that the topologies with 5 to 6 $N_{s(cells)}$ prove to have similar total losses to the 2-level inverter. However, considering only the semiconductor and capacitor losses, we observe that most BI-MMC topologies with $2 - 10$ $N_{s(cells)}$ have lower losses than the 2-level inverter. The BI-MMC topologies have higher battery losses when compared to the 2-level inverter. However, the capacitor energy requirement on the BI-MMC topologies are lower than the 2-level inverter. Although BI-MMCs have higher battery losses than the 2-level inverter, the high modularity provides increased controllability of cells which is expected to extend lifetime and battery utilization.

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A MOSFET and capacitor data

Table II: MOSFET database

$N_{s(cells)}$	MOSFET	V_{ds} [V]	$R_{ds(on)}$ [mΩ]	$R_{\theta jc}$ [K/W]	$R_{\theta pad}$ [K/W]
1	LiU MOSFET [25]	5	0.25	1.4	3.7
2 – 3	SiR178DP	20	0.4	1.2	10.2
4 – 6	NTMTS0D4N04CL	40	0.4	0.61	10.2
7 – 9	NTMTS0D7N06CL	60	0.68	0.5	4.2
10 – 12	NVBLS1D1N08H	80	1.05	0.48	1.9

Table III: Capacitor database

$N_{s(cells)}$	Capacitor	C_{cap}^{def} [μF]	V_{cap}^{dc} [V]	R_{cap}^{def} [mΩ]	I_{cap}^{def} [A]
1	T530X108K004	1000	4	5	7
2	T530X337K010	330	10	5	7
3 – 4	T530X157K016	150	16	15	4.5
5 – 6	T541X107K025	100	25	15	3.3
7 – 8	T541X476K035	47	35	15	3.3
9 – 12	T541X336K050	33	50	15	3.3